Lowering the Environmental Impact of High-*k* and Metal Gate-Stack Surface Preparation Processes

(*Task Number: 425.028)*

PIs

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- **Kedar Dhane, PhD, Chemical Engineering, U of Arizona (now with Intel)**
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- **Davoud Zamani, PhD candidate, Chemical Engineering, U of Arizona**
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Cost Sharing:

- **$50k from Stanford CIS**
- **$50k from WSP**

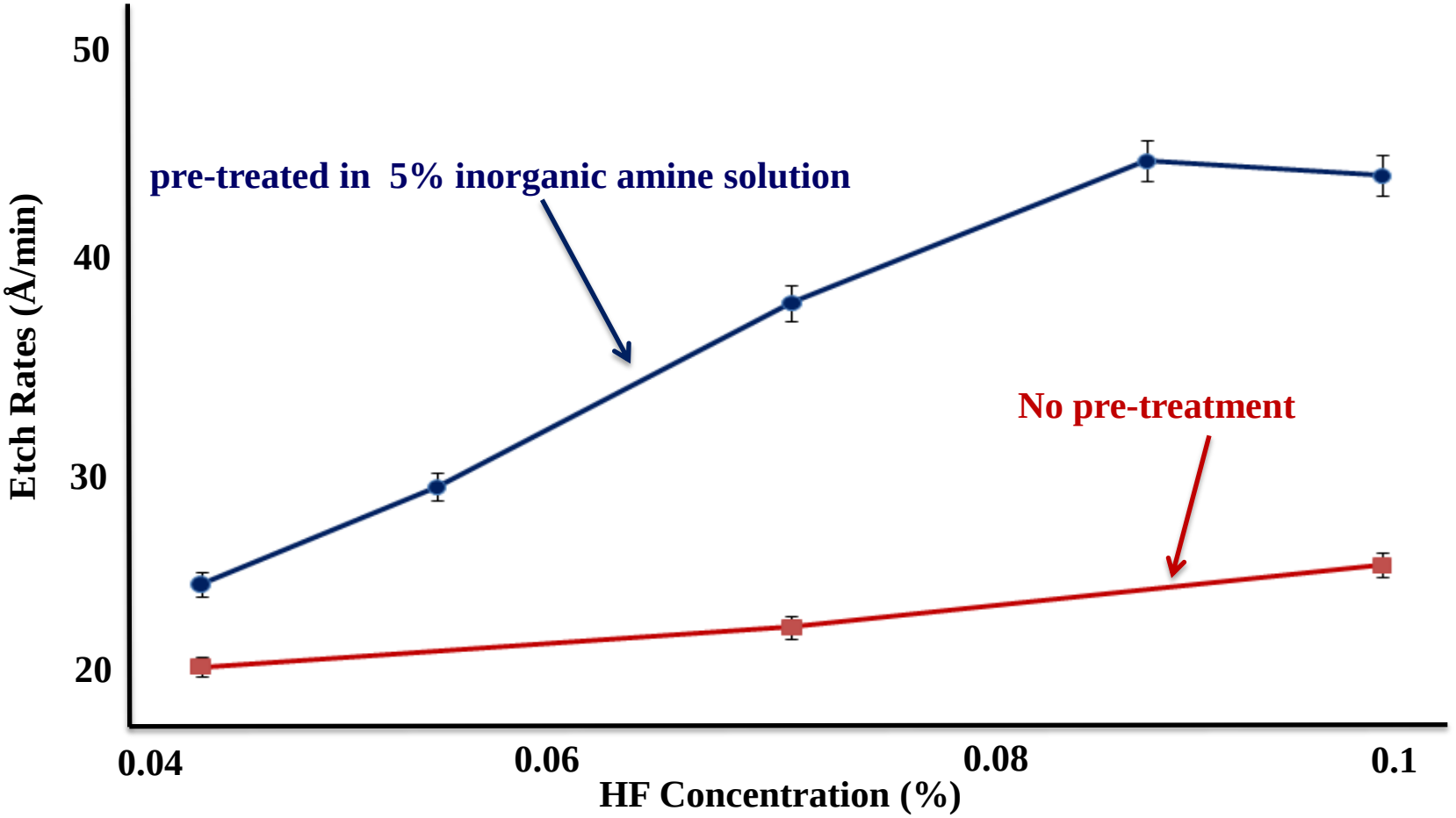
Objectives

- **Development of a wet etch method to lower fluoride consumption during etching of hafnium based high-*k* materials**
- **Investigate the rinsing fundamentals of micro and nano structures in hafnium based high-*k* materials; develop new technologies (hardware, process models, and process recipes) to reduce water and energy usage during these processes.**

Subtasks 1 and 2

- **A wet etch method to reduce fluoride consumption during etching of high-*k*.**
- **Reduction of water and energy usage for rinse after high-*k* etch.**

ESH Gain in Etching of Hafnium Silicate



Reductive pretreatment of hafnium silicate ($HfSi0_{0.74}O_{3.42}$) in 5% inorganic amine solution improves the etch rate in 1:1000 HF:H_2O.

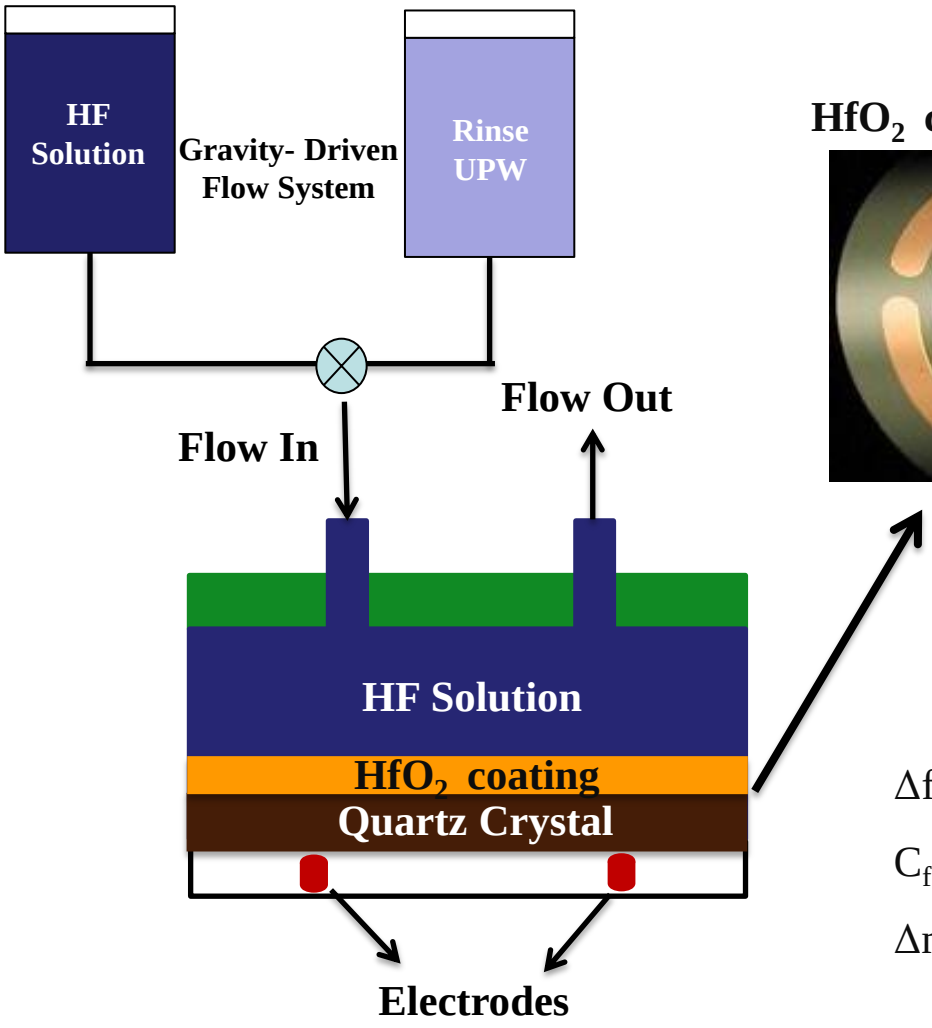
Rinsing Dynamics of Hafnium-Based High-*K* Micro and Nano Structures in Single-Wafer Cleaning Tools

Method of Approach

- **Apply the novel ECRS metrology method for in-situ and real-time monitoring of the hafnium-based high-*k* surfaces in single wafer tools.**

- **Combine metrology with process modeling to identify the controlling steps (bottlenecks) in the cleaning and rinsing of micro and nano structures for hafnium based high-*k* materials.**

Determining the Process Parameters
Experimental Set Up



HfO_2 coated Quartz Crystal

20 Å Hafnium Oxide

T=22°C

1:1000 and 1:5000 $HF:H_2O$

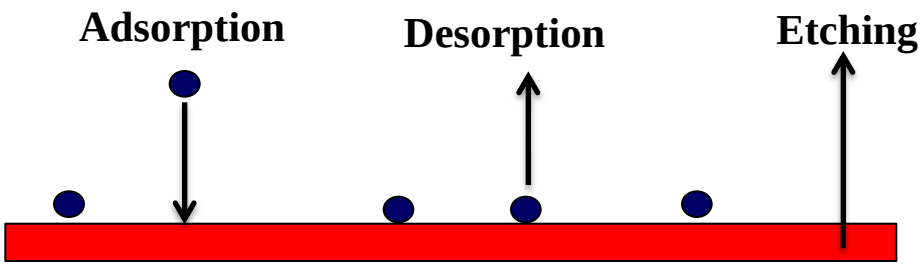
$$\Delta f = -C_f \Delta m$$

Δf = Observed frequency change in Hz,

C_f = Sensitivity factor of the crystal

Δm= Change in mass per unit area, in $\mu g/cm^2$

Process Model for HF /High-*k* Interactions



k_a: Adsorption Rate Coefficient

k_d: Desorption Rate Coefficient

k_e: Etching Rate Coefficient

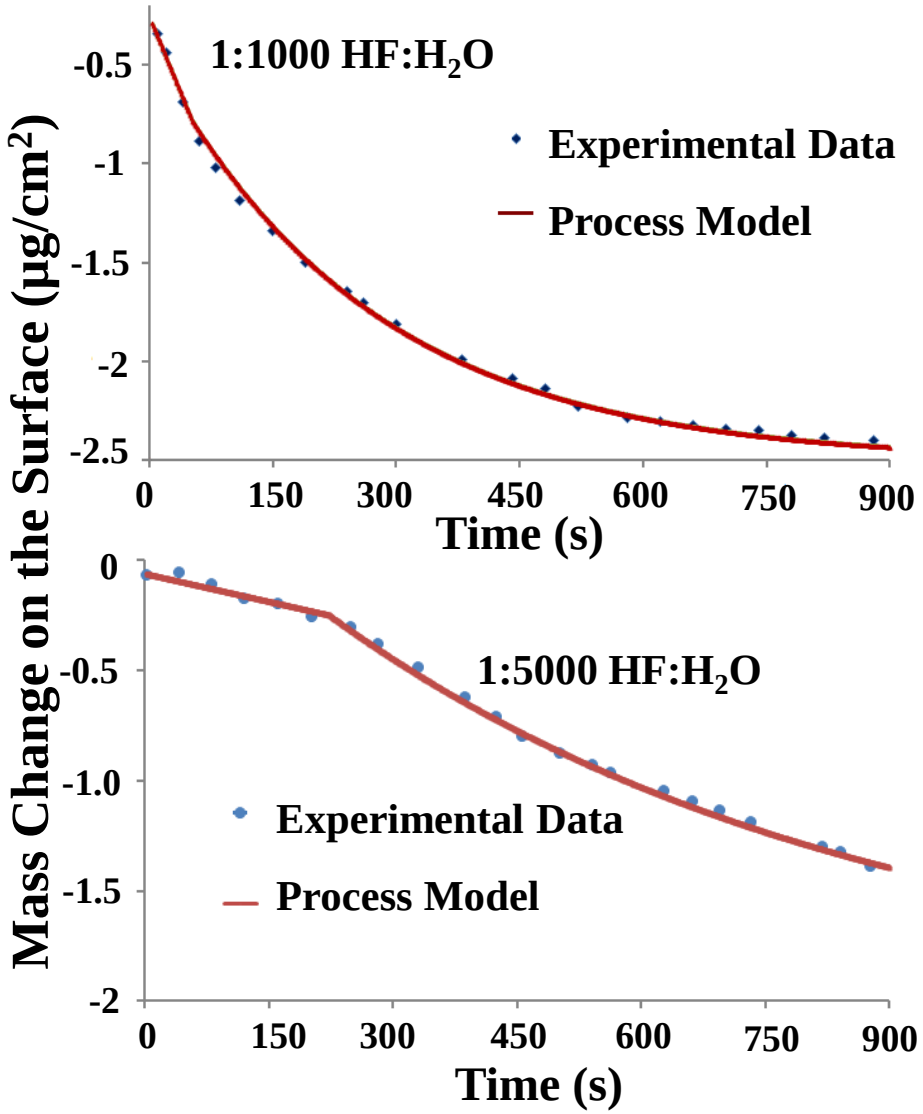
$$\frac{dC_s}{dt} = \underbrace{k_a C_b (S_0 - S_2 - C_s)}_{\text{adsorption rate of HF}} - \underbrace{k_d (C_s)}_{\text{desorption rate of HF}}$$

$$\frac{dS_2}{dt} = k_p [H^+](S_0 - S_2 - C_s) - k_e C_b S_2$$

$$\frac{1}{A}\frac{dM}{dt} = (MW_{HF})\frac{dC_s}{dt} + (MW_{H^+})\frac{dS_2}{dt} - (MW_{HfO_2})k_e C_b S_2$$

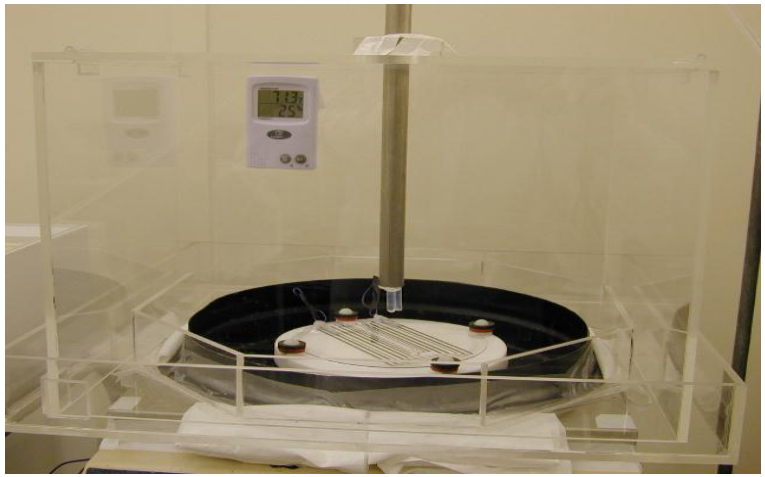
$-(MW_{HfO_2})k_e C_b S_2$ } etching rate of HfO_2

Analysis of the Experimental Data

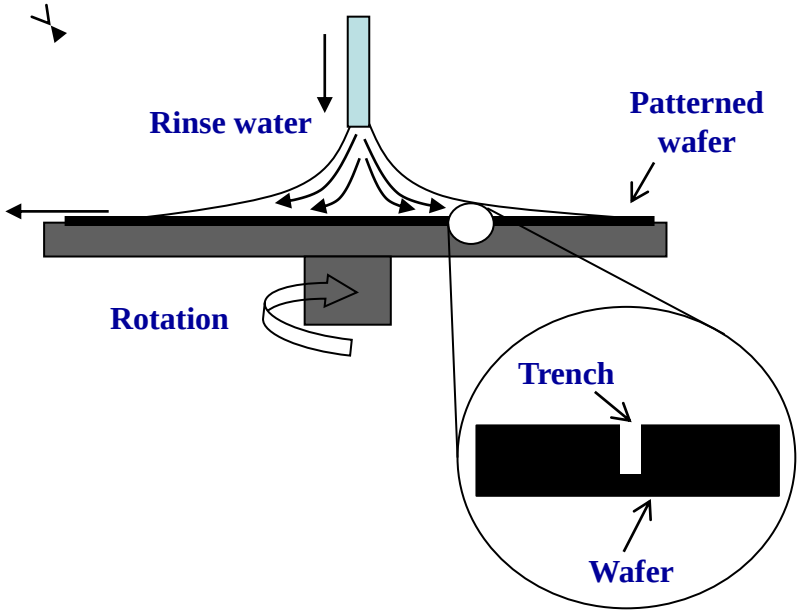


- **Adsorption Rate Coefficient: 1000 (lit/mol.s)**
- **Desorption Rate Coefficient : 0.1 (1/s)**
- **Etching Rate Coefficient : 1200 (lit/mol.s)**

Testbed for Single-Wafer Spin Rinsing and Drying

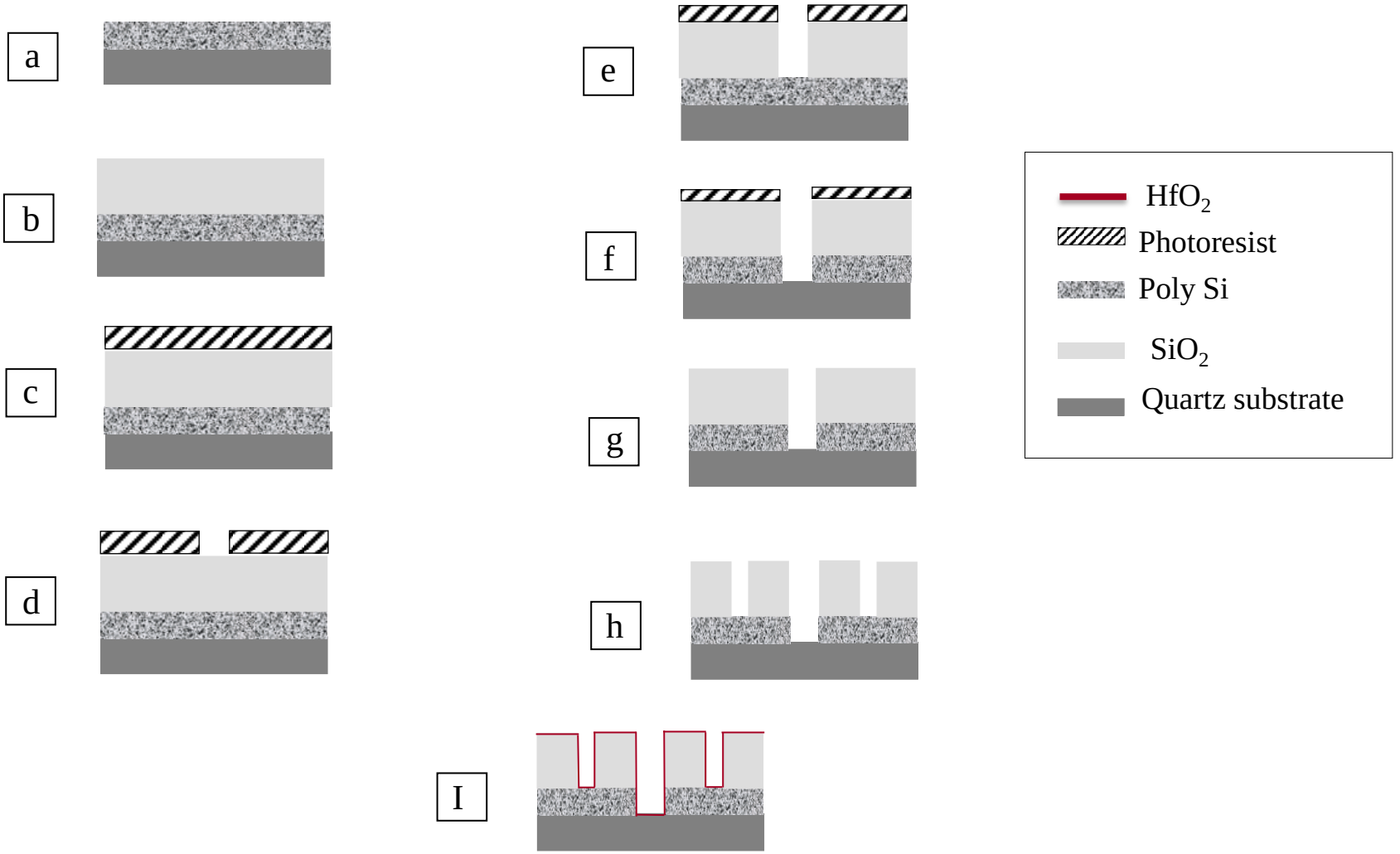


Spin Rinse Testbed



- A single wafer tool equipped with ECRS is designed and set up.
- Combination of experiments and process model is used to study the effect of various process parameters.

Fabrication of Test Wafer and In-Situ Sensor (ECRS)



Process Simulator for Single-Wafer Spin Rinsing of Patterned Wafers

Multi-component species transport equations :

$$\frac{\partial C_i}{\partial t} = \nabla \cdot (D_i \nabla C_i + z_i F \mu_i C_i \nabla \varphi) - u \nabla C_i$$

Surface adsorption and desorption:

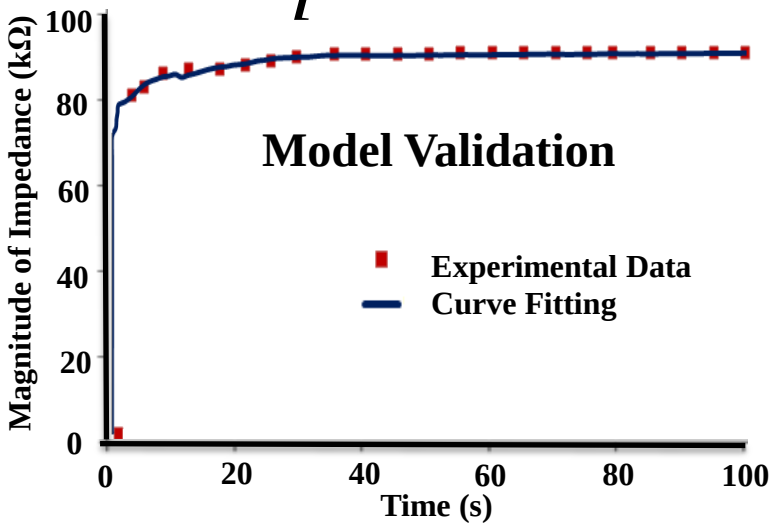
$$\frac{dC_s}{dt} = k_a C_b (S_0 - C_s) - k_d C_s$$

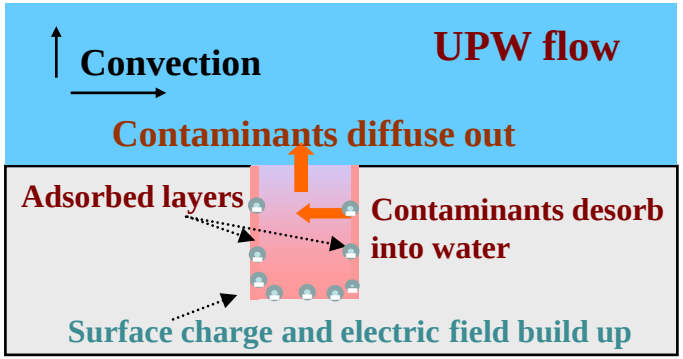
Poisson equation: $\nabla^2 \varphi = -\frac{\rho}{\varepsilon}$

where charge density: $\rho = F \sum_i z_i C_i$

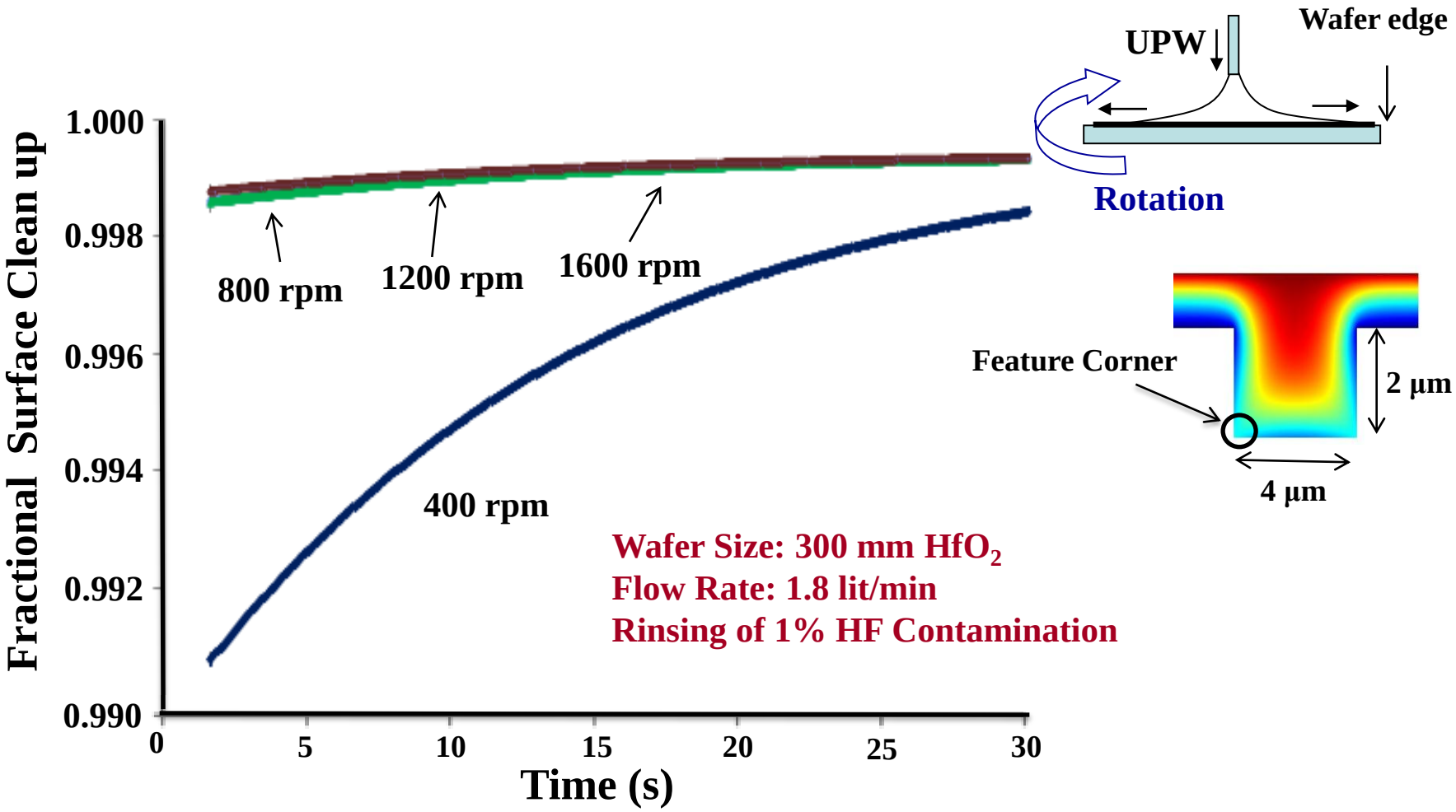
Ohm's law: $j = \sigma \vec{E} \quad \nabla \times \vec{E} = 0$

where electrical conductivity: $\sigma = \sum \lambda_i C_i$



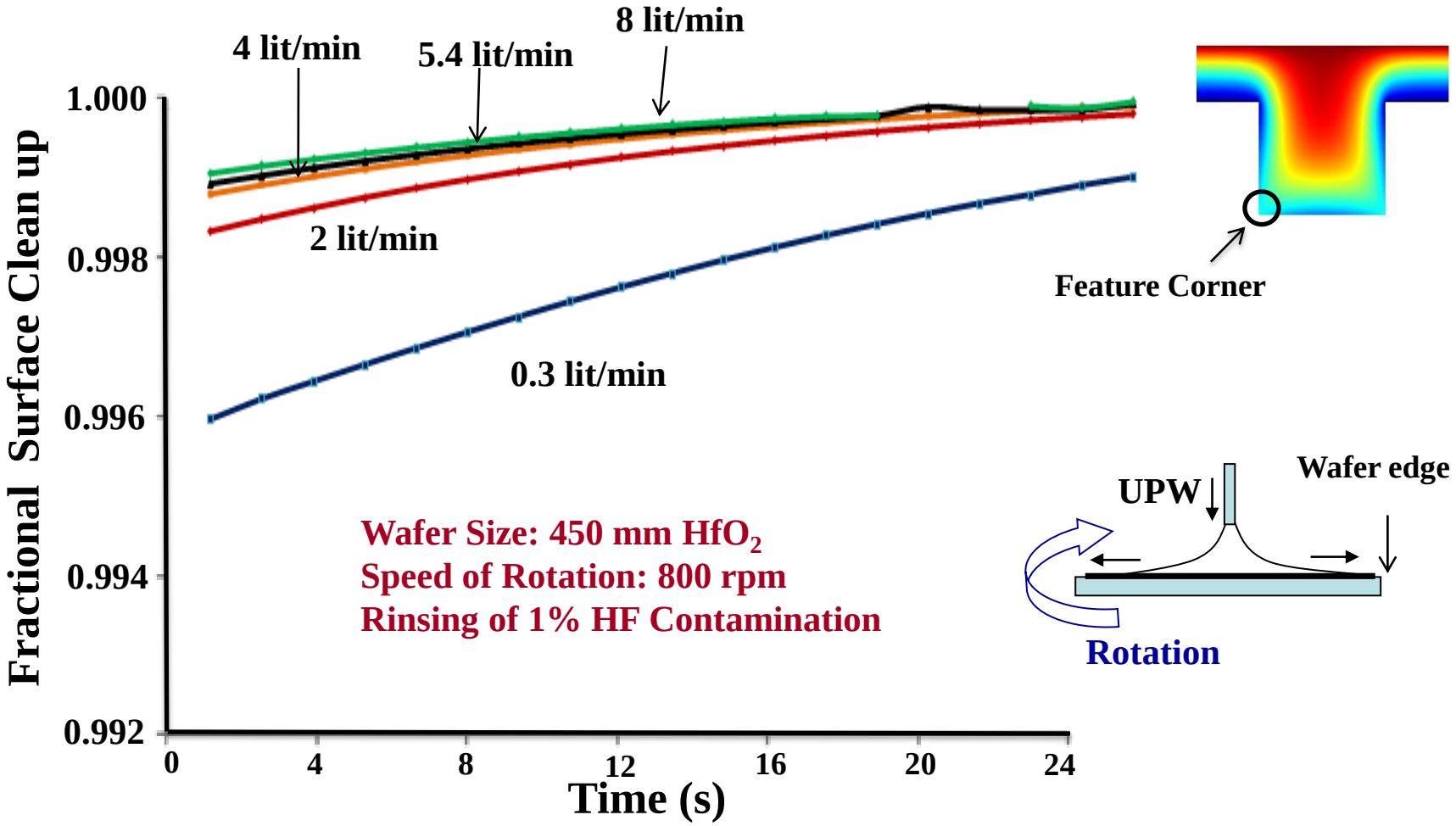


Effect of Rotation Speed in Single-Wafer Tools



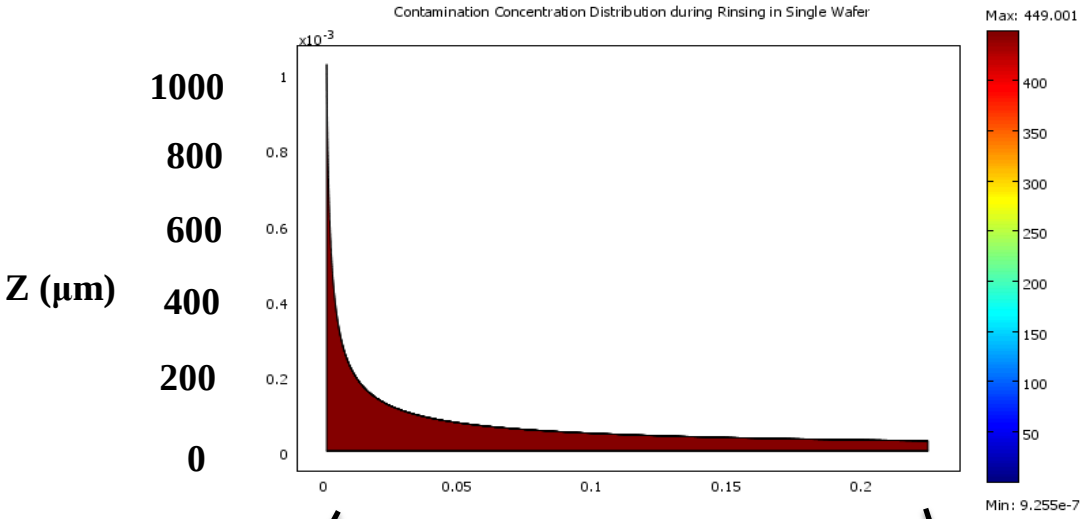
The results indicate an increase in rinsing efficiency as the spin rate increases. However, increasing the spin rate beyond 800 rpm has no further impact on the rinse efficiency.

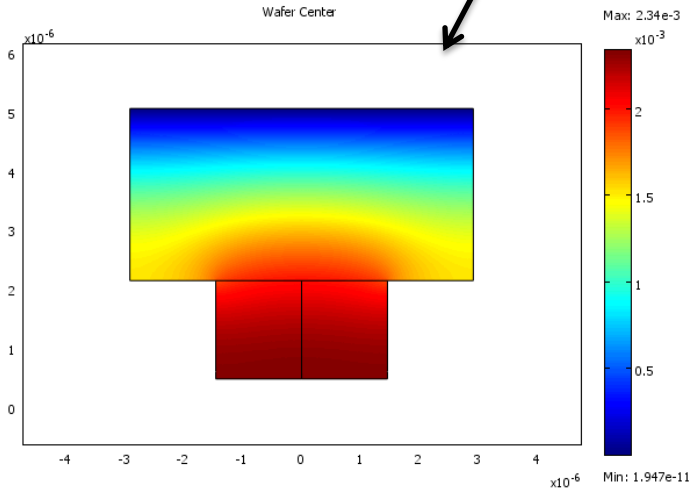
Effect of Flow Rate in Single-Wafer Tools

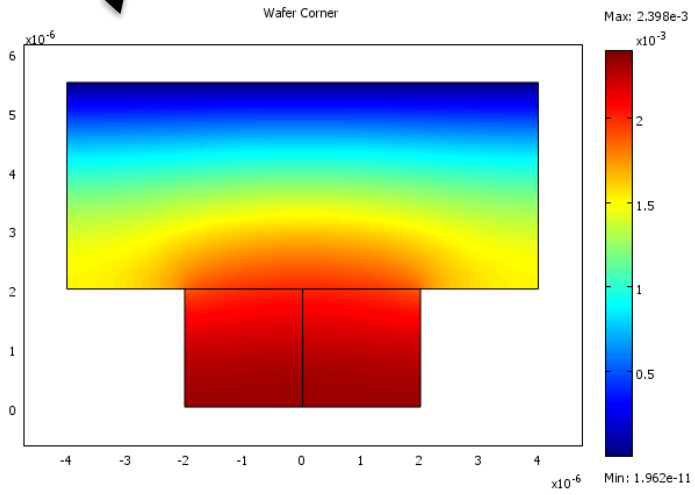


The results indicate an increase in rinsing efficiency as the flow rate increases. Increasing the flow rate beyond 4 lit/min has lower impact on the rinse efficiency.

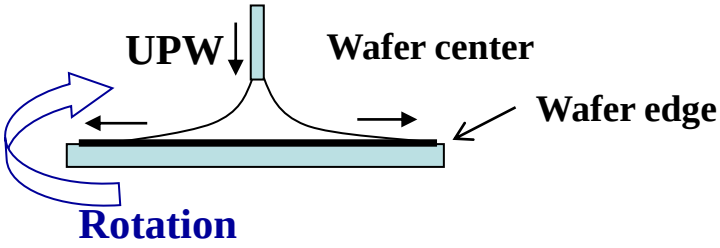
Residue Concentration Distribution During Rinsing

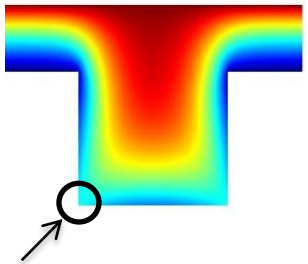


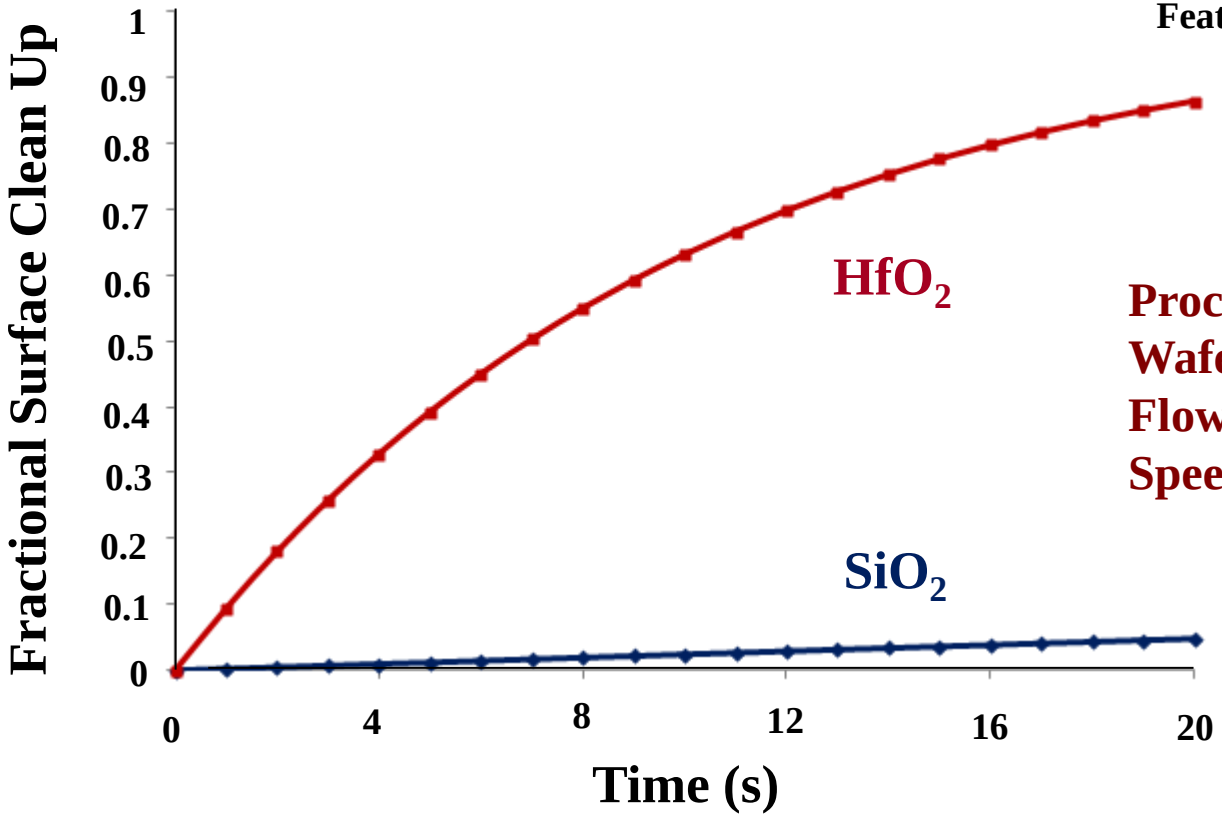




HfO_2 and SiO_2 Surface Cleaning Comparison







Process Simulation Results
Wafer Size: 450 mm
Flow Rate: 2 lit/min
Speed of Rotation: 800 rpm

Summary and Conclusions

- **An experimental method was developed to determine the fundamental mechanism and process parameters in rinsing and cleaning of high-*k* materials and nano-structures.**
- **The effects of key process parameters, including the speed of rotation, flow rate, and wafer size were investigated.**
- **A comprehensive rinse process simulator was developed and tested. The simulator can be used to optimize and lower water and energy usage.**

Industrial Interactions and Technology Transfer

- **Interactions with ASM (Eric Shero and Eric Liu) for preparation of high-*k* wafers**
- **Interactions with Freescale and Environmental Metrology Corp (EMC) for testing of new low-water rinse recipes**
- **Interactions with Sematech (Joel Barnett) for high-*k* etching and development of the cleaning/rinsing recipe/process**
- **Technical interactions with Kedar Dhane and Jun Yan on application of the rinse model and metrology techniques.**

Publications and Presentations

•Zamani, D., Mahdavi, O., McBride, M., Dhane, K, Shadman, F., "Cleaning and Rinsing of Hafnium based High-K Micro and Nano Structures in Single-Wafer Cleaning Tools" ready to submit to AIChE Journal.

•Zamani, D., Keswani, M., Mahdavi, O., Yan, J., Raghavan, S., Shadman, F., "Dynamics of Interactions between HF and Hafnium Oxide during Surface Preparation of High-K Dielectrics" in press at IEEE Transactions and Semiconductor Manufacturing.

•Zamani, D., Keswani, M., Yan, J., Raghavan, S., Shadman, F., "Determining the Fundamental Kinetic Parameters for Rinsing and Cleaning of Hafnium-Based High-k Materials" ECS Transactions, 41 (5) 45-50 (2011).

•Zamani, D., Yan, J., Mahdavi, O., Zhang, X., Vermeire, B., Shadman, F., "Application of Novel On-Line Metrology Technique to Reduce Water and Energy Usage during Surface Preparation of Patterned Wafers in Single – Wafer Tools" Invited Paper for SRC-TECHCON, Presentation –Poster, September 2011.

•Zamani, D., Yan, J., Keswani, M., Mahdavi, O., Raghavan, S., Shadman, F., "Environmentally Friendly Chemicals for Patterning of Hafnium Based High-K Materials and Rinsing in Single-Wafer Cleaning Tools" SRC-TECHCON, Presentation-Poster, September 2011.

•Zamani, D., Thareja, G., Yan, J., Keswani, M., Mahdavi, O., Dhane, K., Nishi, Y., Raghavan, S., Vermeire, B., Shadman, F., "Lowering the Environmental Impact of High-k and Metal Gate-Stack Surface Preparation Processes" Annual Site Review, SRC/Sematech Engineering Research Center for Environmentally Benign Semiconductor Manufacturing , Presentation –Poster, March 2011.

•Dhane, K., Han, J., Yan, J., Mahdavi, O., Zamani, D., Vermeire, B., Shadman, F., "Dynamics of Cleaning and Rinsing of Micro and Nano Structures in Single – Wafer Cleaning Tools" IEEE Transactions and Semiconductor Manufacturing, Vol. 24, NO. 1, February 2011.