NSF/SRC Engineering Research Center for
Environmentally Benign Semiconductor Manufacturing

Program Overview

February 23, 2006

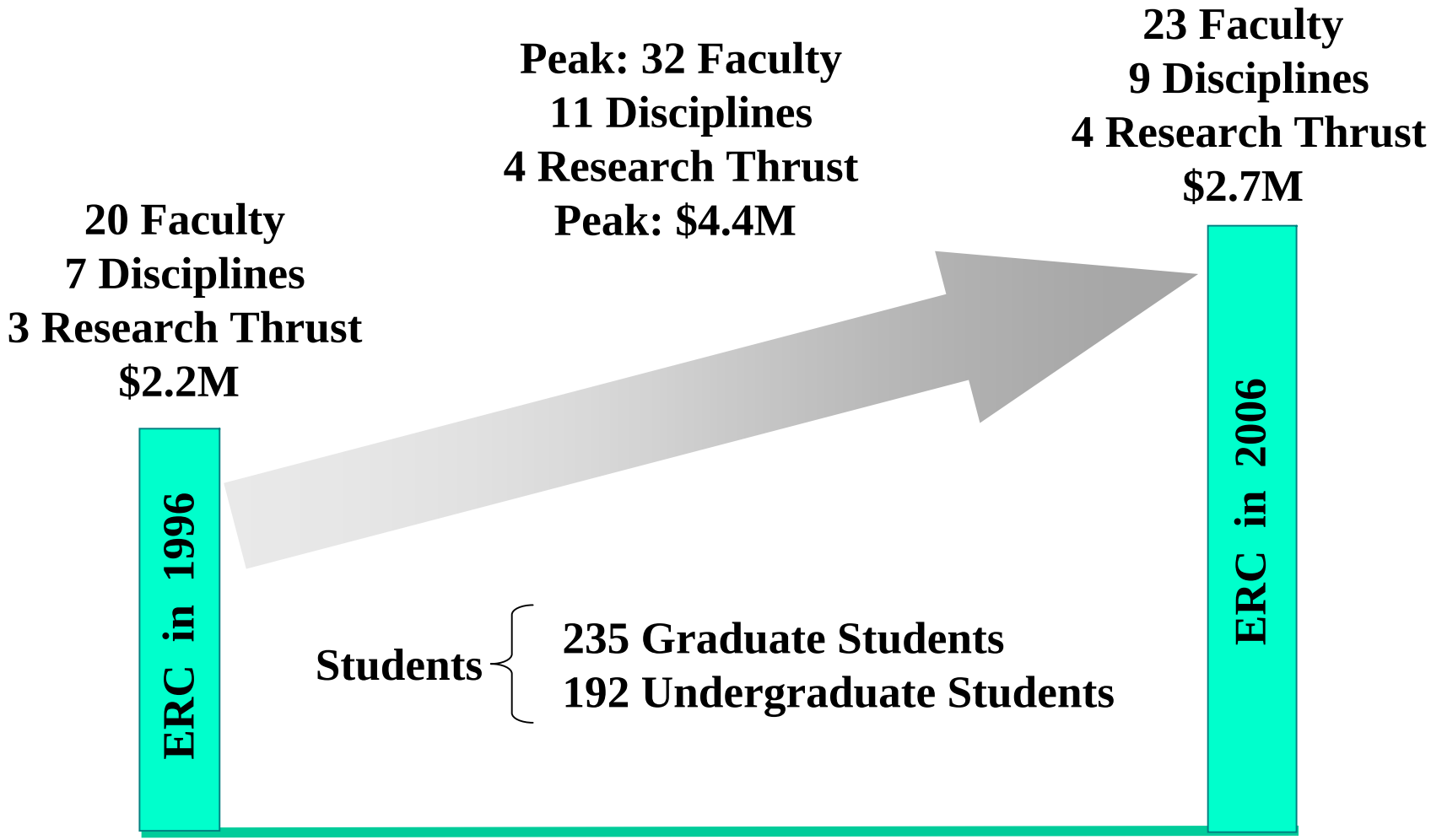
Participating Institutions

- University of Arizona
- MIT
- Stanford University
- UC Berkeley

} Founders 1996

- Cornell University (1998 -)
- Lincoln Laboratory (1998 -)
- Arizona State University (1998 - 2003)
- University of Maryland (1999-2003)
- Purdue University (2003 -)
- Tufts University (2005 -)
- Columbia University (new; starting April 2006)

Statistics on the Growth of the ERC



Program Organization

Thrust A
BEOL Processes

- Environmentally Benign Etching of BEOL Dielectrics
- Solventless Low-k Dielectric
- Novel Barrier Film Deposition Methods
- CMP Waste Minimization
- Environmentally Benign Planarization

Thrust B
FEOL Processes

- Novel Surface Cleaning and Passivation
- Selective Deposition for Gate Stack Manufacturing
- Etching of New High-k and Electrode Materials

Thrust C
Factory Integration

- Low-Energy Water Purification and Wastewater Treatment
- Efficient Wafer Rinsing and Cleaning
- Water Recycle and Reuse
- Integrated ESH Impact Assessment

Thrust D
Patterning

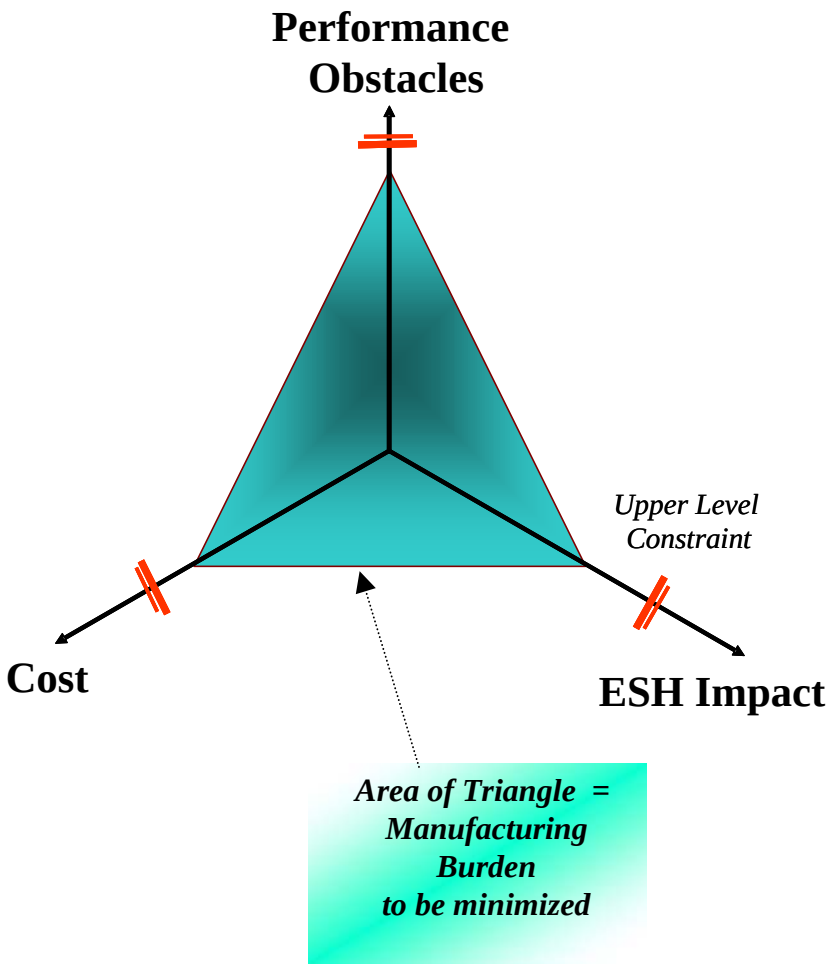
- Solventless Lithography
- Additive Processing

Education

- ESH Concepts in Science/Engineering Curricula
- Continuing Education and Short Courses
- Outreach

ERC Mission and Objectives

1. **Research to develop science and technology leading to simultaneous *performance improvement*, *cost reduction*, *and ESH gain***
2. **Incorporating ESH principles in engineering and science education**
3. **Promoting *Design for Environment and Sustainability as a Technology Driver* and not a burden**



Design for Environment and Sustainability is a Technology Driver

Examples of ERC

Strategies, Project, and Highlights

Design for Environment and Sustainability is a Technology Driver

Strategy 1: Low ESH-Impact through Alternate Chemistries

Alternate Chemistries and Processes for Etching

Reif (MIT), Graves (UCB)

Focus on identifying potential alternative chemistries (1995 – 1996)

PECVD chamber clean experiments (NF_3 and C_4F_8O) (1996 – 1998)

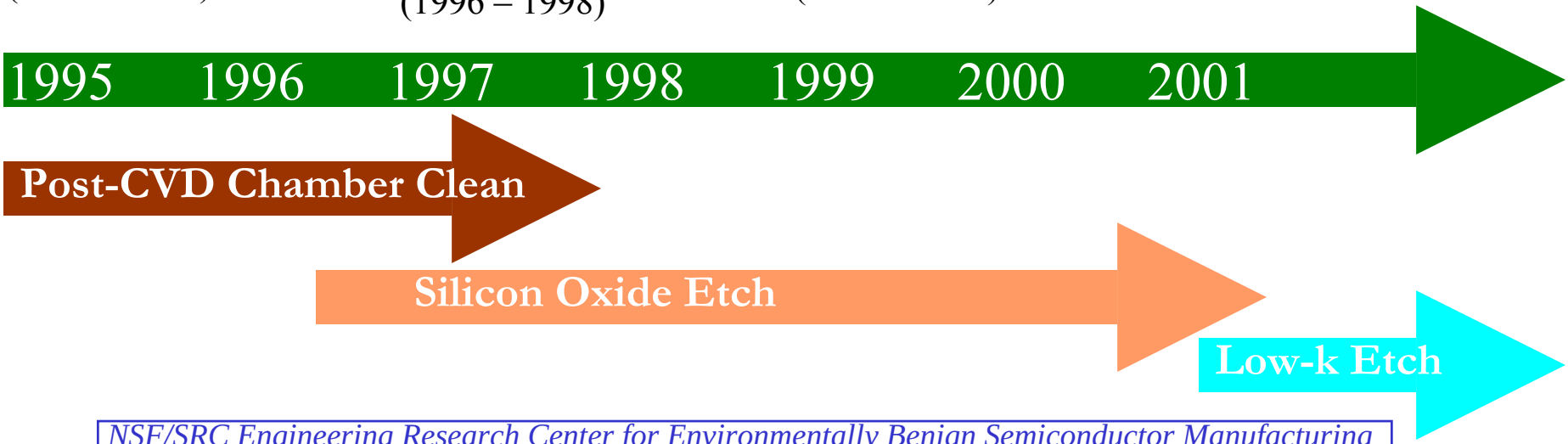
Drop-in dielectric etch replacements (hydrofluorocarbons) (1996 – 1998)

More exotic dielectric etch replacements (iodofluorocarbons) (1997 – 1999)

Decouple C and F (NF_3/hydrocarbon) (1999 – 2001)

Unsaturated molecules for dielectric etch (UFC) (1999 – present)

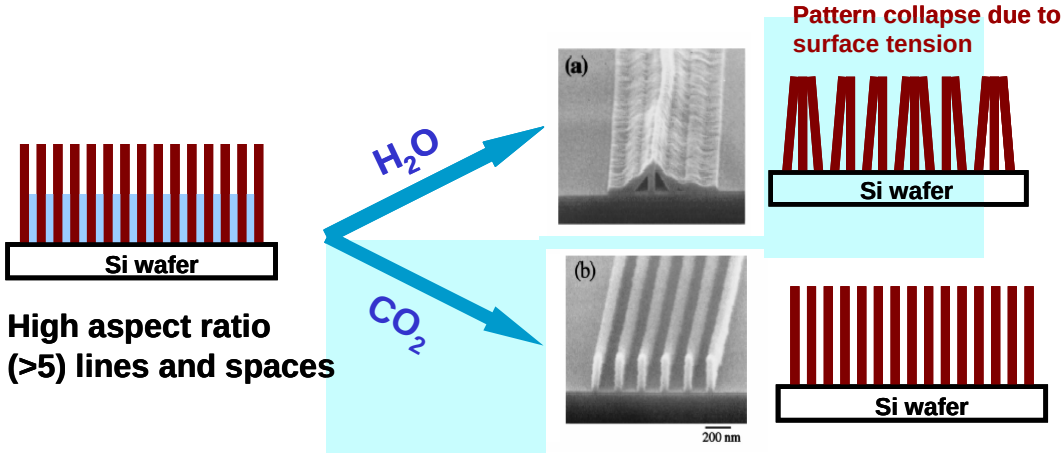
Apply etch process and emissions knowledge to future generation processes (Deep-submicron – low-k and ultra low-k) (2001 – present)



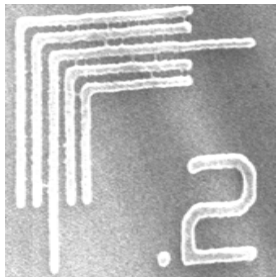
Applications of Supercritical Carbon Dioxide

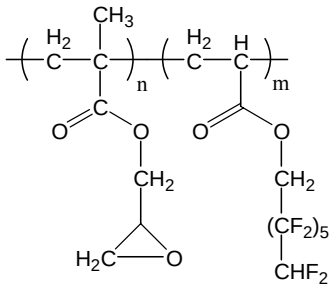
Ober (Cornell), Muscat (UA)

1. Cleaning of submicron features



2. Novel photoresist chemistries and photo-imageable dielectrics



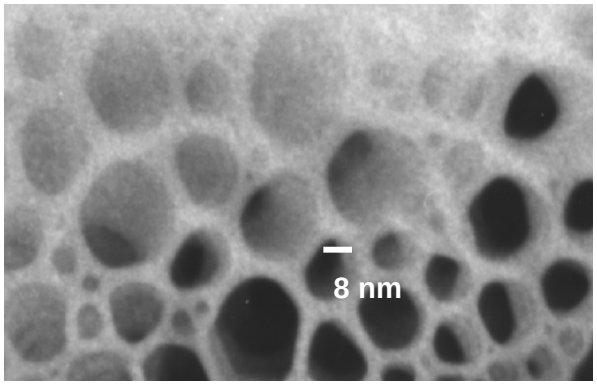


ESH Driver → **Major performance gain**

Air for Low-k: ESH Gain and Performance Gain

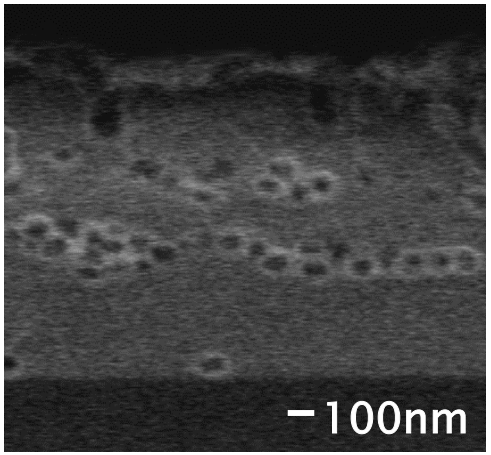
Gleason (MIT)

	% porosity	
	κ = 2	κ = 1.5
silicon dioxide	55 – 65	75 – 85
hydrocarbon polymer	40 – 50	64 – 75
fluorocarbon polymer	0	40-50

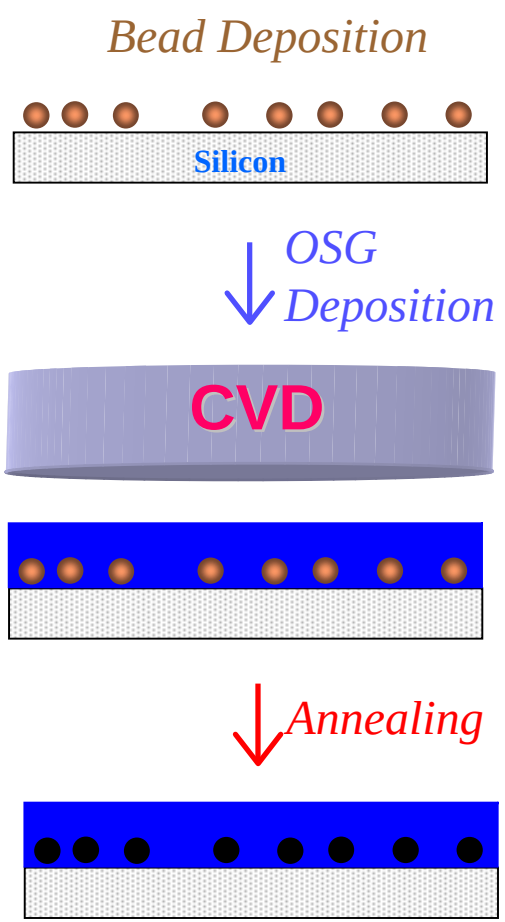


Dielectric Constant = 1.4
Refractive Index = 1.067

Wu, Ross, Gleason; Plasma Proc. Poly. 2, 401 (2005).



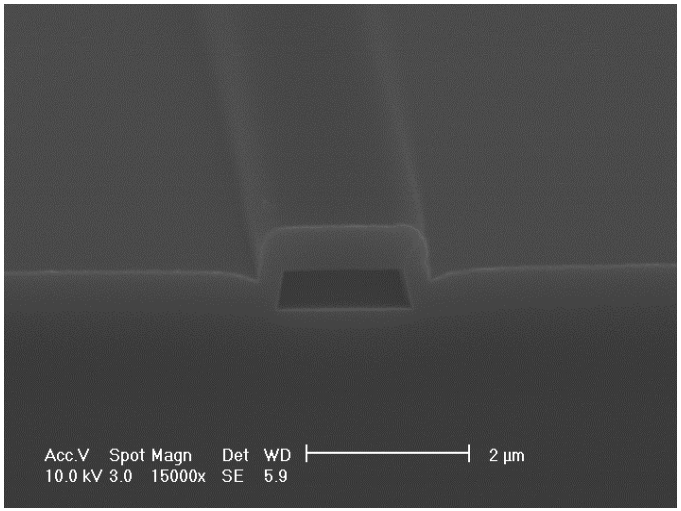
Alternating Bead/OSG Deposition: Controls Degree of Porosity



Air for Low-k: ESH Gain and Performance Gain

Gleason (MIT)

Ultimate Dielectric
Air Gap by CVD Process



- All dry
- Simplified process
- No hardmask
- RIE resist strip
- With better lithography, smaller feature sizes can be fabricated.

$\varepsilon_{(FC)} = 1.73$

$\varepsilon_{Air} = 1.00$

$\varepsilon\varepsilon_{eff} \sim 1.30 – 1.35$

Low-k dense material
+
Porosity
+
Air gap
=
Aggressive low-k approach

Chan, Gleason; J. Electrochem. Soc. (in press)

Design for Environment and Sustainability is a Technology Driver

Strategy 2: Integration of Process Steps

Example: Integrated Deposition and Patterning of Low-k Dielectrics

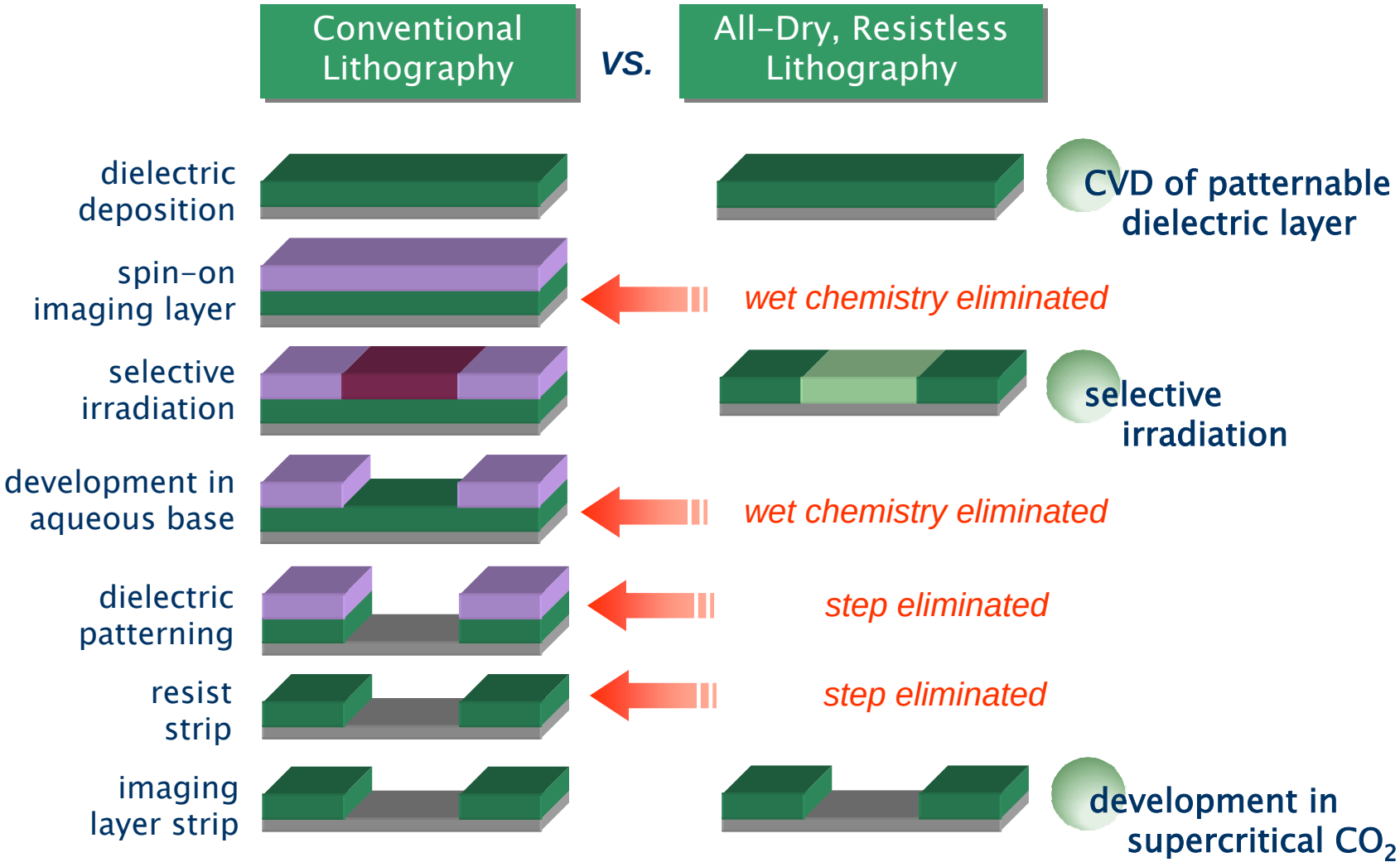
ESH Gain by Integrated Deposition and Patterning of Low-K

Gleason (MIT), Ober (Cornell)

	Conventional Lithography	ESH Issues
dielectric deposition		**Precursors, HAPs, wastes**
spin-on imaging layer		**VOCs, waste**
selective irradiation		**VOCs, radiation**
development in aqueous base		**VOCs, HAPs**
dielectric patterning		**HAPs, PFCs**
resist strip		**A/B chemicals, solvents**
imaging layer strip		**A/B chemicals, UPW**

ESH Gain by Integrated Deposition and Patterning of Low-K

Gleason (MIT), Ober (Cornell)



ESH Gain by Integrated Deposition and Patterning of Low-K

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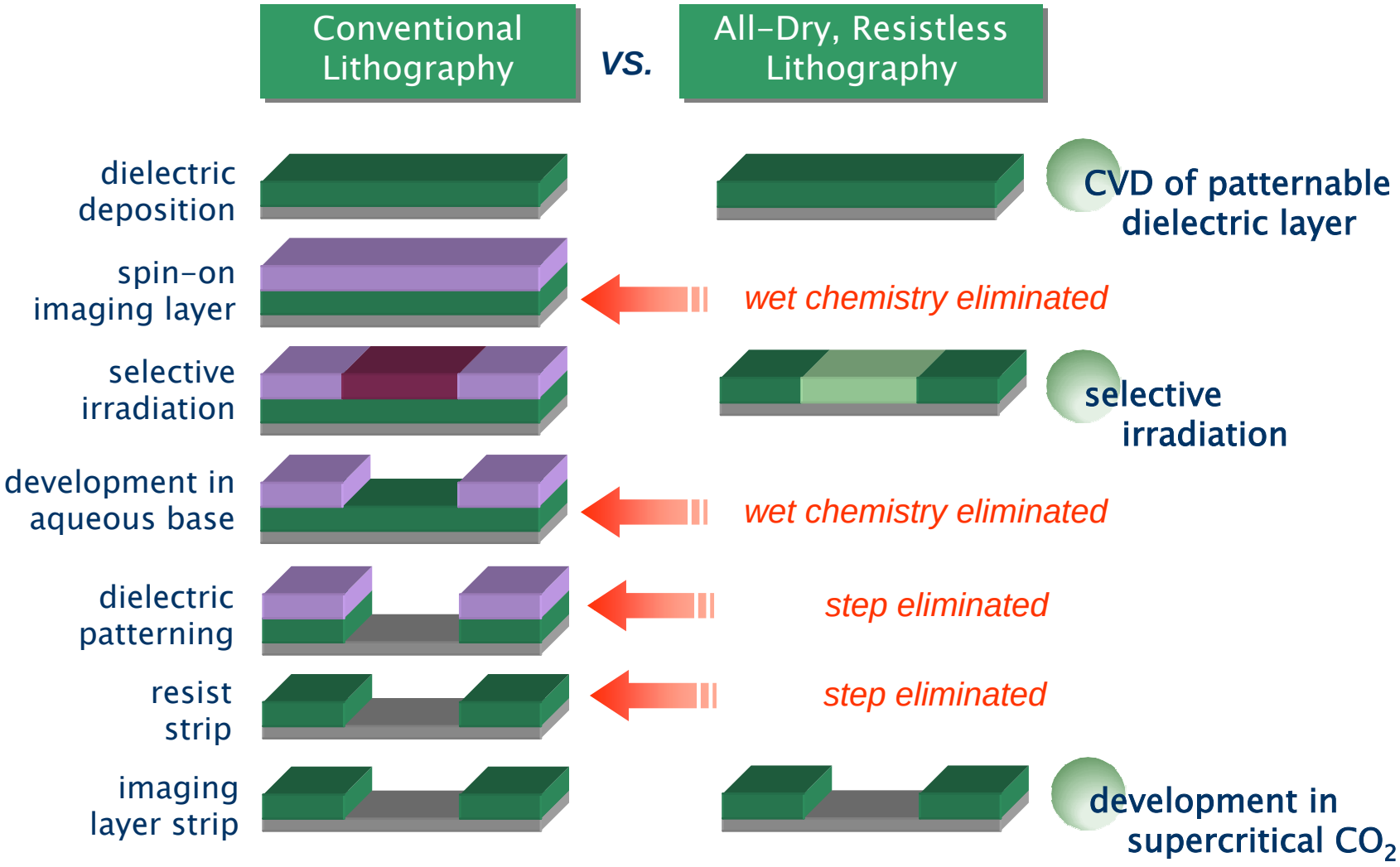
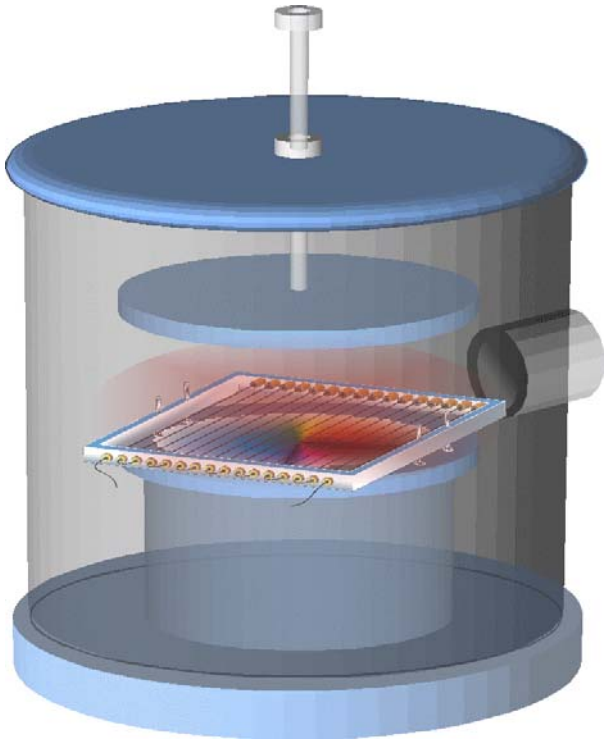
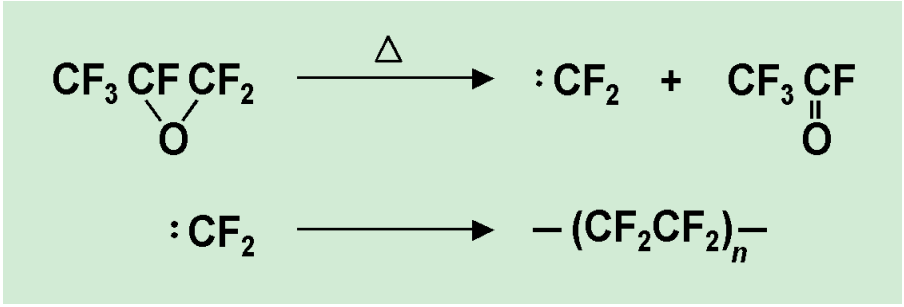


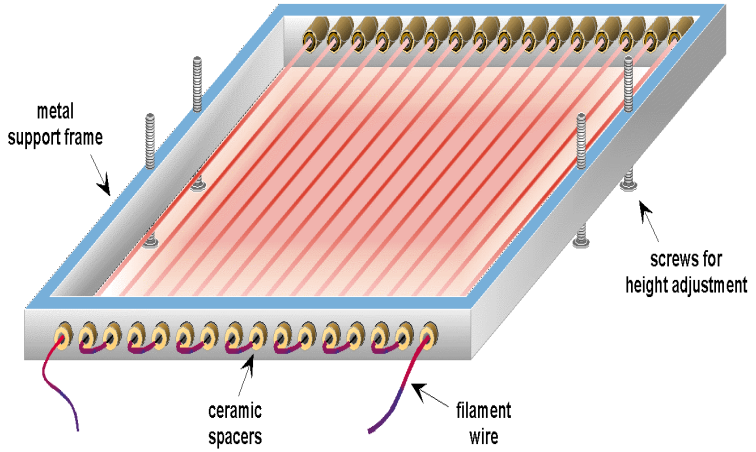
Solventless Deposition of Low-k Dielectrics

Gleason (MIT)



Pyrolytic CVD

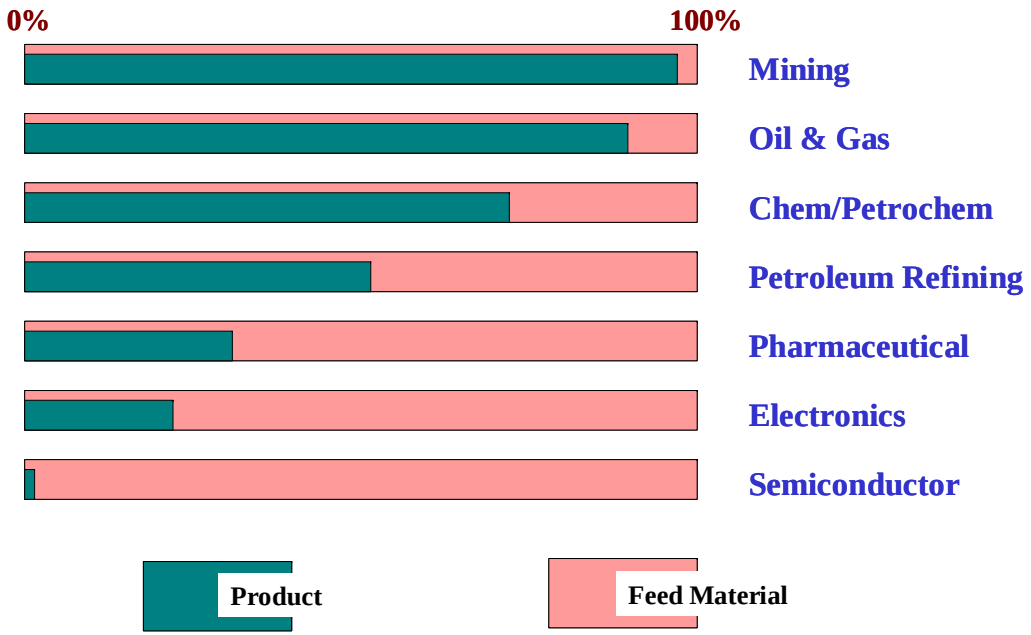




Design for Environment and Sustainability is a Technology Driver

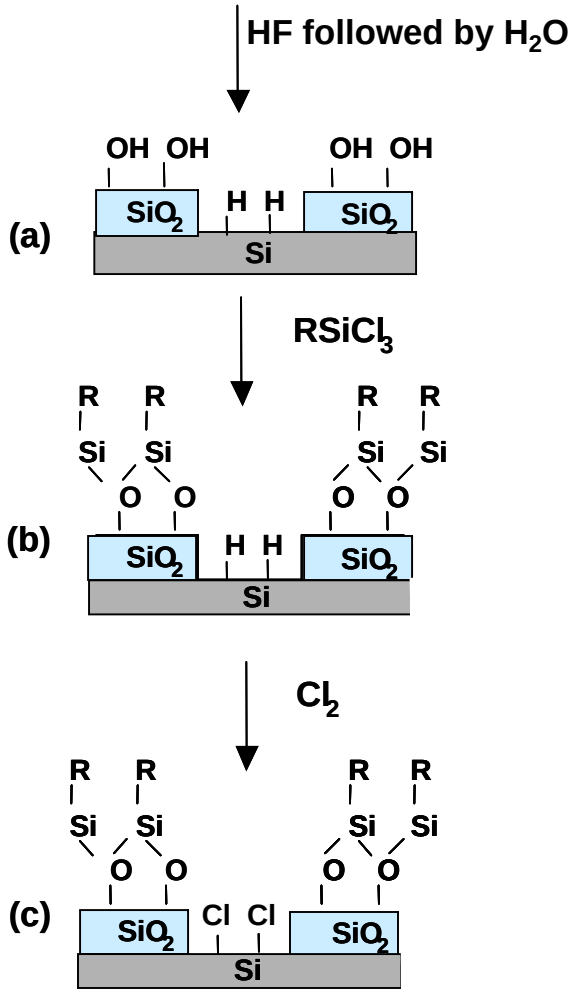
Strategy 3: Replace Subtractive Processing with Additive Processing

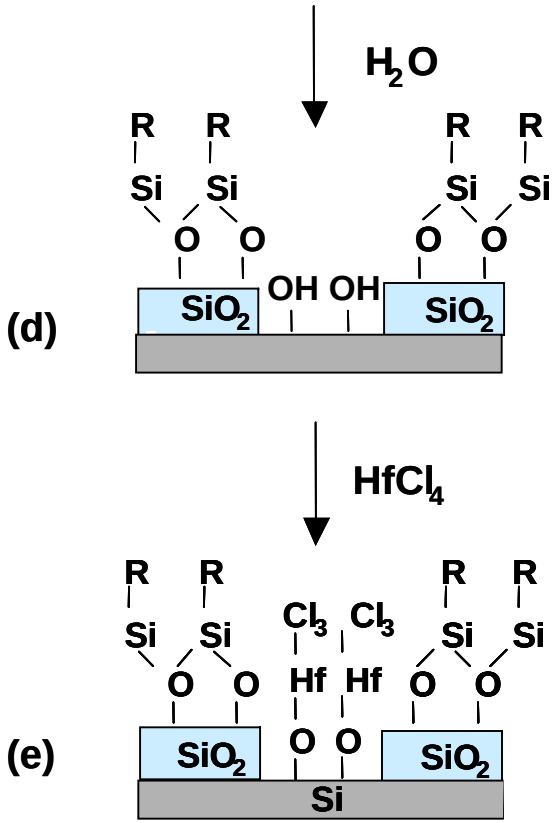
- **Current semiconductor manufacturing process sequence is primarily *subtractive***
- **ESH goal: Innovations which make the manufacturing sequence primarily *additive***



Additive Process for High-k Gate-Stack Fabrication

Bent, Chidsey, McIntyre, Saraswat (Stanford), Muscat (UA)





a) Clean and Pattern Si

b) Protect SiO_2

c) Activate Si

d, e) Maskless selective ALD of high-k dielectric

Design for Environment and Sustainability is a Technology Driver

Strategy 4: All-Out Effort Against Major Obvious Culprits

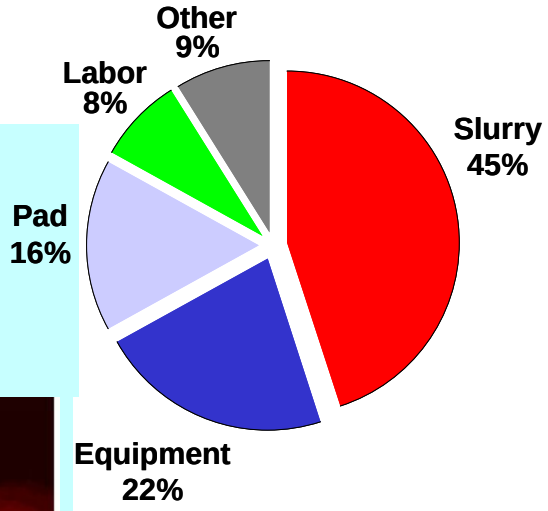
CMP: large material/energy usage, large waste, high cost

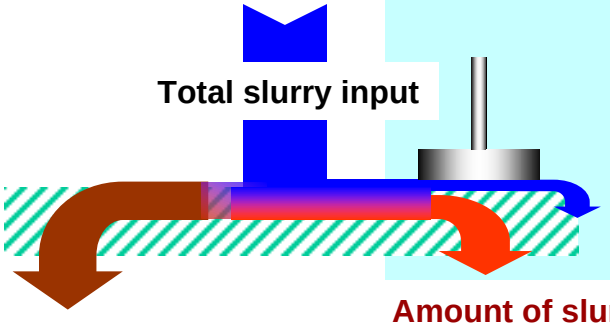
ESH Gain Through Slurry Use Minimization

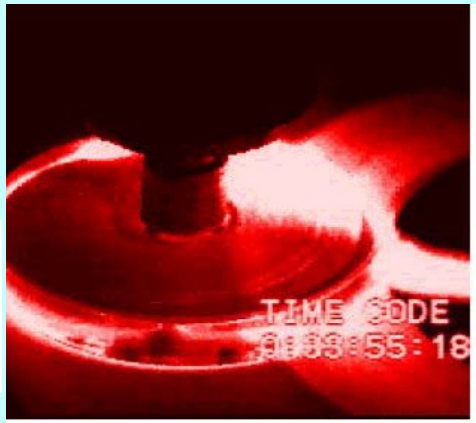
Philipossian, Raghavan (UA), Boning (MIT), Beaudoin (PU)

Slurry is the largest contributor to CMP COO.
Example: for 8000 WSPW, 200-mm factory, and five Cu layers:

- **6,000,000 liters of slurry ($20M) per year**
- **300 metric tons of solid waste per year**







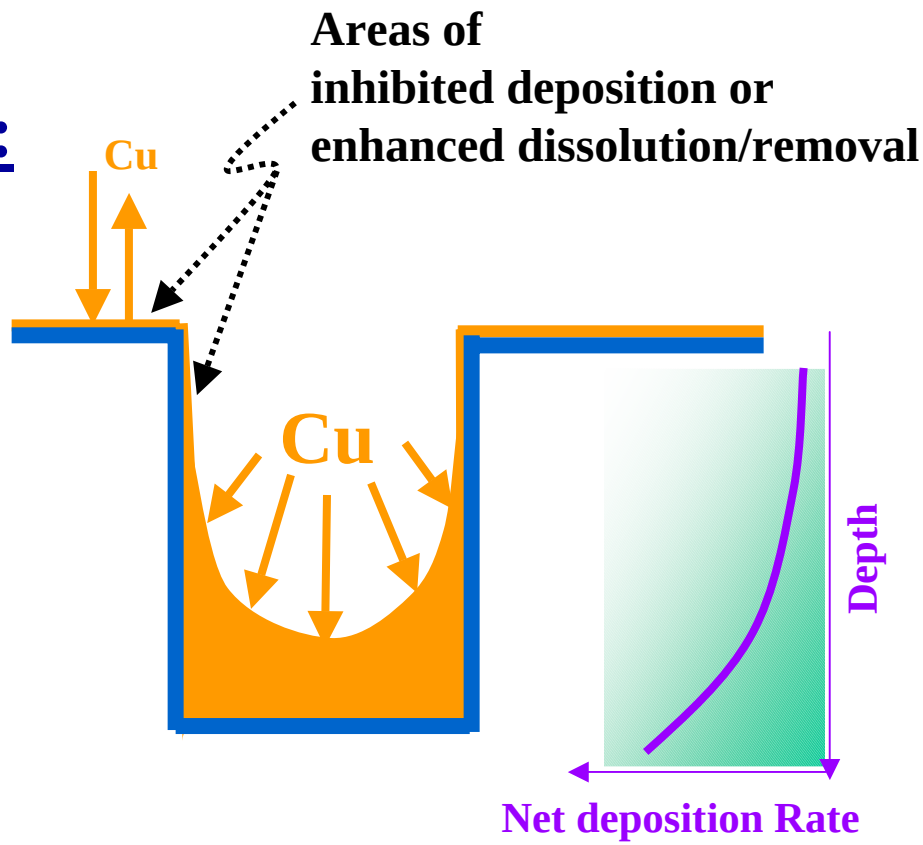
Amount of slurry that does the actual polishing is often less than 10%

ESH Gain through study of slurry/pad/wafer interactions and pattern dependency, novel pad and chemistries, process control, and alternative planarization techniques (e.g. AFP, CAP, and ECMP)

Reducing CMP and Associate Waste By Selective Deposition of Metal and Dielectrics

Site-Selective Deposition:

- Diffusion-limited inhibitors for local rate modification
- Cyclic deposition and dissolution
- Simultaneous deposition and planarization



Design for Environment and Sustainability is a Technology Driver

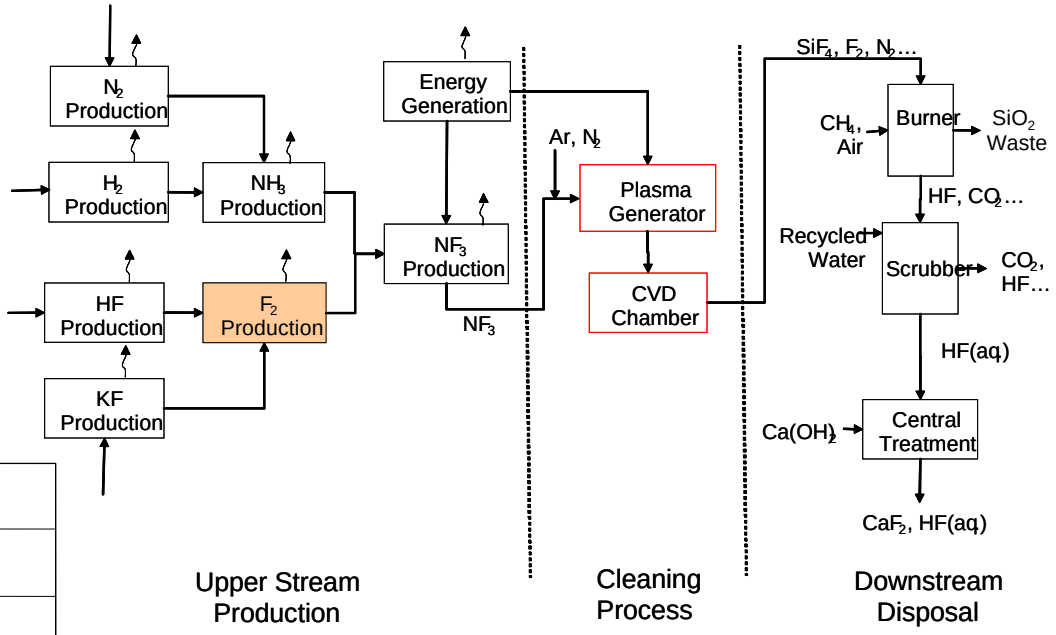
Strategy 5: ESH Impact Assessment of New Materials and Processes

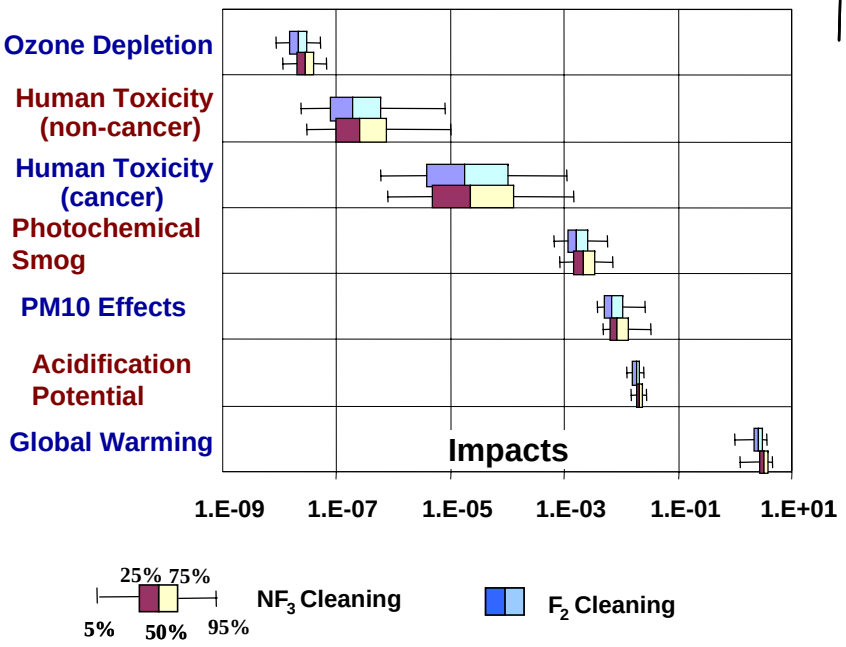
Life Cycle Analysis (LCA)
Comprehensive Impact Modeling (Performance, Cost, and ESH)

ESH Impact of New Processes and New Materials

McRae (MIT), Dornfeld (UCB), Rubloff (UM), Blowers (UA)

- **Developed a new ESH impact assessment tool**
- **Combined *LCA* with *CoO* and *performance metrics***
- **Developed method for handling uncertainties**



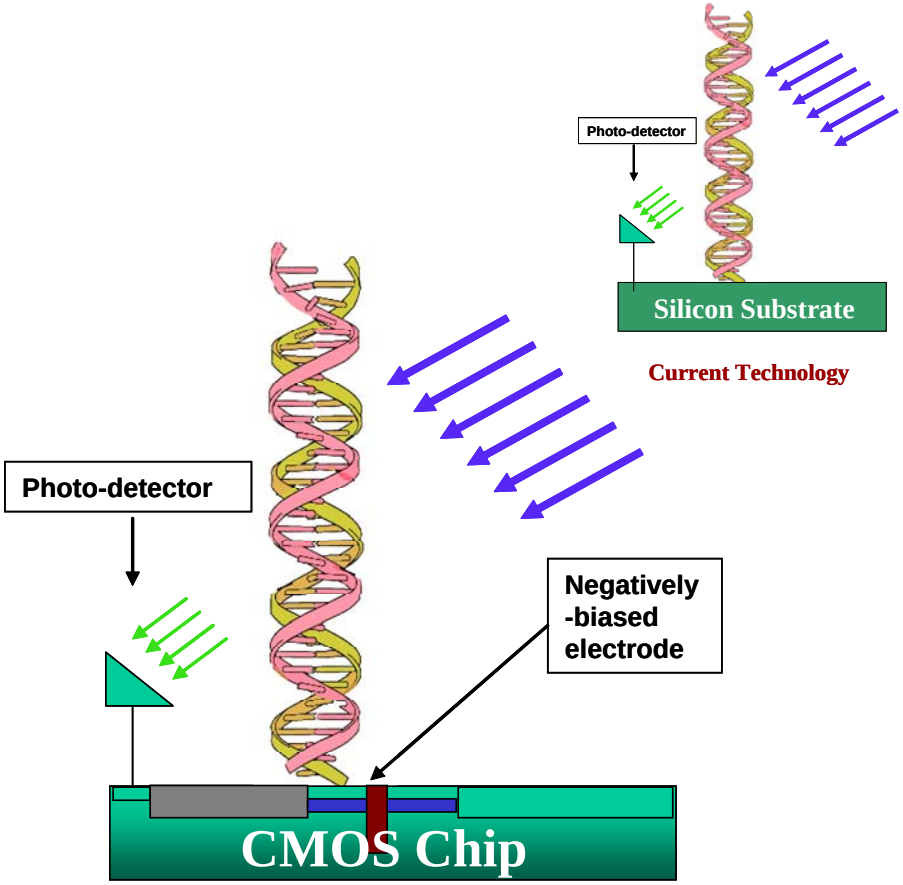


- **Needed in the early stage of research planning**
- **Cost effective**
- ***Design for Environment and Sustainability* (pro-active approach)**

Biochip for Rapid Toxicity Testing of New Chemicals

Mathine, Runyan (UA)

- Rapid assessment of chemicals and process chemistries
- Important for both chemical suppliers (starting materials) and equipment suppliers/end users (for process-generated by-products, interactions of multiple chemicals, proprietary chemistries in R/D stage, etc.)
- A first step towards an on-line ESH monitor.



Novel Technology

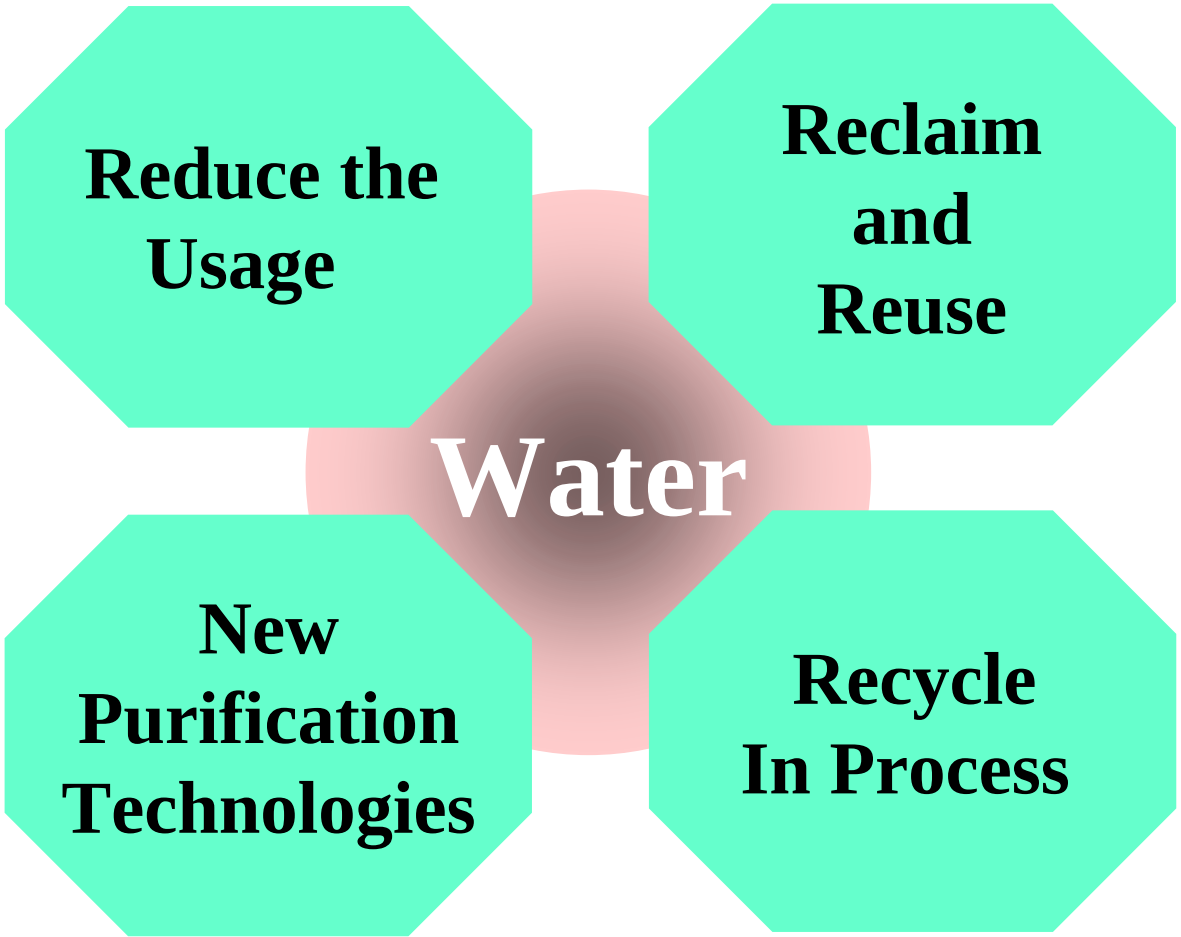
Disclosure filed for patent application

Design for Environment and Sustainability is a Technology Driver

Strategy 6: Minimize Use of Natural Resources

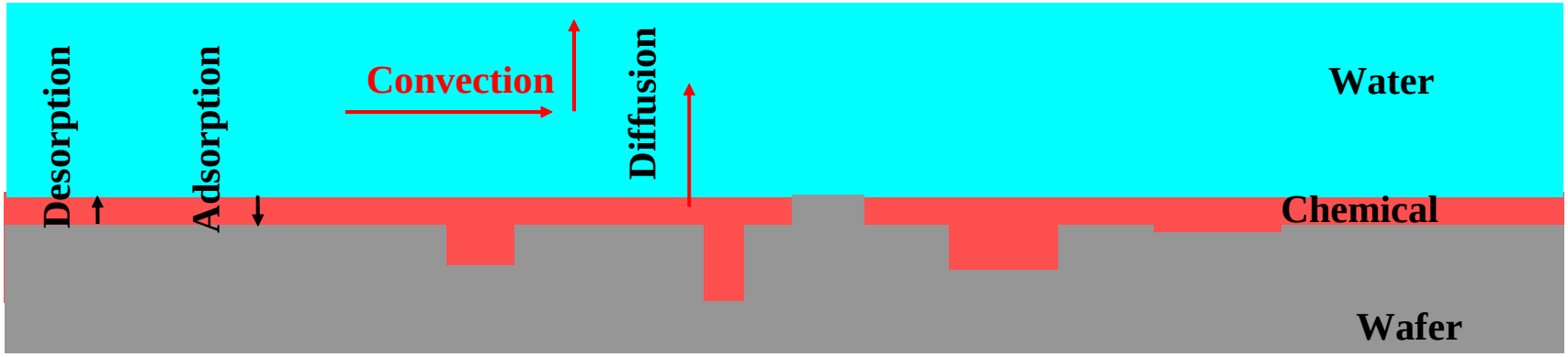
Example: Water and Energy Use Reduction

Water Sustainability Strategies



Low-Water Rinsing and Cleaning of Micro- and Nano-Features

Shadman (UA), Vermeire (ASU)

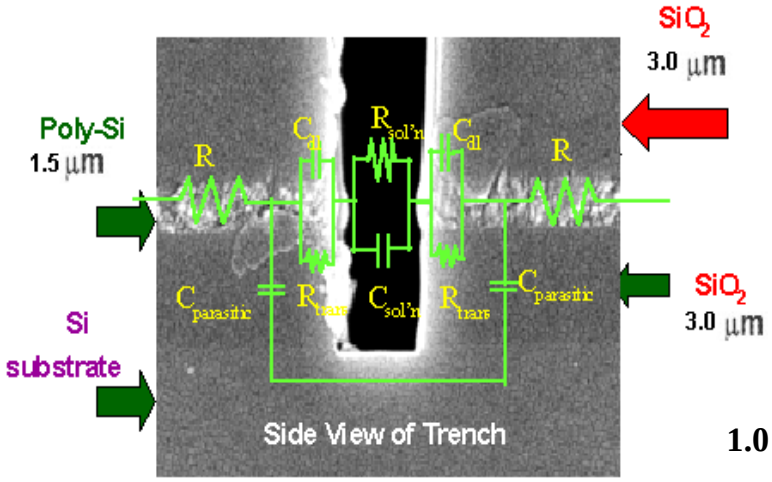


Low water rinse technology requires:

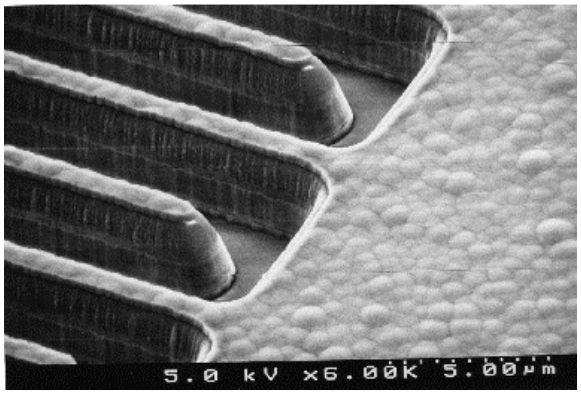
1. Metrology for real-time and on-line monitoring of surface contamination
2. Understanding the process bottleneck in the complex combination of process steps

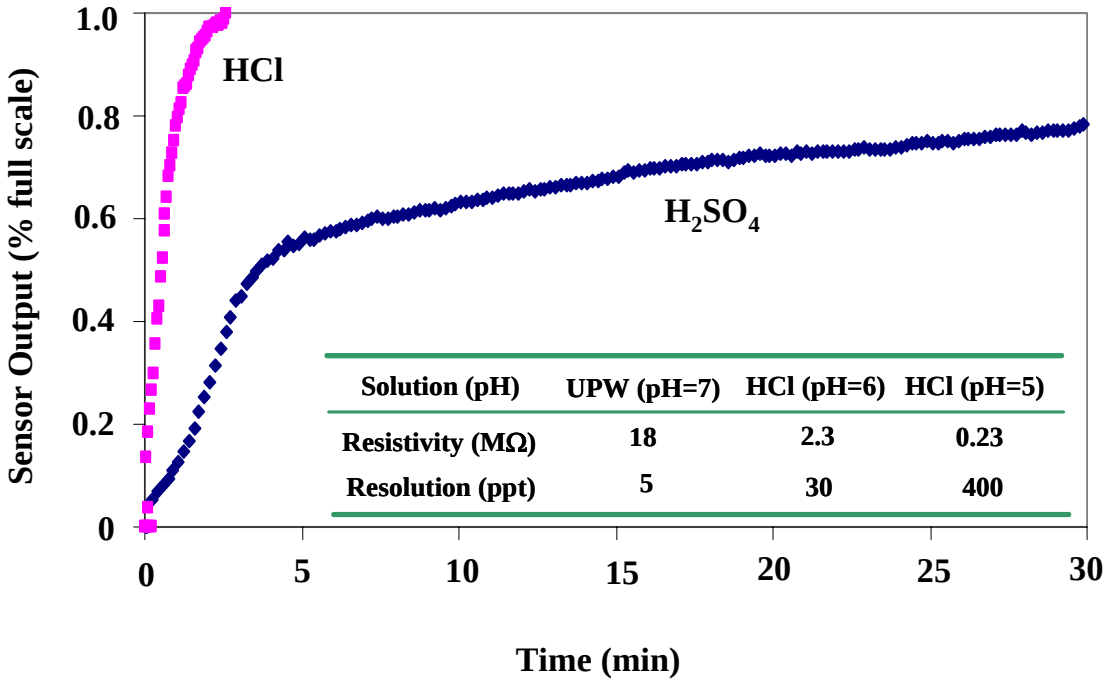
Low-Water Rinsing and Cleaning of Micro- and Nano-Features

Shadman (UA), Vermeire (ASU)



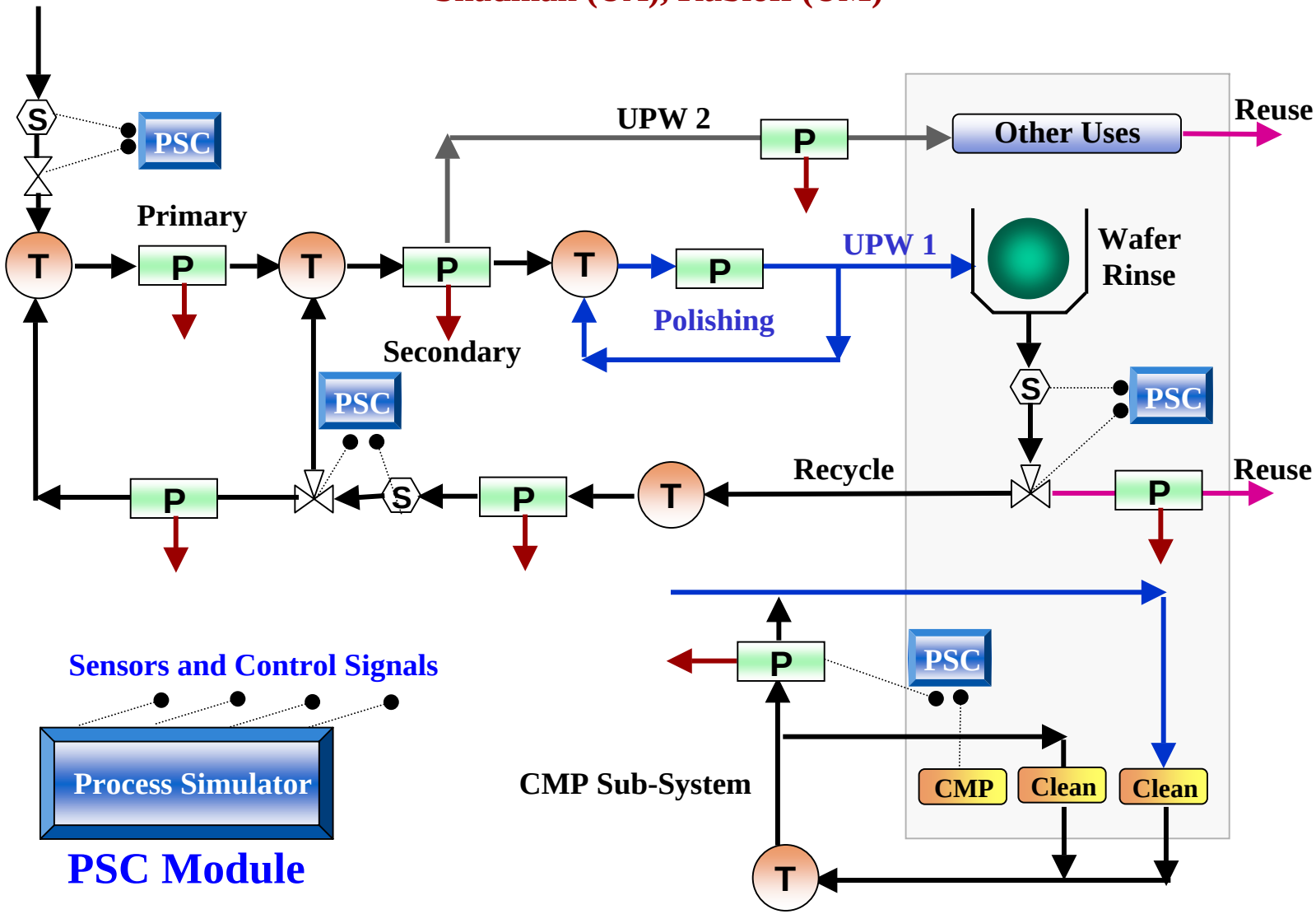
Electro-Chemical Residue Sensor (ECRS)





Water Recycling Technology

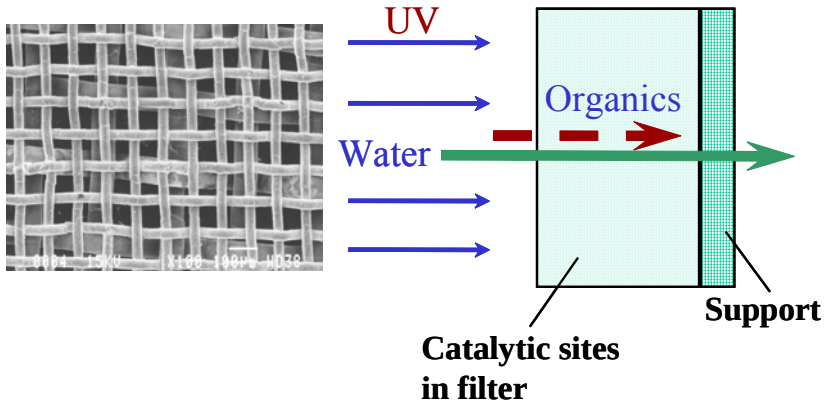
Shadman (UA), Rubloff (UM)



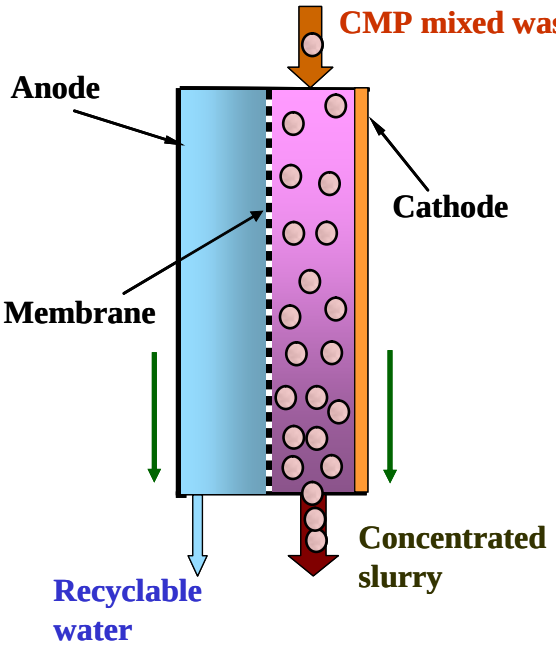
Low-Energy Wastewater Treatment

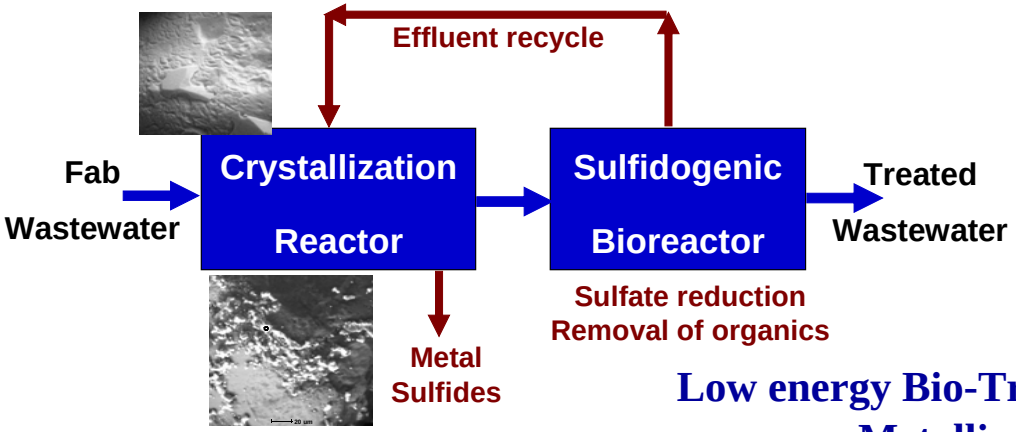
Baygents, Farrell, Field, Ogden, Raghavan, Sierra, Shadman (UA)

Integrated Filtration & Oxidation



Field-Assisted Membrane Treatment of CMP Waste





Low energy Bio-Treatment of Organic and Metallic Contaminants

Selected Facts/Figures

- **Research: 58 research projects; average of 25 peer-reviewed publications/year**
- **48 national/international awards and fellow positions for students; many institutional fellowships and scholarships**
- **21 national/international awards for faculty**
- **Technology Development: 16 patents**
- **Technology Transfer: 28 joint ventures with member companies**
- **Five new spin-off companies**
- **$1 M endowed chair**

Education and Outreach

- **Pre-University Outreach**
  - **Wide range of activities (example: *Teachers Institute* for science teachers; 73 teachers from 25 schools have participated and graduated)**
  - **74 REU undergraduates (60% are women and minorities)**
- **University Education:**
  - **Industry internship for students**
  - **Research experience for undergraduates**
  - **New courses in *benign manufacturing***
- **Post-University Education:**
  - **36 short courses and workshops for practicing scientists and engineers; weekly Tele-Seminars; distance learning courses; internships for industry residents at universities; faculty sabbaticals sponsored by industry**

ERC Membership and Affiliate List

- **Advanced Micro Devices, Inc.**
- **Air Products and Chemicals, Inc.**
- **Applied Materials, Inc.**
- **Arkema, Inc.**
- **Asahi Sunac Corporation**
- **Axcelis Technologies, Inc.**
- **BOC**
- **Cabot Microelectronics Corp.**
- **Cadence Design Systems**
- **Degussa AG**
- **DuPont Corp.**
- **Freescale Semiconductor, Inc.**
- **Fujikoshi Machinery Corp.**
- **Fujimi, Inc.**
- **Hitachi Chemicals Co., Ltd.**
- **IBM Corp.**
- **Industrial Tech Research Institute (ITRI)**
- **Infineon Technologies**
- **INOAC**
- **Intel Corp.**
- **LSI Logic Corp.**
- **National Inst. Standards and Tech. (NIST)**
- **NeoPad**
- **Novellus Systems, Inc.**
- **Pall Corp.**
- **Philips**
- **Powerchip Semiconductor Co.**
- **Praxair, Inc.**
- **Samsung Electronics Co.**
- **SCP Global Technologies**
- **SEMATECH**
- **Semiconductor Industry Association (SIA)**
- **Showa-Denko Inc.**
- **ST Microelectronics**
- **Texas Instruments, Inc.**
- **Tokyo Electron, Ltd.**
- **TSMC**
- **United Microelectronics Corp.**

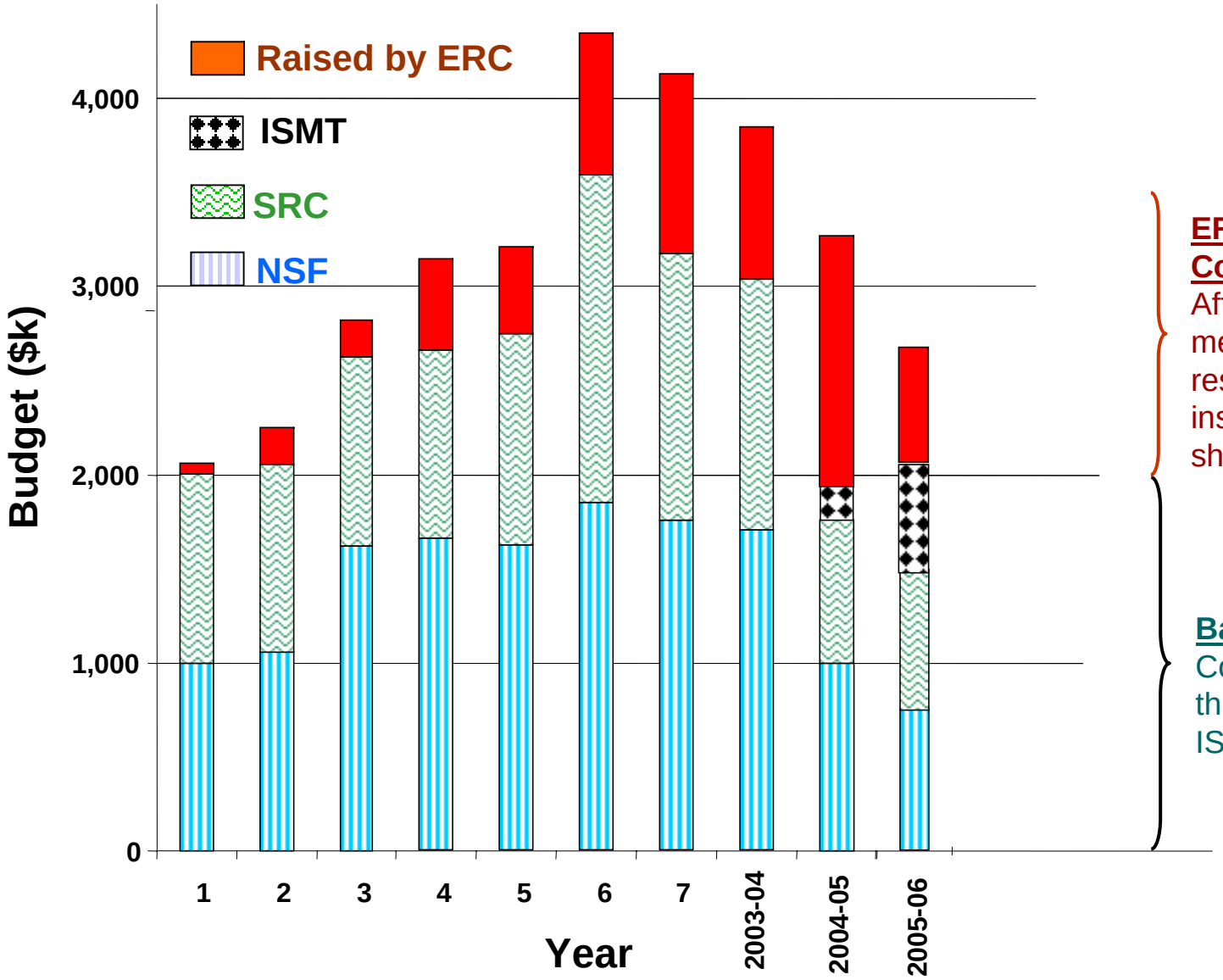
Faculty Awards in 2005

- **Steve Beaudoin: Student Government Teaching Excellence Award, Purdue**
- **Paul Blowers: Award for Excellence at the Student Interface, UA**
- **Karen Gleason: Franciscus C. Donders Visiting Prof Chair, University of Utrecht**
- **Anthony Muscat: da Vinci Circle Fellow, UA**
- **Chris Ober: ACS Award in Applied Polymer Science**
- **Chris Ober: Elected Vice President of the IUPAC Polymer Division**
- **Chris Ober: Xerox Lecturer at the Canadian High Polymer Forum**
- **Ara Philipossian: Takagi Prize, Japan Society for Precision Engineering**
- **Rafael Reif: Provost, MIT**
- **Farhang Shadman: Regents Professor, UA**

Student Awards in 2005

- **Katy Bosworth (Cornell): IBM Fellowship**
- **Drew Forman (Cornell): SRC Fellowship**
- **Darren DeNardis (UA): Thomas Chapman Fellowship**
- **Darren DeNardis (UA): Outstanding Paper Award, VLSI/ULSI Multilevel Interconnection Conference**
- **Umur Yenal (UA): Environmental Scholarship from SEAEMS**
- **Daniel Rosales-Yeomans (UA): Best Paper Award, NMS: Environment, Safety, and Health**
- **Zheng, X. (UA): Outstanding Paper Award, Electronic Computational Chemistry Conference**
- **Ashok Muthukumaran (UA): National Association of Corrosion Engineers Graduate Scholarship**
- **Caprice Grey (Tufts): Provost Fellowship**

ERC Financial Status



ERC Fundraising Commitment: Affiliate/intl membership; research grants; institutional cost-sharing, etc.

Base Funding: Core members through SRC and ISMT

Core Projects Selected for 2006-2007

1. **An Integrated, Multi-Scale Framework for Designing Environmentally-Benign Copper, Tantalum, and Ruthenium Planarization Processes**
2. **CMOS Biochip for Rapid Assessment of New Chemicals**
3. **Destruction of Perfluoroalkyl Surfactants in Semiconductor Process Waters Using Boron-Doped Diamond Film Electrodes**
4. **EHS Impact of Electrochemical Planarization Technologies**
5. **Environmentally Benign Electrochemically Assisted Chemical Mechanical Planarization (E-CMP)**
6. **Environmentally Benign Vapor Phase and SC CO_2 Processes for Patterned Low- k Dielectrics**
7. **Environmentally-Friendly Cleaning of New Materials and Structures for Future Micro-and Nano-Electronics Manufacturing**
8. **Low Environmental Impact Processing of sub-50 nm Interconnect Structures**
9. **Low-Water and Low-Energy Rinsing and Drying of Patterned Wafers, Nano-Structures, and New Materials Surfaces**
10. **Non-PFOS/non-PFAS Photoacid Generators: Environmentally Friendly Candidates for Next Generation Lithography**
11. **Reductive Dehalogenation of Perfluoroalkyl Surfactants in Semiconductor Effluents**

Thrust A
Back-End Processes
Overview

February 23, 2005

Agenda

- Overview … Philipossian … 5 min

- Task A – 1 … Boning … 5 min
- Tasks A – 2 – 1 and A – 2 – 2 … Gleason … 10 min

- Planarization LRP, Tasks A – 4 – 2, A – 5, A – 6 – 3, A – 7, A – 8 and A – 10 … Philipossian … 20 min
- Tasks A – 4 – 1, A – 6 – 1, A – 6 – 3 and A – 9 … Boning … 15 min

- Q & A … 5 min

Tasks … 3D ICs and LK Dielectrics

- Total of 4 PIs and 6 PhD students
- A – 1 … Environmentally Benign Manufacturing of 3D ICs
  - Prof. D. Boning (MIT)
  - Prof. P. Gschwend (MIT)
  - Prof. R. Reif (MIT)
- A – 2 – 1 … Solventless LK Dielectrics
  - Prof. K. Gleason (MIT)
- A – 2 – 2 … Environmentally Benign Precursors for Pore Scaling and Repair of Porous LK Films
  - Prof. K. Gleason (MIT)

Tasks … Planarization

- Total of 6 PIs, 18 PhD students, 2 undergraduate students, 1 post-doc, 1 consultant and 2 visiting researchers

- A – 4 – 1 … Modeling of Pattern Dependency Effects
  - Prof. D. Boning (MIT)

- A – 4 – 2 … Fluid Dynamics Analysis and Tribological Characterization
  - Prof. A. Philipossian (UA)
  - Prof. C. Rogers (Tufts)
  - Prof. V. Manno (Tufts)

- A – 5 … Fundamental Pad Characterization
  - Prof. A. Philipossian (UA)

Tasks … Planarization (continued)

- **A – 6 – 1 … ECMP of Copper**
  - **Prof. S. Raghavan (UA)**
- **A – 6 – 3 … Coupled Plating and Planarization**
  - **Prof. D. Boning (MIT)**
- **A – 6 – 4 … Controlled Atmosphere Polishing & Novel Pad Conditioning**
  - **Prof. A. Philipossian (UA)**
- **A – 7 … Post-Planarization Cleaning Waste Minimization**
  - **Prof. A. Philipossian (UA)**

Tasks … Planarization (continued)

- **A – 8 … Fundamental Characterization of Diamond Wear in CMP**
  - **Prof. A. Philipossian (UA)**
- **A – 9 … Environmentally Benign Copper Planarization for Advanced IC Manufacturing**
  - **Prof. S. Beaudoin (Purdue)**
- **A – 10 … Mechanistic Study of Novel Orbital Polishers for Copper CMP**
  - **Prof. A. Philipossian (UA)**

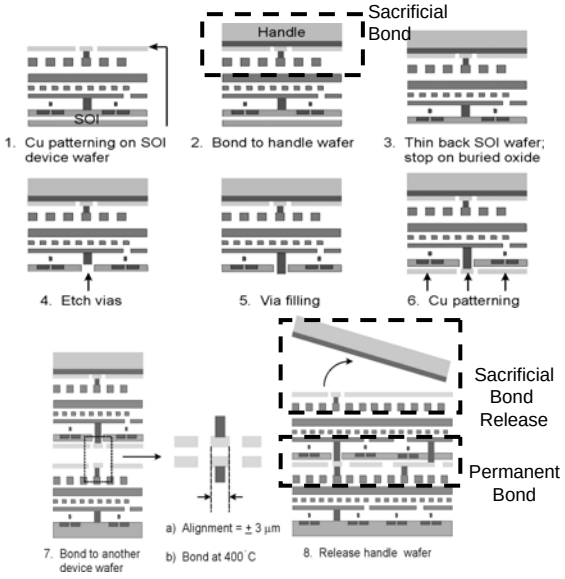
Environmental Assessment of New Technology Options – EBSM of 3D Integrated Circuits (Task A1)

- Faculty:
  - Prof. Philip Gschwend, MIT Civil & Environmental Engineering
  - Prof. Duane Boning, MIT EECS
  - Prof. Rafael Reif, MIT EECS (ending)
- Students
  - Ajay Somani, PhD Candidate, MIT Mat. Sci. and Eng.
  - Sarah Jane White, PhD Candidate, MIT Civil & Eng. Eng.
- Research Objectives:
  - Develop methodology to analyze environmental impacts for new process technologies
  - Construct a corresponding database which is more transparent than previous LCA studies
  - Identify critical unit processes that need to be designed with environmental considerations in addition to performance and cost

Technology Assessment/ Comparison Methodology

1. Identify ***boundaries*** for analysis (wafer fabrication)
2. Define ***functional unit*** for comparison (e.g., # of transistors)
3. Generate environmental ***footprint*** for fabrication of a standard IC functional unit with chemical/material specificity
4. ***Compare alternative*** fabrication technologies with respect to ***performance, cost and environmental footprint***
5. ***Identify critical unit processes*** which have performance, cost, or environmental issues
6. ***Design new unit process*** approaches to improve performance, cost, AND environmental issues

Case Study: MIT 3-D Process Flow

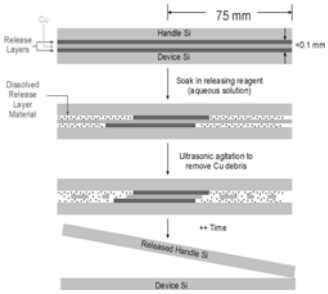


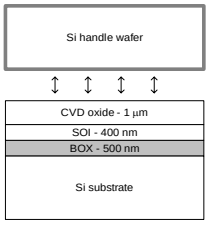
2-D vs. 3-D Process Steps/Footprint

Unit operation	2D process flow (for one wafer)	Additional 3D processes in flow
Photo/Stepper/Ashing	25	1
Dry Etch	13	2
Wet Etch/Clean	31/14	3/4
CVD	11	1
CMP	14	2
Sputtering Al	1 (0.5 µm for metal 1)	2 (20 µm)
Sputtering Ta/Cu	6	1
Electrodeposition Cu	6	1
Bonding	0	2
Grinding	0	1

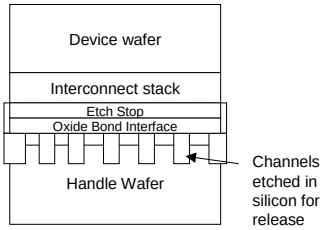
Critical step: handle wafer & release

Handle Wafer Options





Top wafer is bonded to handle wafer (CVD-to-thermal oxides bonding).



Al release layer[1]
- Described in MIT 3-D IC
- Requires 20 µm Al (twice) on each handle and device wafer
- Cu-Cu bonding, use Ta
- Yield is still an issue ~ for die level, works fine

Smart cut release[2]
- H_2 implant @ 150KeV
- High energy and expensive
- Use oxide-oxide bonding
- Thermal energy required to release
- Yield is good

Oxide release structures
- Similar oxide-oxide bonding
- Channels etched in handle wafer for release
- Nitride used as etch stop
- 49% HF used for release
- Yield is good but still to prove layer transfer – work in progress

[1] Fan et al., Electrochem. Solid State Lett., 2, 534 (1999)
[2] Tan et al., SOI Conference 2005

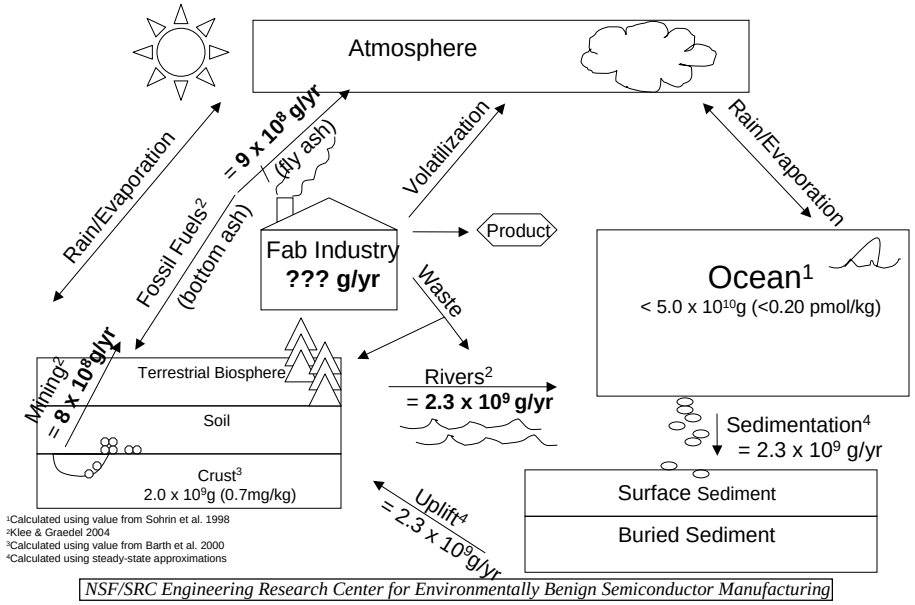
Comparison of Handle Wafer Options

Overall comparison	Al release	Smart cut	Oxide release
Yield (performance)	10% - depends on Cu-Cu bonding and mass transfer of acid	80% - work with oxide bond subjected to CMP oxide	80% subjected to functionality – as layer transfer is yet to be proven
Cost -additional	Cost for depositing Al on Si wafer which means 1.2 X	Cost for H_2 implantation which is 10 X	Oxidation, etch along with one CMP which means 1.2X
Environmental - additional	Illustrated very briefly in table below.		

Environmental comparison for additional steps	Al release	Smart cut	Oxide release
Energy	50-100 KWH primarily Al sputtering	20-40 KWH primarily H_2 implant	10-20 KWH oxidation, CMP, Photo and etch
Water	Primarily PCW for cooling Al dep./ Wet etch requires DI water	PCW for implantation, CMP and annealing	PCW for oxidation, etching and CMP, DI water for wet etch in 49% HF
Chemical (inputs)	Al, HCl (Ta), Cu	H2, SiH2Cl2, O2, CMP slurry, piranha	SiH2Cl2, O2, CMP slurry, NH4, HF, piranha, photoresist
Chemical (outputs)	$AlCl_3$, HCl	Oxide CMP waste, oxide dep. exhaust	Oxide CMP waste, oxide and nitride dep. exhaust, HF, SIF4

- Overall comparisons of different handle wafer options are considered
  - Performance here primarily is denoted by yield
  - Cost are estimates and are expressed in terms of one Si wafer
  - Additional means processes required for that handle wafer option
- Environmental comparison of different handle wafer options
  - Energy has been estimated based on which processes are energy intensive in that option
  - Water usage – process cooling water (PCW), de-ionized (DI) water for cleaning
  - Chemical Inputs depend on process and probable outputs are listed
  - **Contrast manufacturing fluxes with estimates of natural fluxes (e.g., Ta)**

Global Cycle of Tantalum: Contrast natural and industrial fluxes



[1]Calculated using value from Sohrin et al. 1998
[2]Klee & Graedel 2004
[3]Calculated using value from Barth et al. 2000
[4]Calculated using steady-state approximations

Task A1 – Summary and Current Work

- Methodology for technology/environment evaluation established
  - Establish environmental footprint (energy and specific material uses) for standard flow
  - Comparing with new/additional significant processes in technology options
- MIT 3D technology as case study
  - Identified handle wafer as critical process in 3D IC
    - Comparing different options for handle wafer on three axes: performance, cost and environment
  - Energy analysis completed
  - Material emissions analysis (e.g. Tantalum, Indium, …) in progress

Solventless Low k Dielectrics (Task 425.001: ERC EBSM)

Tom Casserly[+], Kelvin Chan[+], April Ross[+]*

and Karen Gleason

Department of Chemical Engineering

Massachusetts Institute of Technology

**now at Applied Materials*

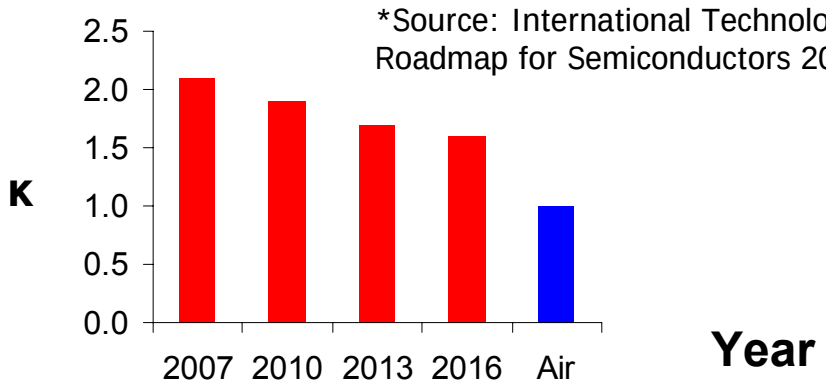
[+]SRC Fellowships

Evolution of Low-k Dielectrics

Either increasing fragile porous low k materials must be integrated

or

A robust sacrificial layer must be integrated which can form air in the final step *(sacrificial layer = 100% porogen)*



"Let's face it. The air gap is a pretty crazy idea. Rather than filling the space between interconnecting wires with anything that would increase line-to-line capacitance and RC delay, just go straight for the best performing low-k dielectric of all: Air. More unusual things have happened. Like effectively taking sandpaper to your device — later perfected into the state-of-the-art technology of CMP."

Laura Peters, Senior Editor -- 1/1/2005, Semiconductor International

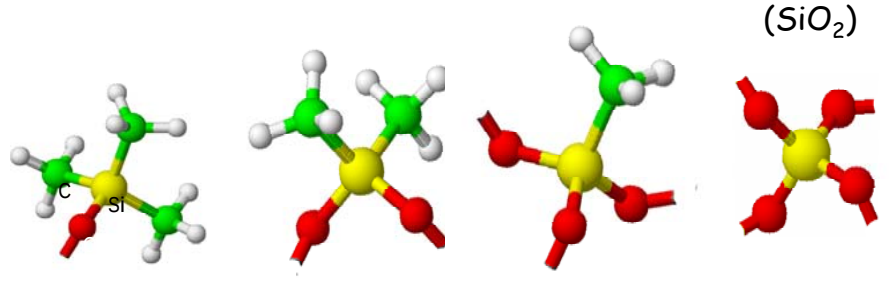
Early air gap work:

- **Havemann and Jeng (TI), US Patent 5461003, 1995.**
- **Anand *et al., IEEE*, 1997.**

OSG Mechanical Properties

"For solids in which all atoms are able to form two or more bonds, the percolation of rigidity occurs at an average connectivity number of 2.4"*

* J. Phillips, *J. Non-Cryst. Solids* **34**, 153 (1979)

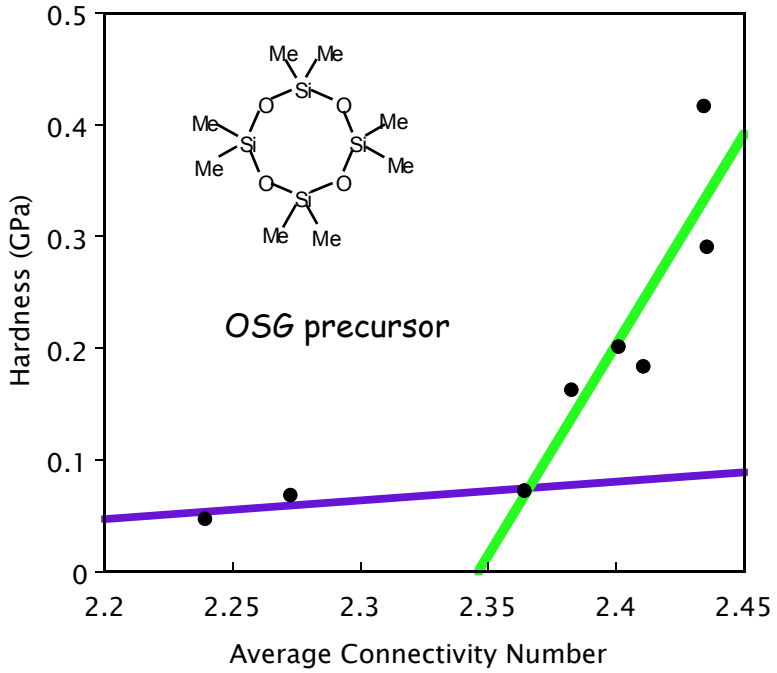


'M' Group
Chain Terminating
<r> = 1.5

'D' Group
Chain Propagating
<r> = 2.0

'T' Group
Crosslinking
<r> = 2.4

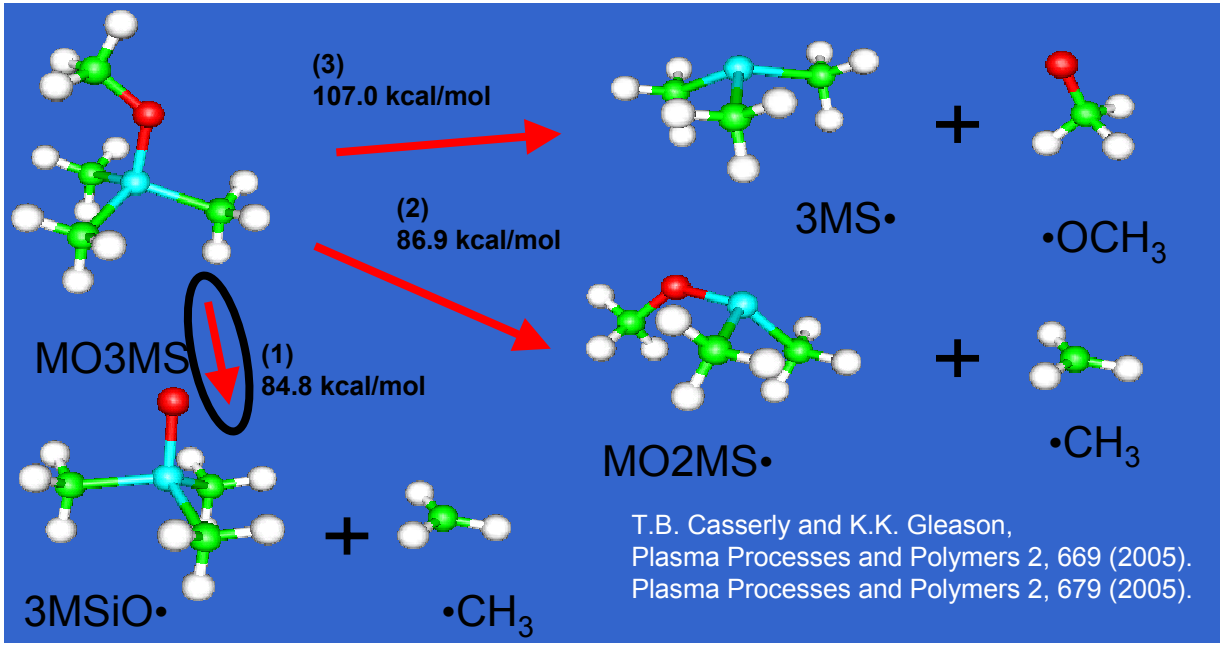
'Q' Group
Fully Networked
<r> = 2.67

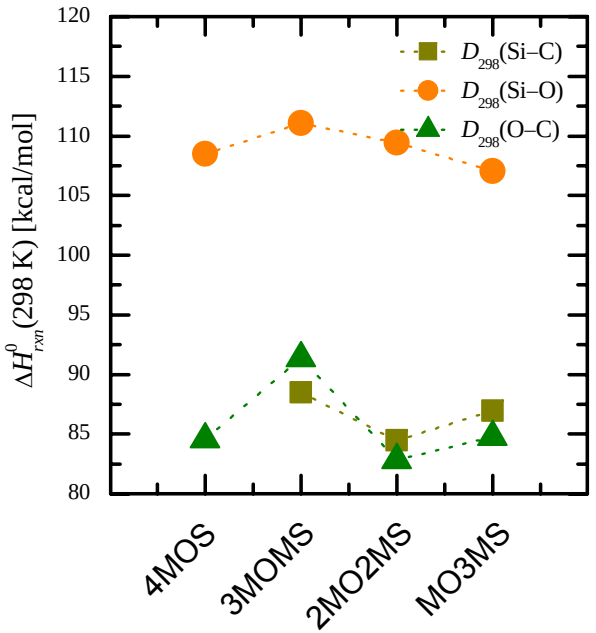


Ross AD and Gleason KK, J. Appl. Phys. 97, 113707 (2005)

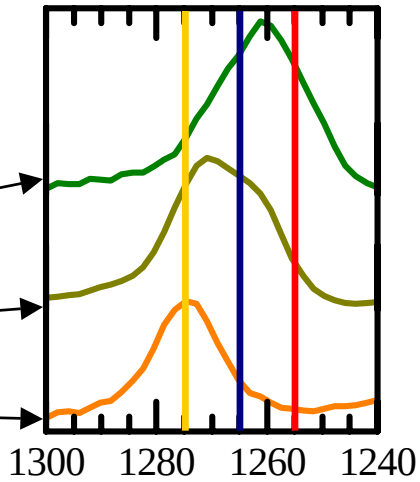
100% T groups gives a matrix just at the percolation threshold

Density Functional Theory for OSG Precursors





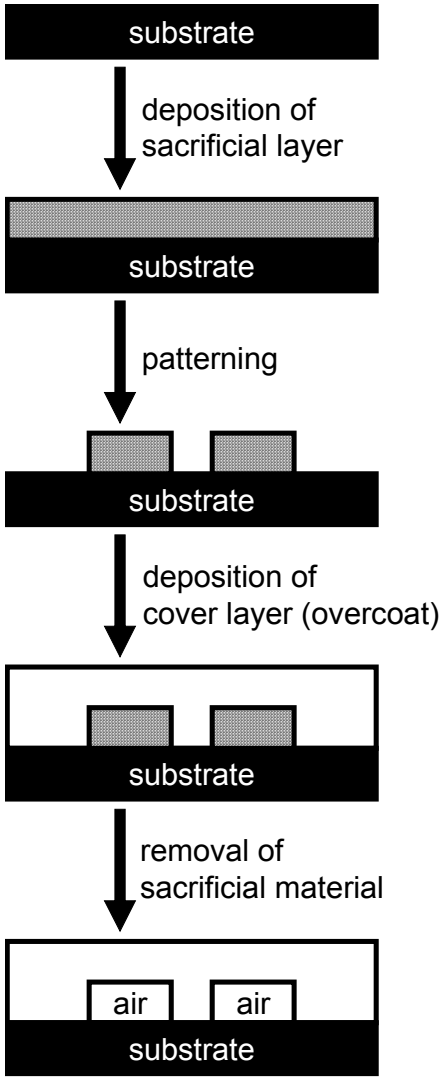
- Si-O bond is strongest (likely preserved)
- Si-C and O-C bonds have similar bond strengths
  - No selectivity
  - Likely loss of Si-C bonding
- Expectations
  - MO3MS – M
  - 2MO2MS – D
  - 3MOMS – T



FTIR from low power PECVD films

DFT predicts even stronger selectivity to T group with addition of H_2 to 3MOMS

Air-Gap Fabrication

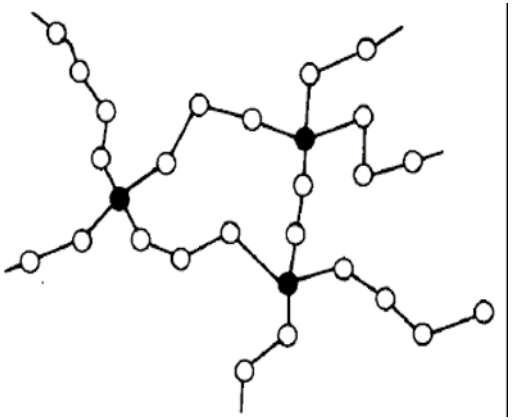


- **Ordinary Sacrificial Materials**
  - Require physical contact with etchant/solvent for selective removal
  - Surface-tension problems for wet processes
- **Self-Decomposing Sacrificial Materials**
  - Requires no agent for removal
  - Dry removal process (heat, UV, e-beam)
  - Allow fabrication of closed-cavity structures
- **CVD sacrificial layers**
  - evolutionary from CVD silicon dioxide and from OSG low k materials
  - environmentally attractive

CVD for Sacrificial Polymers

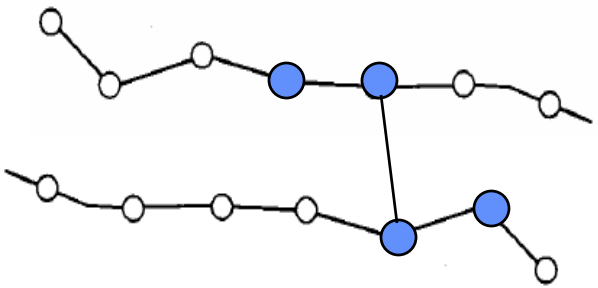
Plasma Enhanced

- nonselective chemistry
- uncontrolled crosslinking which gives rise to char formation: unsuitable for sacrifical layers



Initiated

- selective bond scission
- systematic compositional variation using feed gas
- controlled cross-linking
  - increases solvent stability (insolubility, lack of swelling)
  - increased thermal stability
  - increased mechanical strength
  - designed to prevent char formation

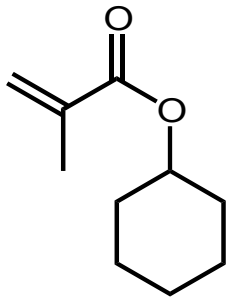


iCVD process characteristics:

- low energy input (<10 watts for 200 mm wafer)
- low-temperature process (substrate at ~ room temperature)
- no ion bombardment or UV irradiation (no plasma)
- All-dry process, no worker exposure to solvents

CVD Sacrificial Layer Chemistry

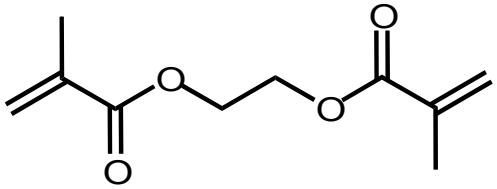
monomer



cyclohexyl methacrylate (CHMA)

Stable under normal temperatures and pressures.
Hazardous Decomposition Products: carbon monoxide, carbon dioxide.
Hazardous Polymerization: Will not occur.
Potential Health Effects: Causes eye and skin irritation.
Carcinogenicity: Not listed by ACGIH, IARC, NIOSH, NTP, or OSHA.

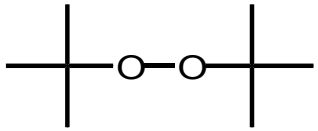
crosslinker



ethylene glycol dimethacrylate (EGDMA)

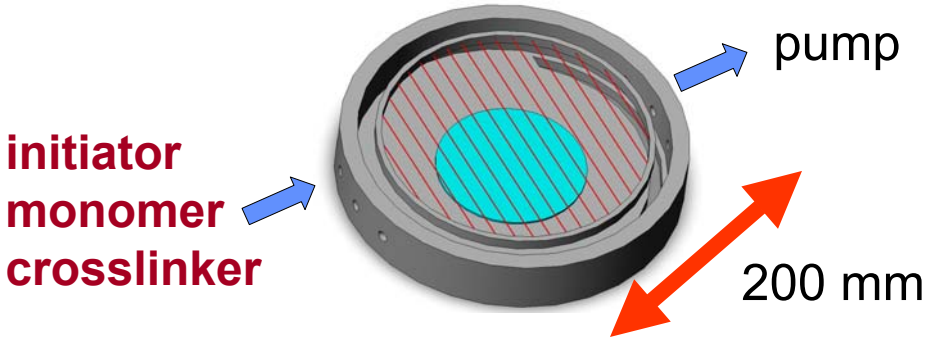
Stable under normal temperatures and pressures.
Irritating to respiratory system.
LD50/LC50: Oral, mouse: LD50 = 2 gm/kg; Oral, rat: LD50 = 3300 mg/kg.
Carcinogenicity: Not listed by ACGIH, IARC, NIOSH, NTP, or OSHA

initiator

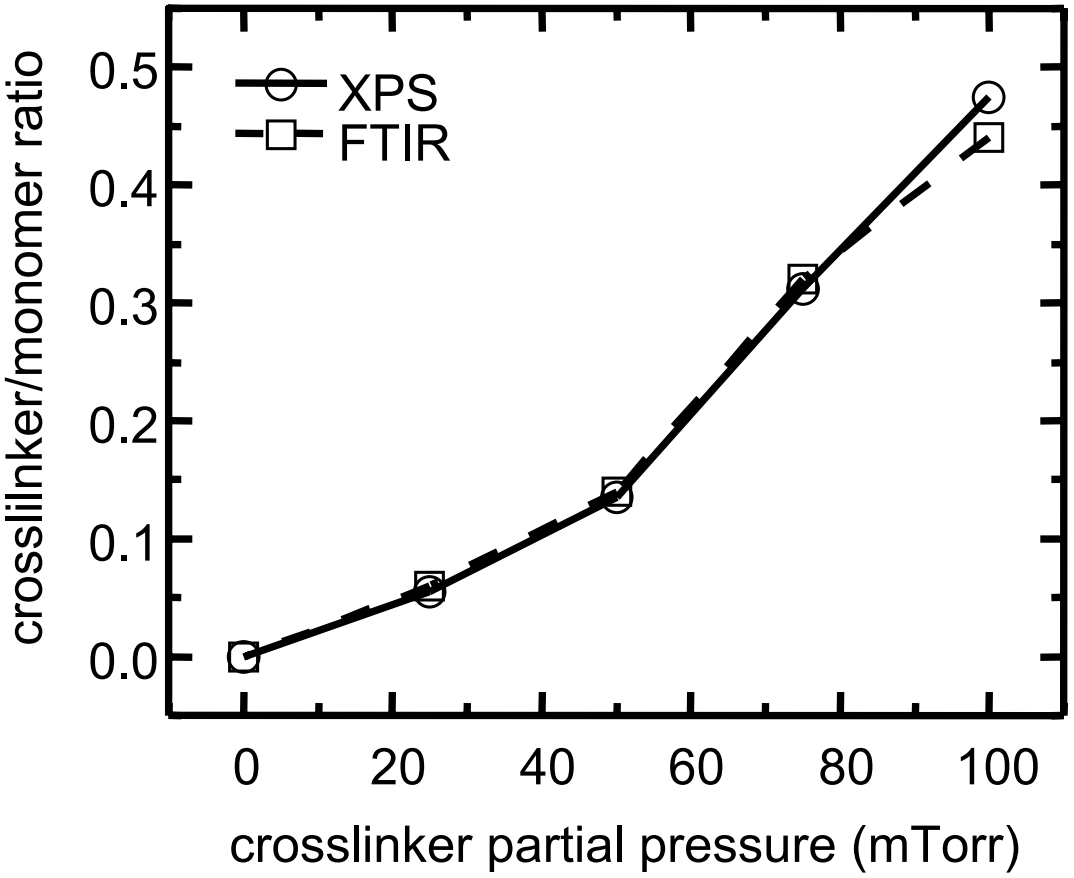


tert-butyl peroxide

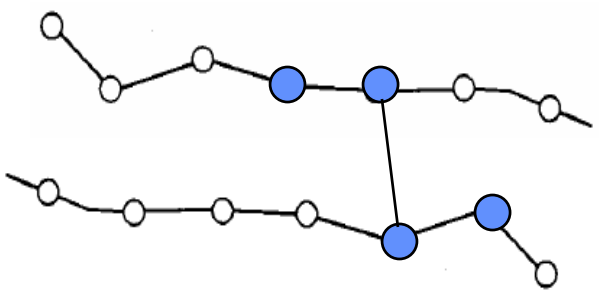
Stability : Explosive if heated, subjected to shock, or treated with reducing agents. Highly flammable. Refrigerate.
IPR-RAT LD50 3.210 g/kg : ORL-RAT LD50 > 25 g/kg
Carcinogenicity: Not listed by ACGIH, IARC, NIOSH, NTP, or OSHA



Cross-link Density (FTIR & XPS)

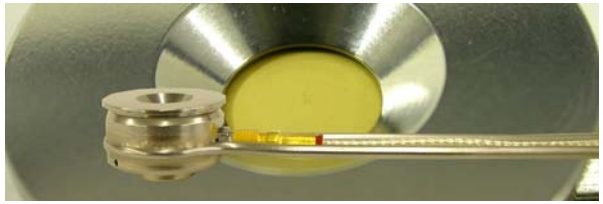


two independent methods confirm systematic control over crosslink incorporation in the film

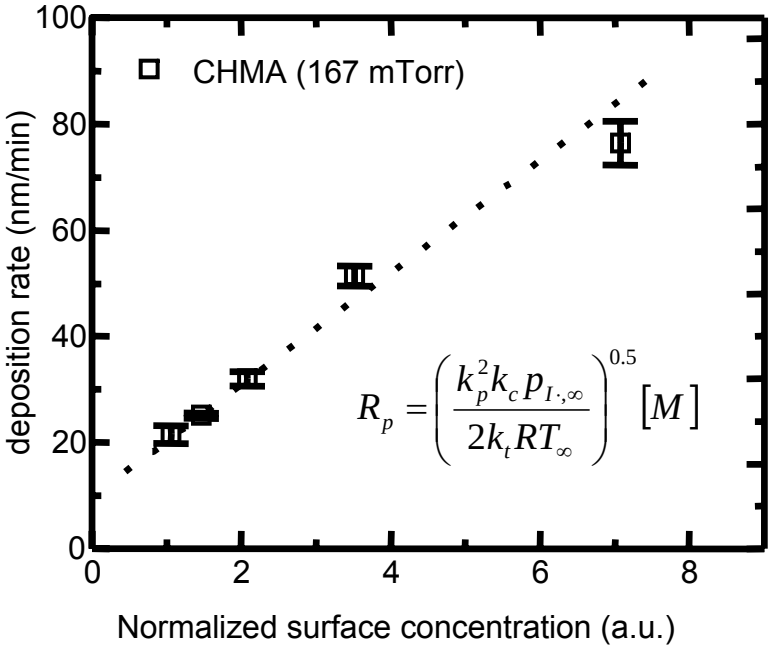


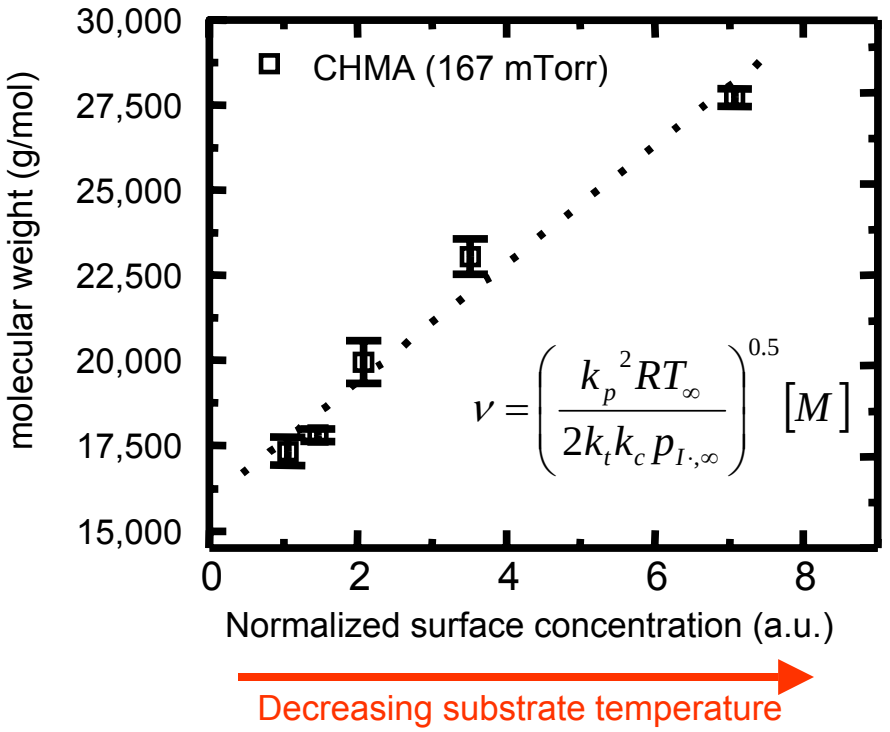
- degree of crosslinking can be systematically adjusted
- impossible to spin cast insoluble crosslinked material

Control using Surface Concentration



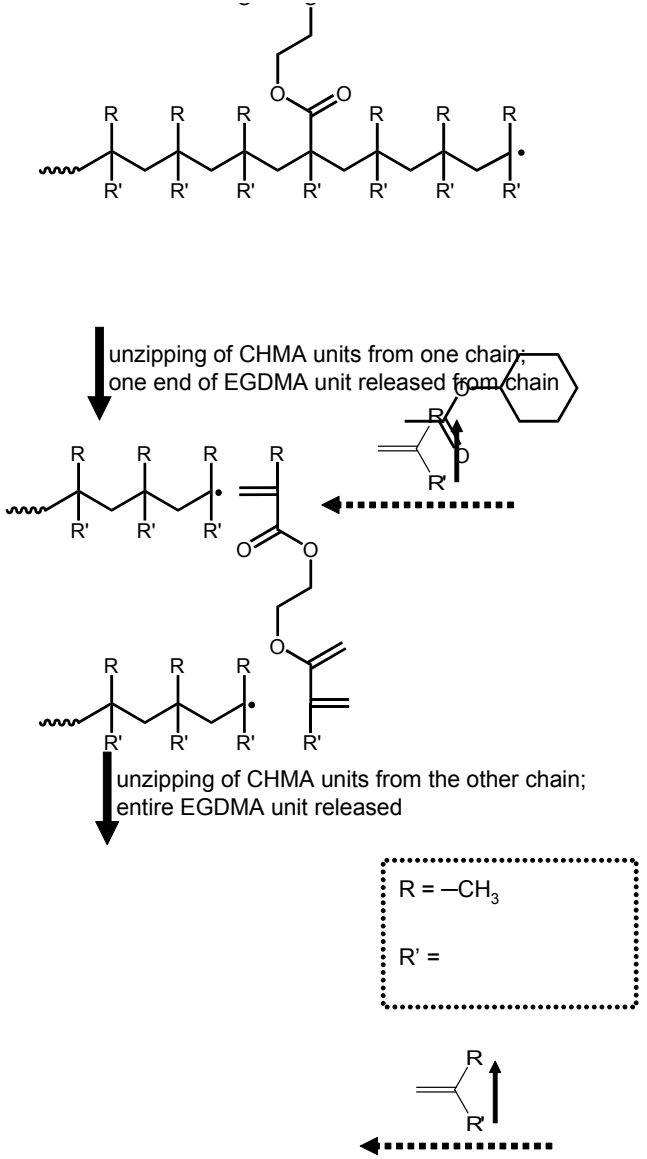
Quartz Crystal Microbalance (QCM)
measures surface concentration of monomer, [M],
in the absence of reaction



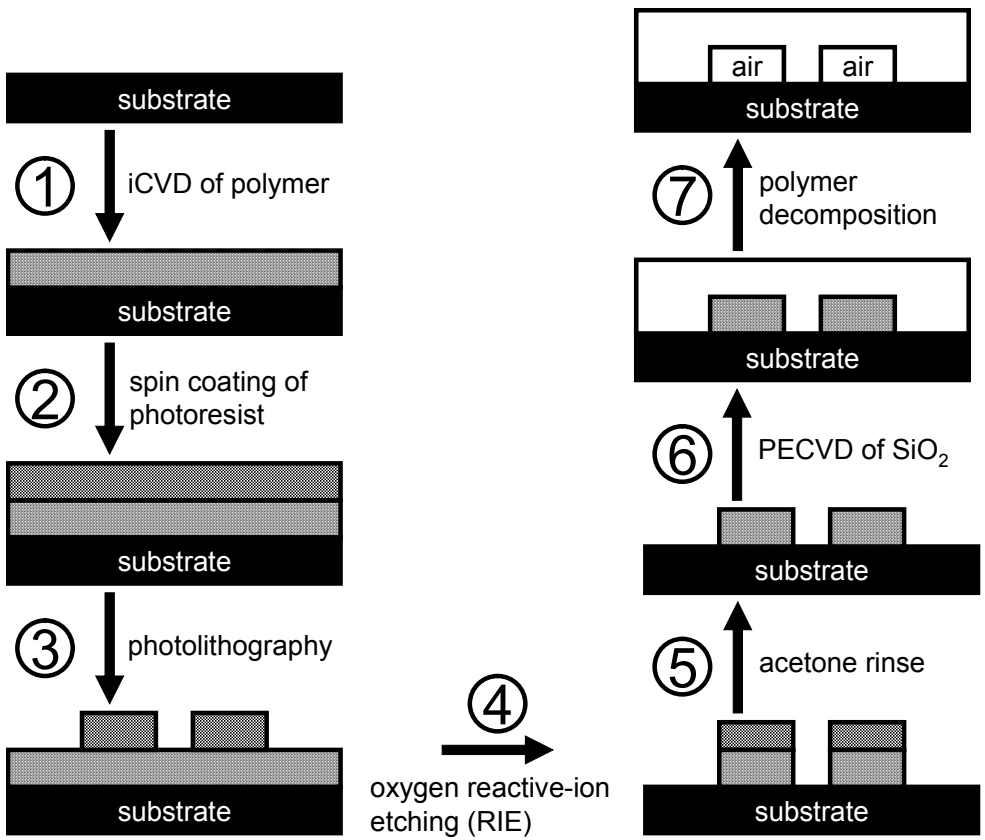


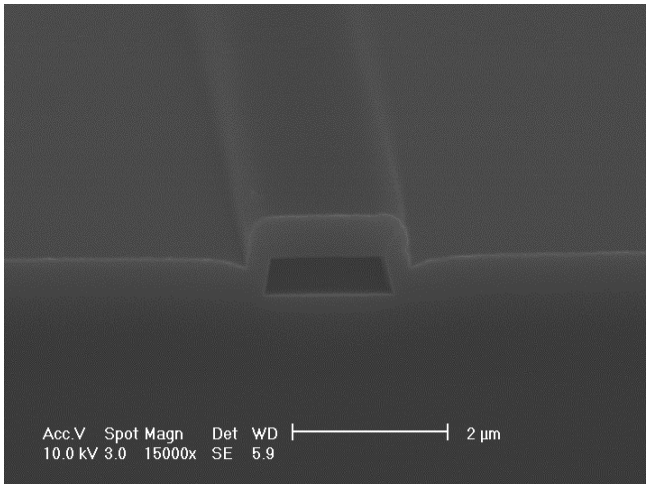
Film Properties

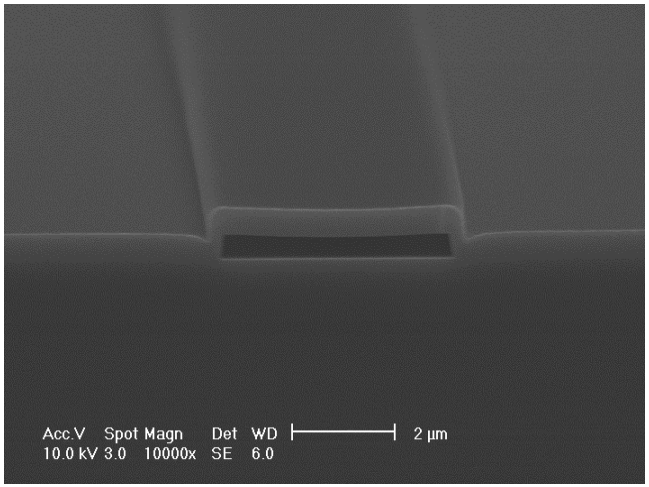
- Does not dissolve in any commonly used solvents: photoresist can be removed by dissolution instead of ashing.
- Decomposition > 99.7% by thickness (VASE). Crosslinking via the dimethacrylate monomer is key.
- Onset temperature of decomp. ~ 270 °C (ITS)
- Good adhesion to substrate and photoresist
- High etch rate in oxygen RIE (0.35 µm/min). Eliminates the need for a hard mask, an economic and environmental improvement over previously-reported spin-on sacrificial materials



Fabrication







With better lithography, smaller feature sizes can be fabricated.

- **no hardmask**
- **RIE resist strip**

Conclusions

- Local bonding environments in OSG films determine mechanical strength: all “T” groups represents a percolation of rigidity limit.
- Density functional theory (DFT) calculations for new precursors predict the likelyhood of formation of local bonding environments in OSG films.
- iCVD sacrificial layers represent a evolutionary and environmentally friendly strategy for the integration of air gaps.
  - controllable crosslinking which cleanly degrades
  - no hardmask required for fabrication

Thrust A
Planarization Long Range Plan

February 23, 2006

Principle Investigators

- **Prof. Ara Philipossian (University of Arizona)**
- **Prof. Duane Boning (MIT)**
- **Prof. Srini Raghavan (University of Arizona)**
- **Prof. Vincent Manno (Tufts University)**
- **Prof. Chris Rogers (Tufts University)**
- **Prof. Stephen Beaudoin (Purdue University)**

Planarization Advisory Committee Members

- **Dr. Paul Fischer (Intel)**
- **Dr. Laertis Economikos (IBM)**
- **Dr. Cliff Spiro (Cabot Microelectronics)**
- **Dr. Chris Borst (Texas Instruments)**

Landscape for the Next 5 Years

- **Research, fundamental in nature yet industrially relevant, addressing the technical, economic and environmental challenges of planarizing the following materials:**
  - **Copper**
  - **Tantalum and tantalum nitride**
  - **Ruthenium**
  - **Dielectric (for STI only)**

Gaps to be Filled in the Next 5 Years

- **Advanced processes and consumables (i.e. pads and chemical solutions) for electrochemically assisted planarization**
- **Advanced processes and consumables (i.e. chemical solutions, abrasive particles, pads and diamond conditioners) for planarization**
- **Advanced post-planarization cleaning and surface preparation processes and consumables (i.e. chemical solutions and brush rollers)**
- **Exploratory planarization schemes**
  - **Controlled Atmosphere Planarization (CAP) or others**

Advanced Processes & Consumables for Electrochemically Assisted Planarization

- **PIs:**
  - **Prof. Srini Raghavan**
  - **Prof. Duane Boning**
  - **Prof. Ara Philipossian**
- **Students:**
  - **3 Ph.D. students (2 at UA and 1 at MIT)**
- **Focus will be on the development and implementation of a 'full' process:**
  - **Clearing of copper (primary focus)**
  - **Planarization of the barrier layer (secondary focus)**

Advanced Processes & Consumables for Electrochemically Assisted Planarization

- **Objectives include development & implementation of:**
  - **Novel chemistries to enhance and control the electrochemical removal and passivation of copper, tantalum, ruthenium, or other future barrier materials**
  - **Novel pads to ensure electrical contact with isolated copper islands during clearing. This requires development of conducting pad technology, with appropriate mechanical, electrochemical & environmental properties.**
  - **Modeling and control of patterned wafer performance: the fundamental technological objective is formation of damascene patterned features, and modeling & characterization of tool, pad and wafer interactions for design and control (particularly endpoint detection) are needed to minimize process cost & environmental impact.**

Advanced Processes & Consumables for Planarization

- **PIs:**
  - **Prof. Duane Boning**
  - **Prof. Ara Philipossian**
  - **Prof. Vincent Manno**
  - **Prof. Chris Rogers**
  - **Prof. Stephen Beaudoin**
- **Students:**
  - **Seven Ph.D. students (3 at UA, 1 at MIT, 2 at Tufts and 1 at Purdue)**

Advanced Processes & Consumables for Planarization

- **Focus:**
  - **Basic scientific investigations of the controlling processes in planarization of advanced materials over several length scales and levels of complexity.**
  - **Development of validated, science-based descriptions that relate specific planarization process and material attributes to measurable process outcomes.**
  - **This understanding will allow environmentally-conscious process and material alternatives to be specified and tested in a rapid manner, and will allow for the rapid feedback of experimental results into the planarization design process**

Advanced Processes & Consumables for Planarization

- **Objectives**
  - **Real-time detection and modeling of pattern evolution**
    - **Develop novel force-spectra endpoint detection methods by determining how various wafer and pad surface states during polish affect the frictional energy in particular frequency bands.**
    - **Relate these signals to details of the wafer topography evolution by integrating pattern evolution models with the above endpoint or diagnostic signal analysis.**

Advanced Processes & Consumables for Planarization

- **Objectives (continued)**
  - **Wear phenomena and their effect on process performance**
    - **Isolate, quantify and model the hydrodynamic, van der Waals, hydrophobic and electrostatic processes that determine how nanoparticles interact with pads, diamonds and wafers in representative systems and how these interactions evolve with extended use.**
    - **Develop methods to visualize wafer-pad mechanical interactions in real-time using laser-induced fluorescence**
    - **Once the fundamentals of pad asperity evolution and the effect of the multitude of contacting bodies on pad asperities are understood, their impact on planarization capability can be modeled, thereby leading to the design of new polishing protocols and consumables that will deliver superior performance but with reduced environmental consequences.**

Advanced Processes & Consumables for Planarization

- **Objectives (continued)**
  - **Effect of pad grooving on process performance**
    - **Empirical and numerical investigation of the effect of various pad designs (materials, groove shapes, dimensions and slant angles) as well as different types of slurries on RR, COF and pad temperature for copper and tantalum CMP**
    - **Identification and verification of optimal pad designs for technology transfer to 300-mm platforms**

Advanced Post-Planarization Cleaning Processes and Consumables

- **PI**
  - **Prof. Ara Philipossian**
- **Student**
  - **One Ph.D. student at UA**
- **Focus:**
  - **Fundamental study of the effects of the brush material and nodule design on the frictional force, brush deformation and cleaning efficiency during silicon dioxide, carbide and copper post-CMP cleaning processes.**
  - **Study will not be limited to new PVA brushes**

Advanced Post-Planarization Cleaning Processes and Consumables

- **Focus (continued):**
  - **The potential degradation and performance of brushes as a function of extended use will also be investigated.**
  - **The ultimate goal of this work is to improve cleaning efficiency as well as extend the life of the PVA brush by understanding the mechanisms and modes of failure during normal and accelerated stress conditions.**

Task A – 4 – 1
Fluid Dynamics and Tribology of CMP

1st Generation Modified Langmuir – Hinshelwood Kinetics Model

'*n*' moles of reactant *R* in the slurry react at rate constant k_1 with copper film on the wafer to form a product layer *L* on the surface

$$\underline{Cu} + nR \xrightarrow{k_1} \underline{L} \qquad k_1 = A\exp(-E/kT_w) \qquad RR = \left(M_w/\rho\right)k_1$$

Product layer *L* *is* subsequently removed by mechanical abrasion with rate constant k_2

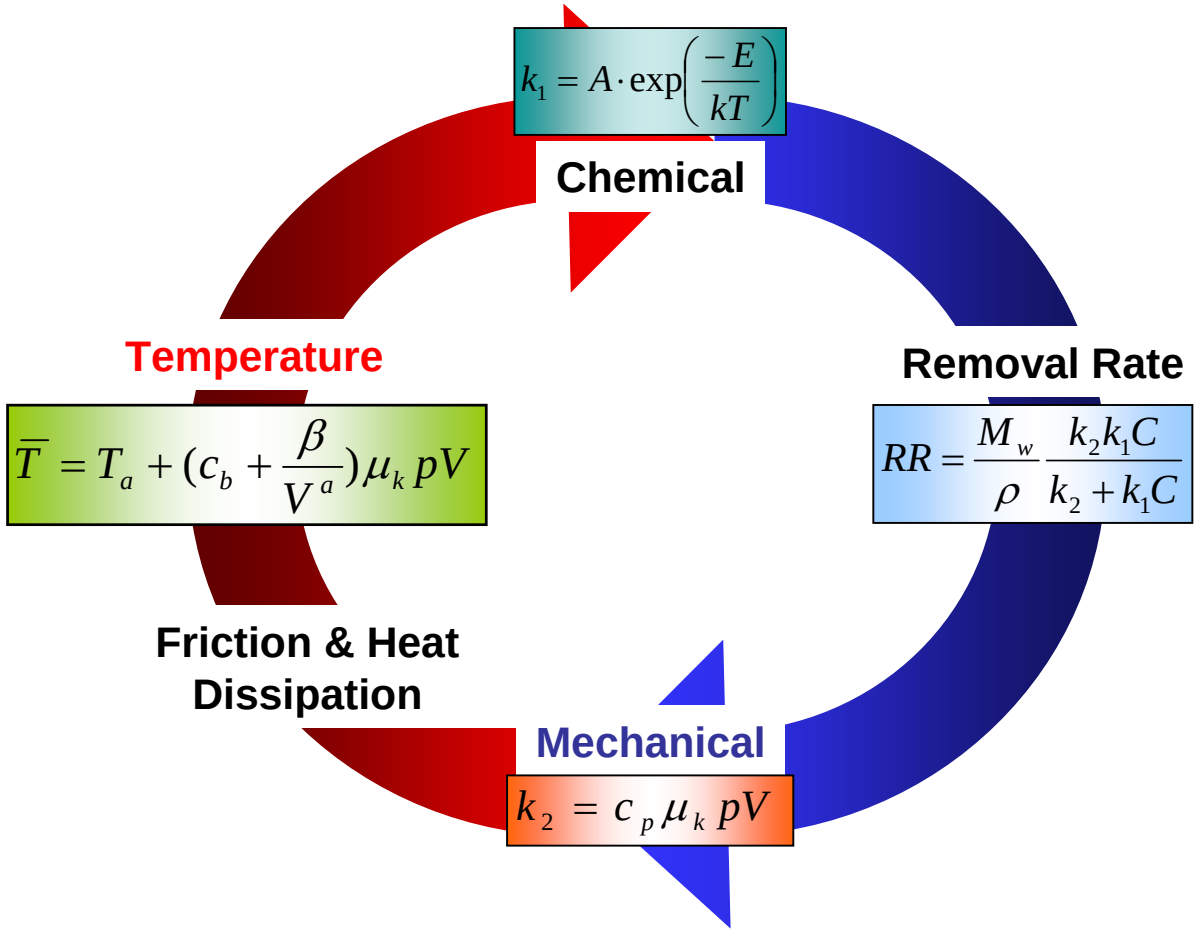
$$\underline{L} \xrightarrow{k_2} L \qquad k_2 = c_p \times (COF)\, pV \qquad RR = \left(M_w c_p/\rho\right)pV$$

Abraded material *L* is carried away by the slurry

$$RR = \frac{M_w}{\rho}\frac{k_1 C}{1+\frac{k_1 C}{k_2}}$$

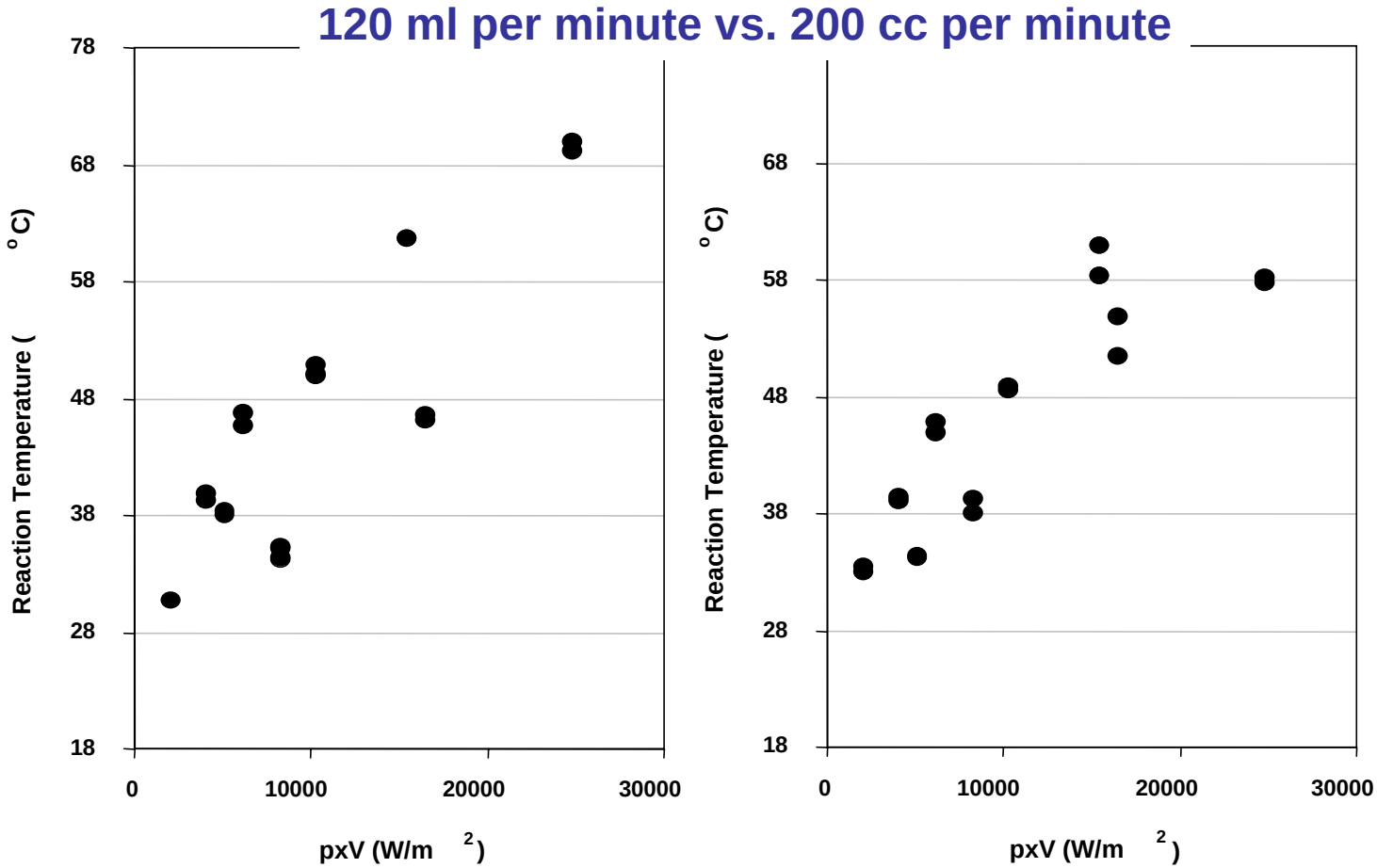
Task A – 4 – 1
Fluid Dynamics and Tribology of CMP

Integrating the Role of Temperature in CMP



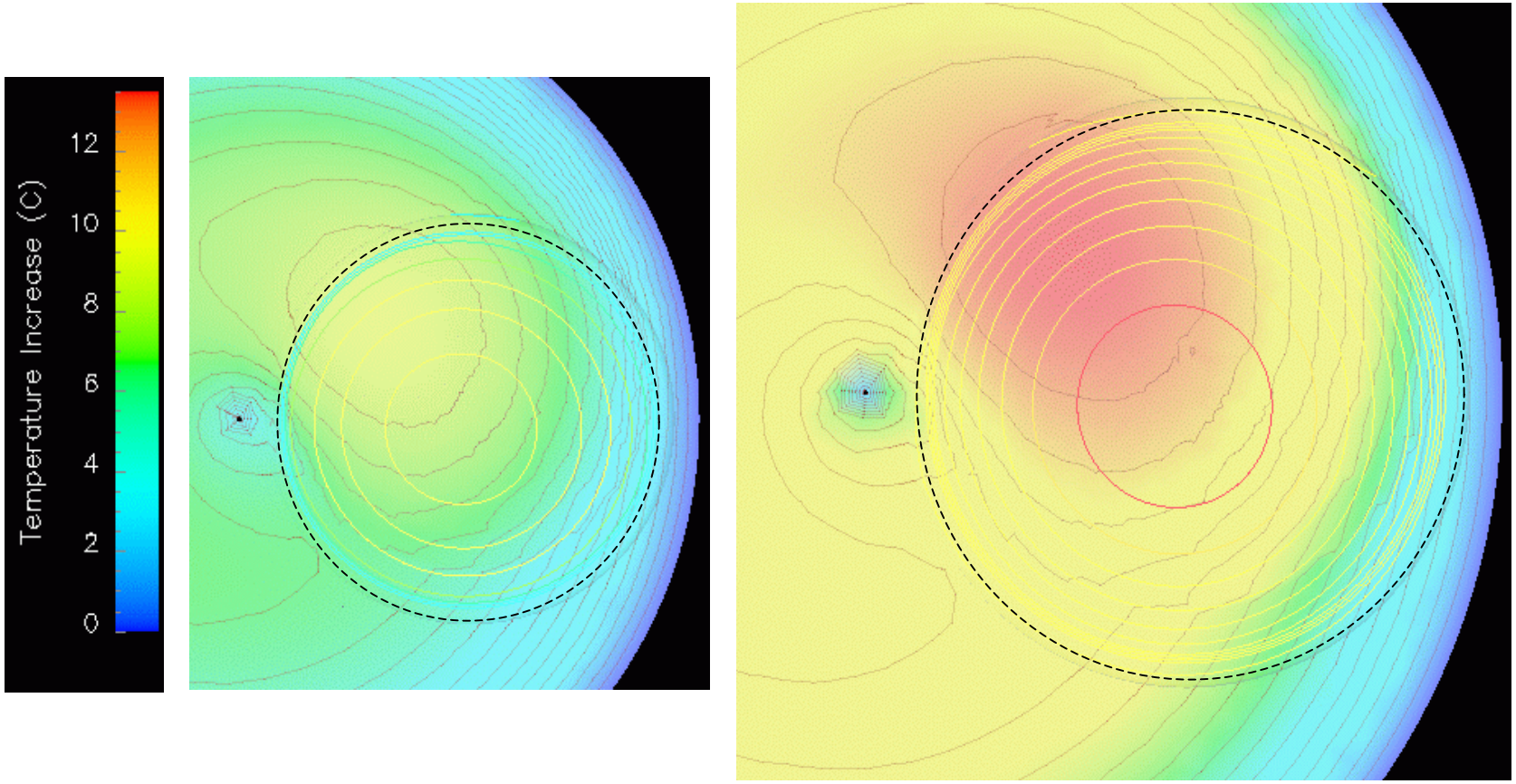
Task A – 4 – 1
Fluid Dynamics and Tribology of CMP

Reaction Temperature vs. Slurry Flow Rate



Task A – 4 – 1
Fluid Dynamics and Tribology of CMP

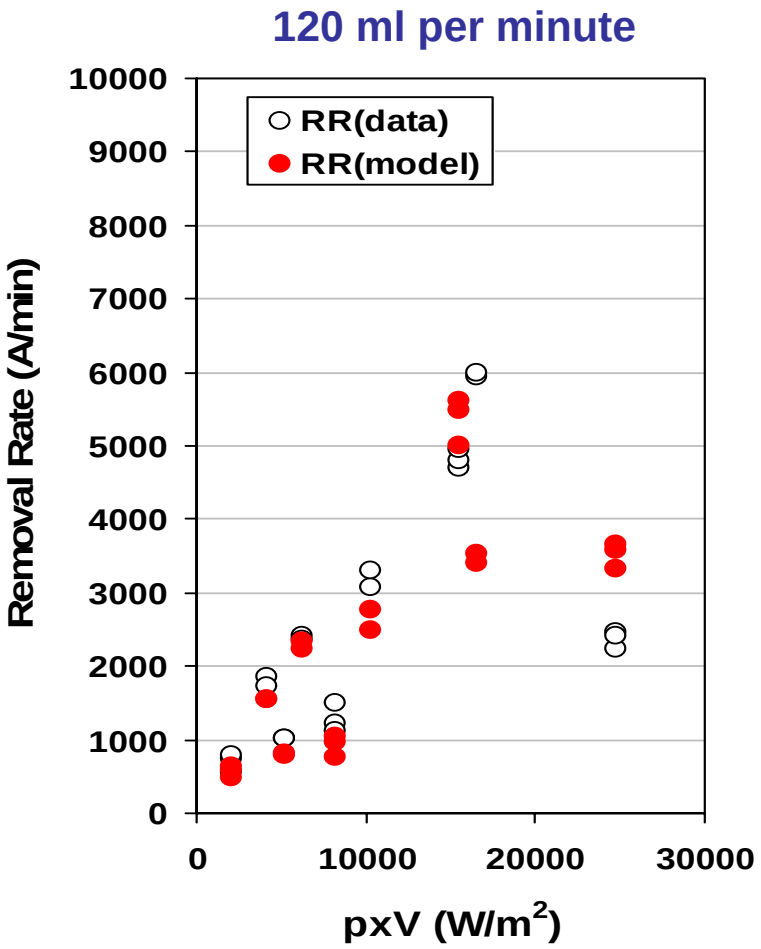
Pad Temperature vs. Wafer Size

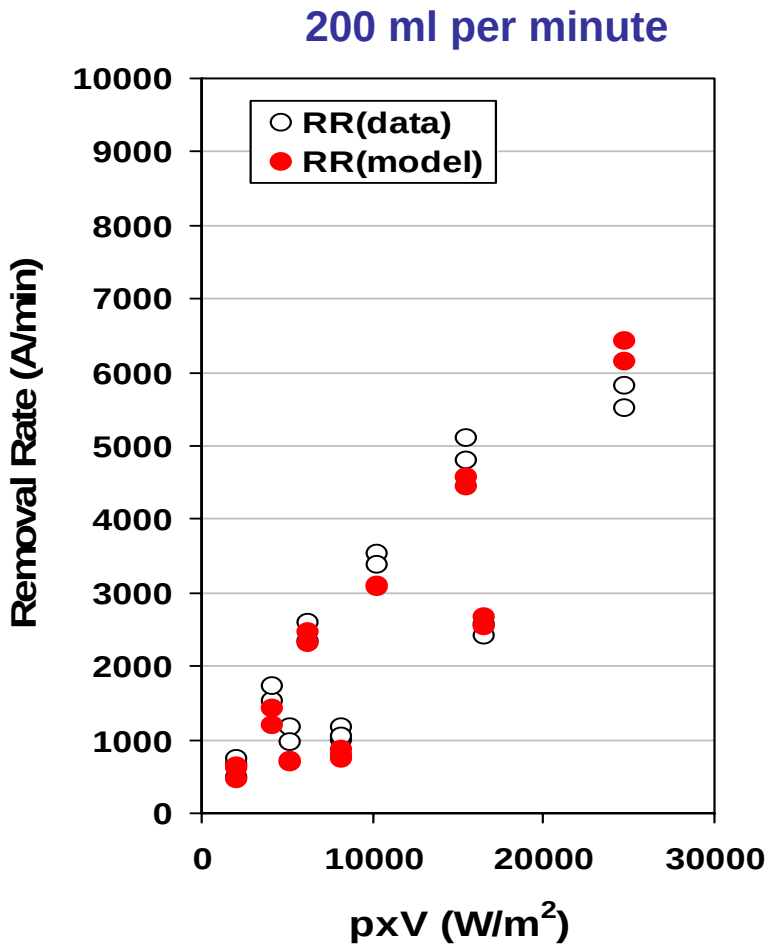


200 mm **300 mm**

Task A – 4 – 1
Fluid Dynamics and Tribology of CMP

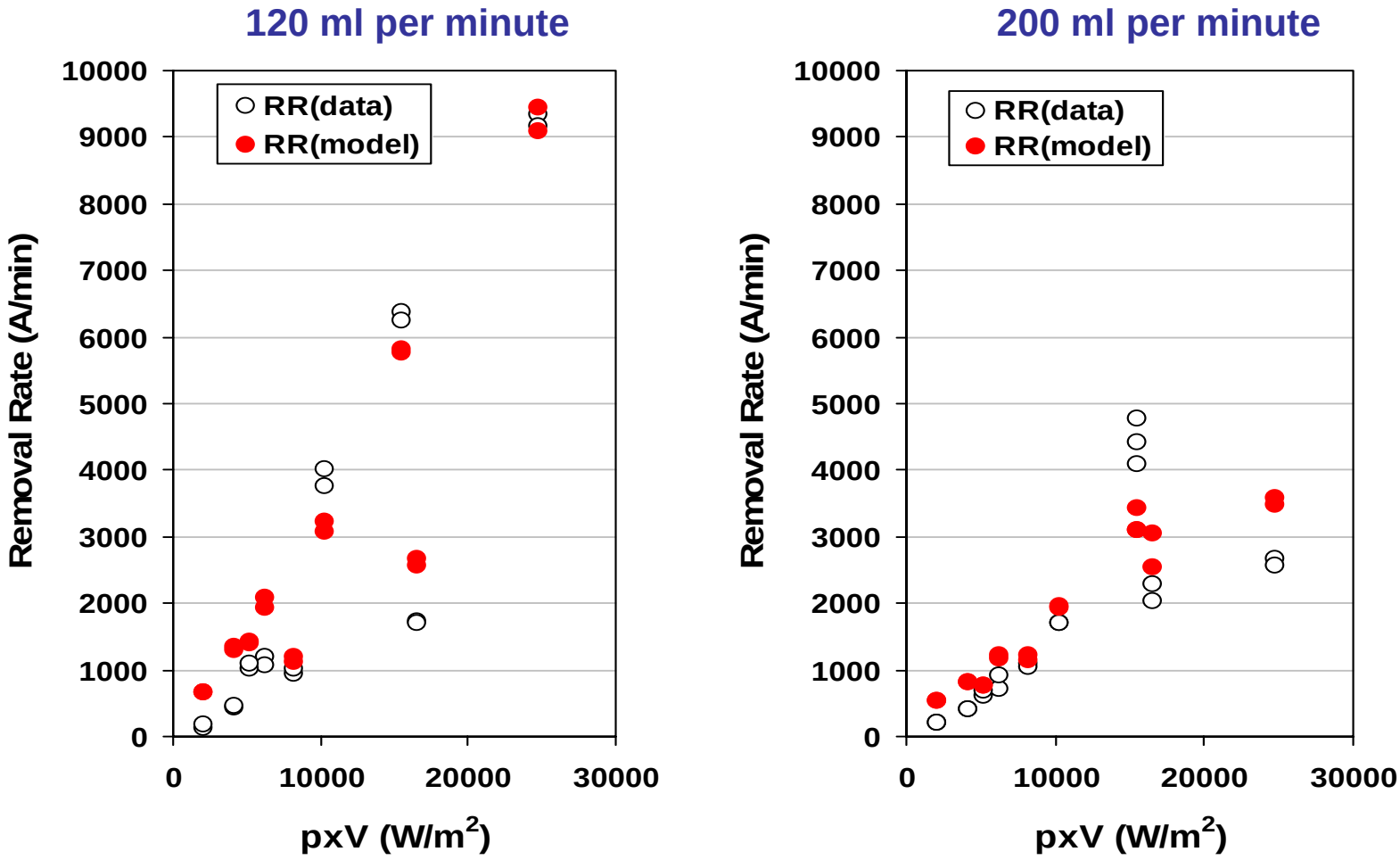
iCue 600Y75





Task A – 4 – 1
Fluid Dynamics and Tribology of CMP

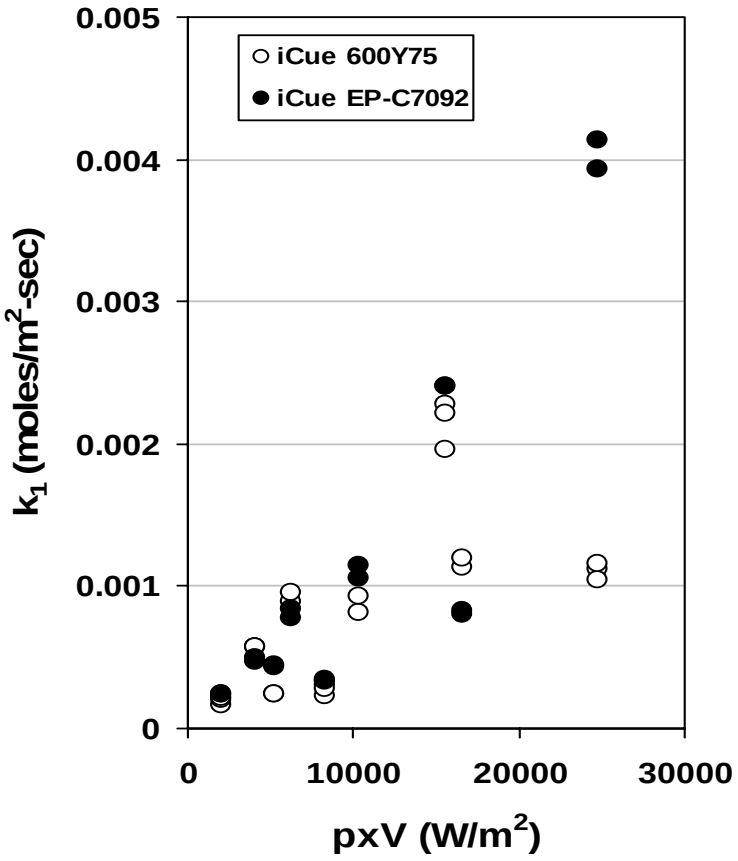
iCue EP-C7092



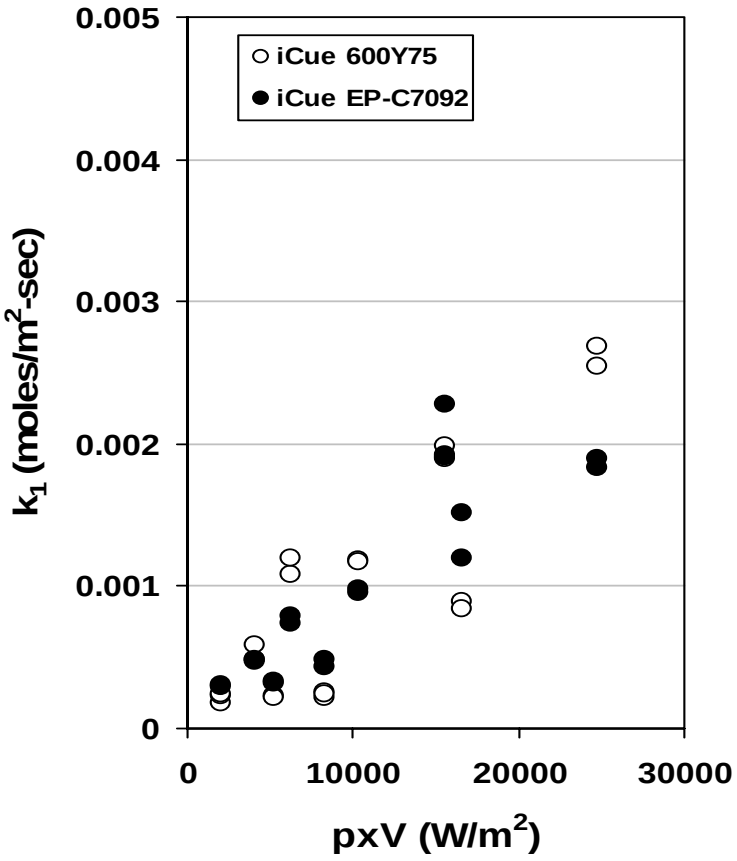
Task A – 4 – 1
Fluid Dynamics and Tribology of CMP

Chemical Rate Constant – k1

120 ml per minute



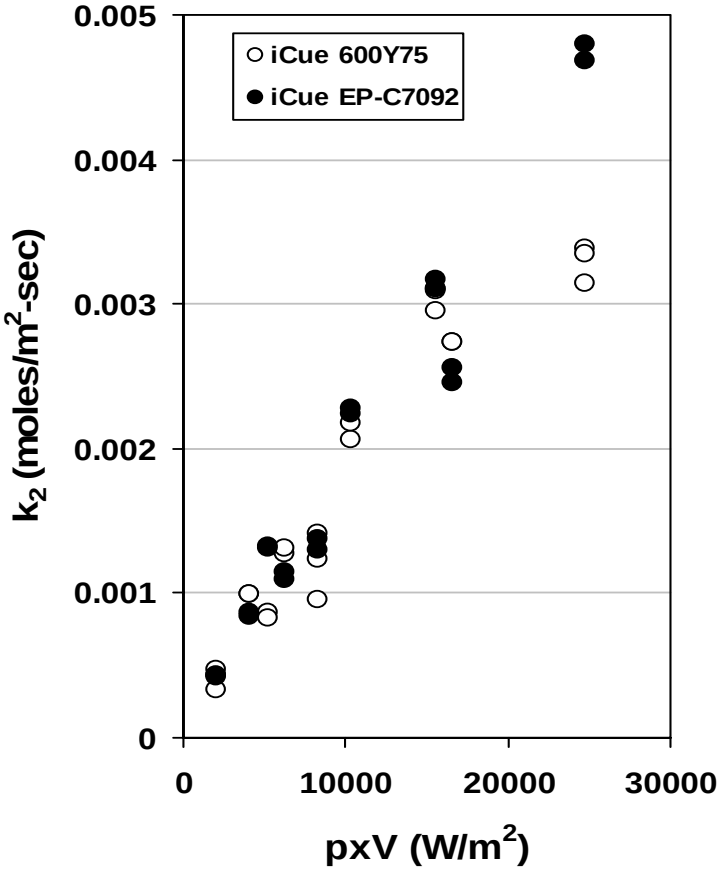
200 ml per minute



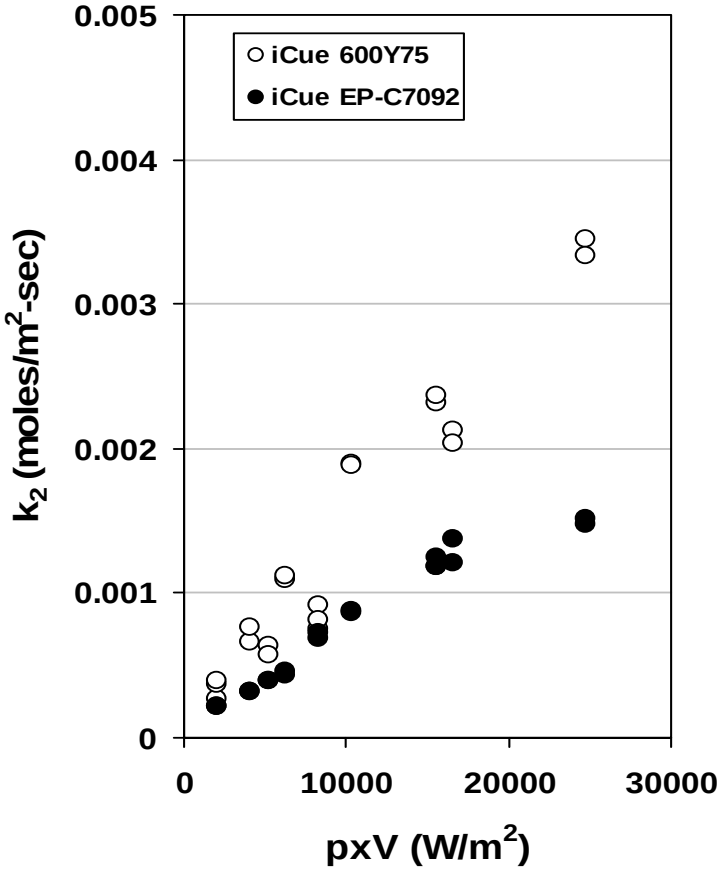
Task A – 4 – 1
Fluid Dynamics and Tribology of CMP

Mechanical Rate Constant – k2

120 ml per minute



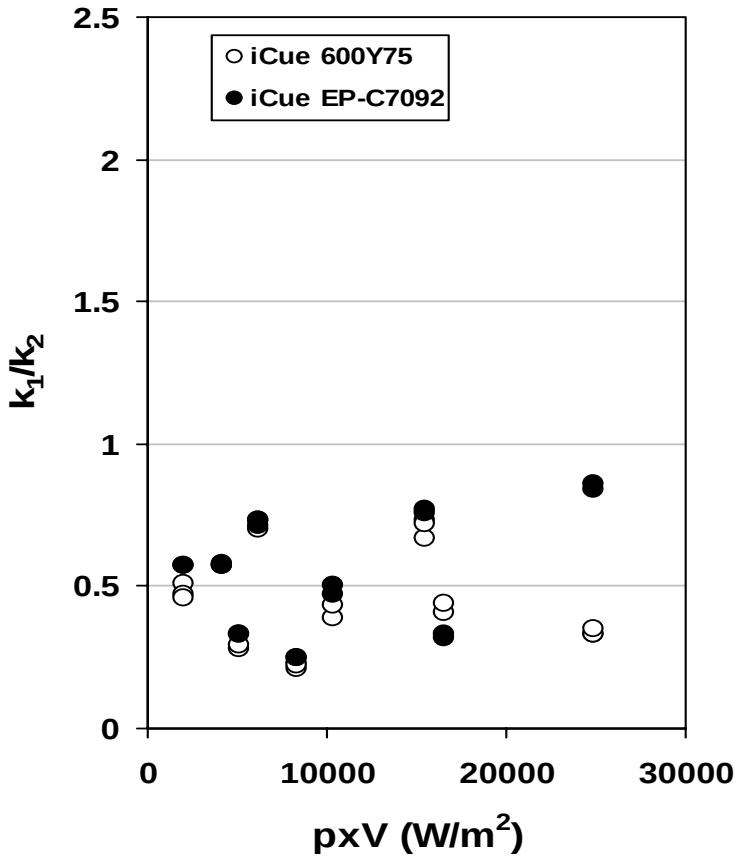
200 ml per minute



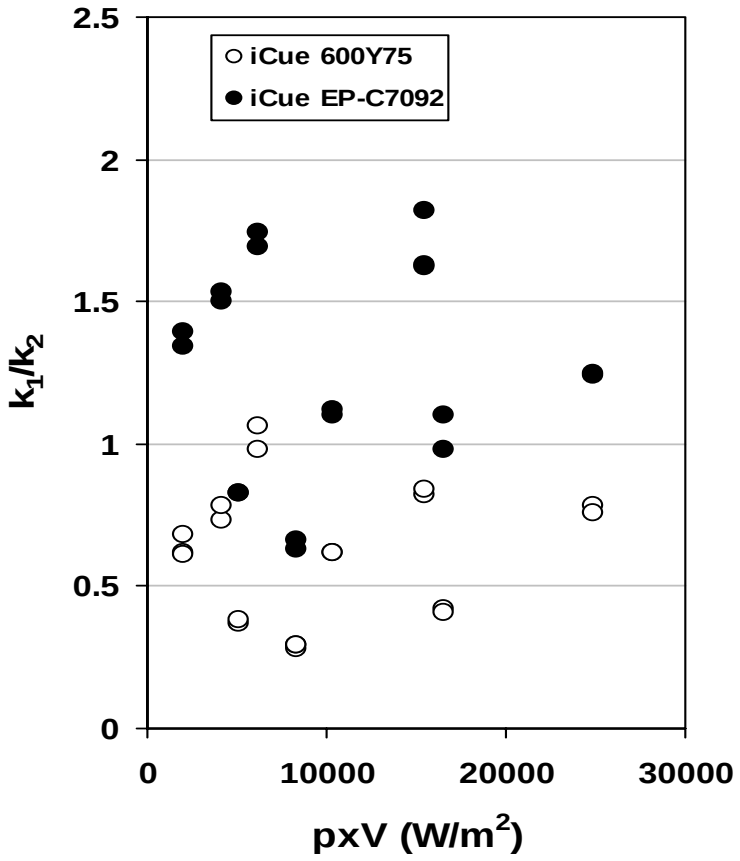
Task A – 4 – 1
Fluid Dynamics and Tribology of CMP

Chemical vs. Mechanical Action

120 ml per minute

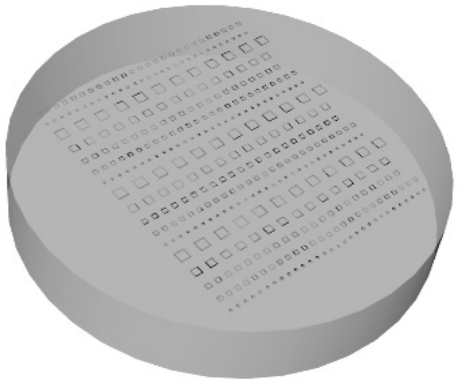


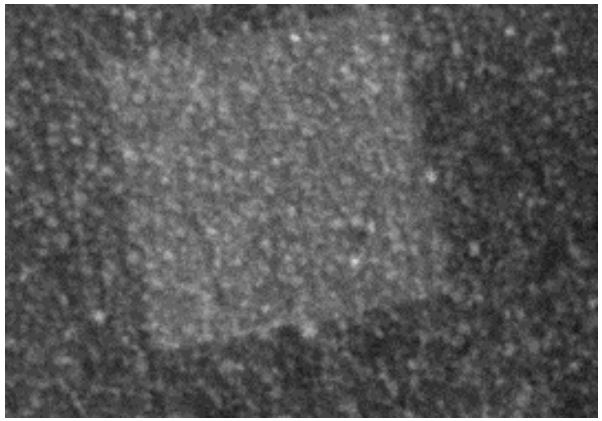
200 ml per minute

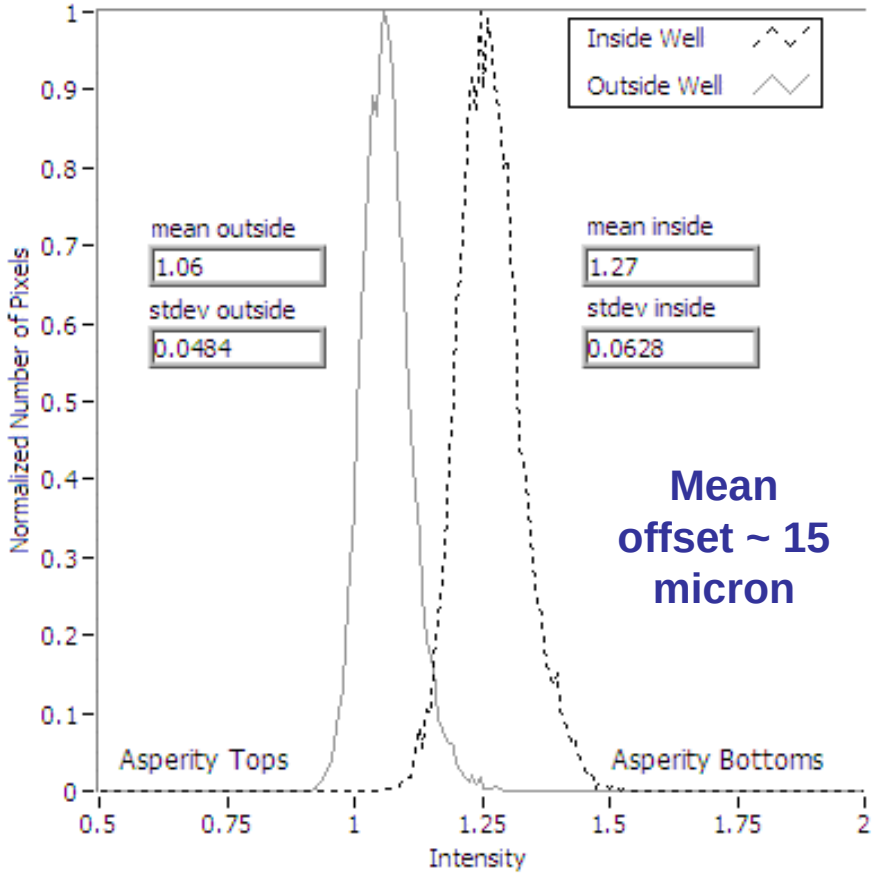


Task A – 4 – 1
Fluid Dynamics and Tribology of CMP

In-Situ Thickness Measurement using DELIF on Wafers with 18-micron Etched Wells



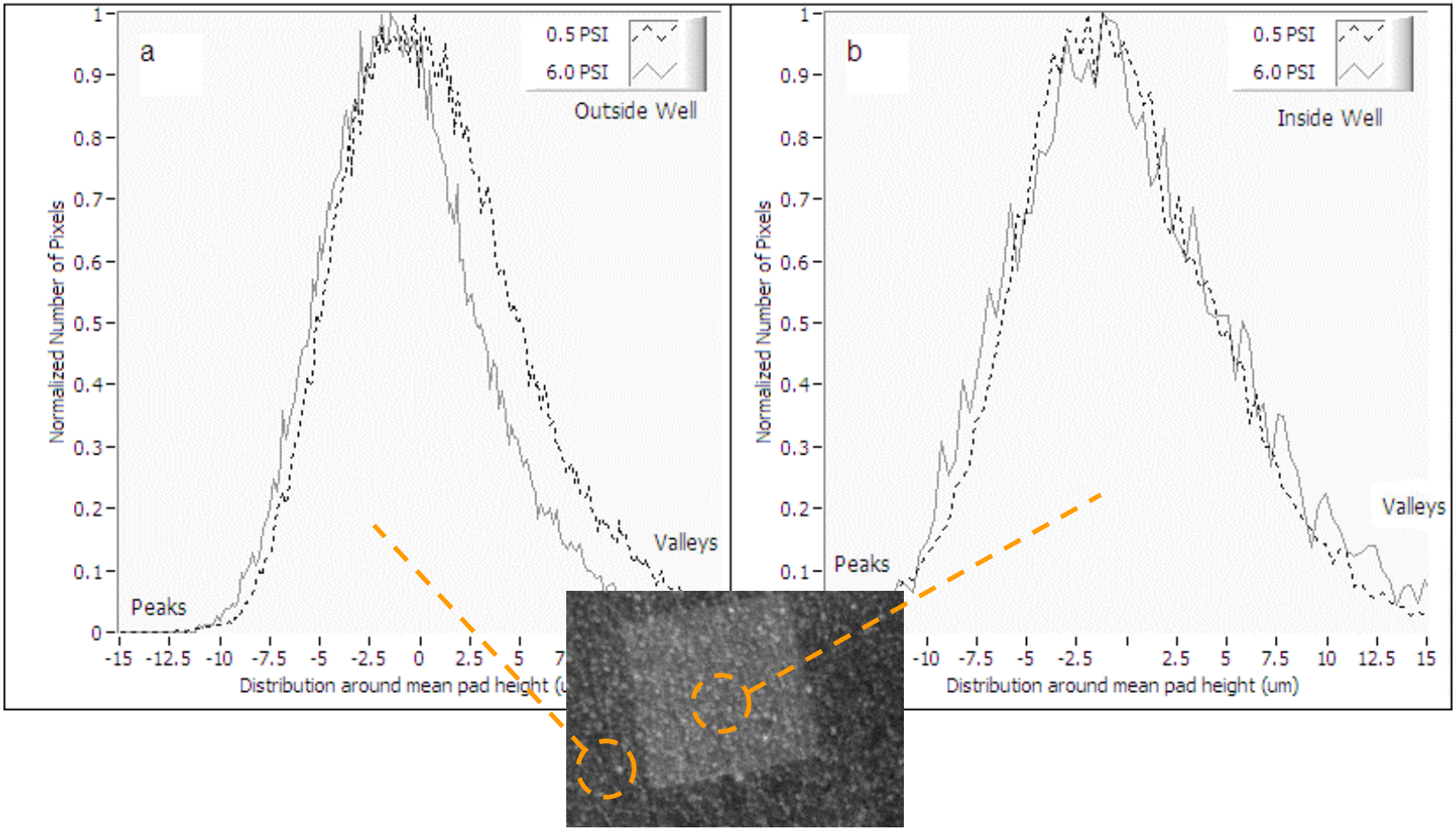




Mean offset ~ 15 micron

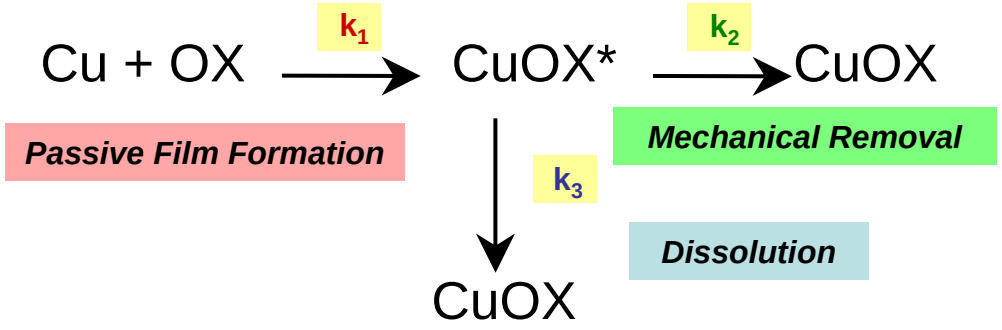
Task A – 4 – 1
Fluid Dynamics and Tribology of CMP

Slurry Thickness in the Wafer – Pad Region as a Function of Wafer Pressure (0.5 vs. 6.0 PSI) … u = 0.34 m/s



Task A – 5
Fundamental Pad Characterization

2nd Generation Kinetics Model



$$k_1 = \frac{\rho_{ox}}{MW_{ox}} N\Omega f \exp\left(\frac{-W}{kT}\right)\exp\left(\frac{qa}{2kTx}V\right)$$

$$RR = \frac{M_w}{\rho}\frac{k_1(k_2+k_3)}{k_1+k_2+k_3}$$

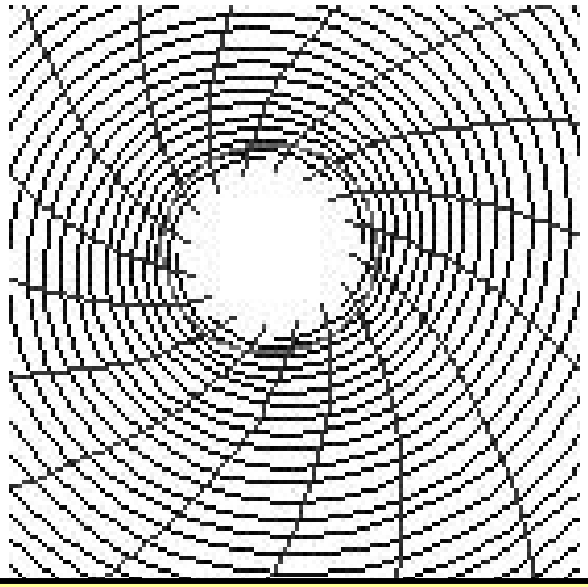
$$k_2 = c_p \mu_k pV$$

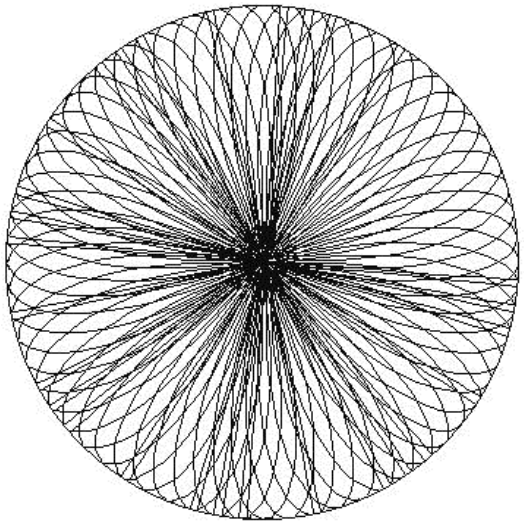
$$k_3 = \frac{-A\exp\left(-\frac{E_a}{RT}\right)}{(x_C - X)}$$

Dissolution rate (k_3) can be significant as *pressure x velocity* approaches zero

Task A – 5
Fundamental Pad Characterization

New Pad Designs … Logarithmic Spiral & Floral





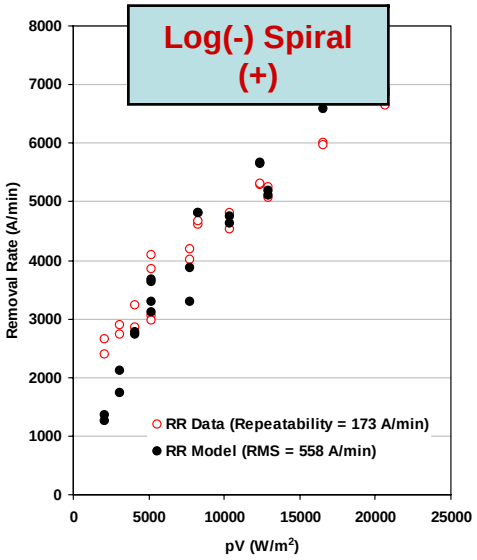
Basic Idea …

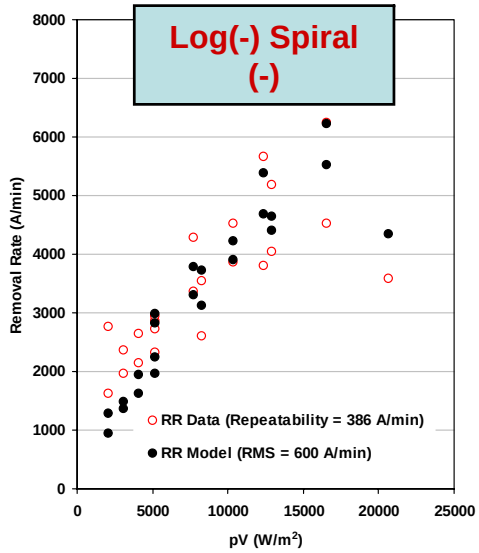
Positive Log. and Spiral Grooves
Transport fresh slurry into the pad – wafer interface

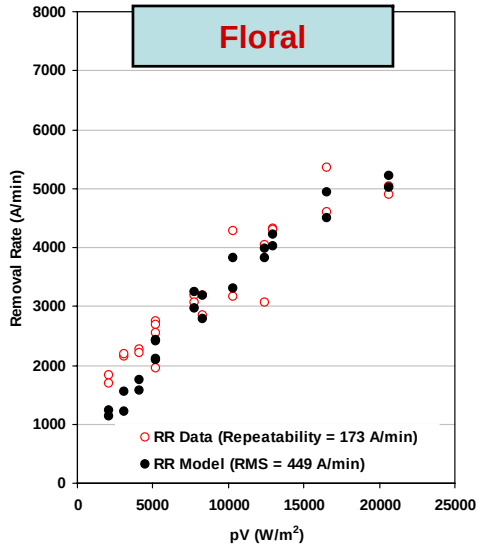
Negative Log. and Spiral Grooves Discharge spent slurry and by – products away from the pad – wafer interface

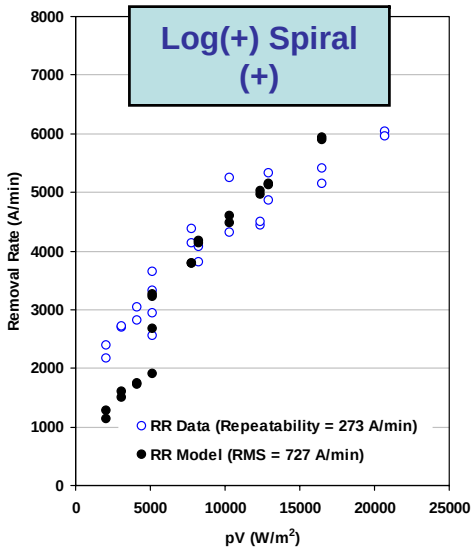
Wafer and pad (i.e grooves) rotate in the counter-clockwise direction

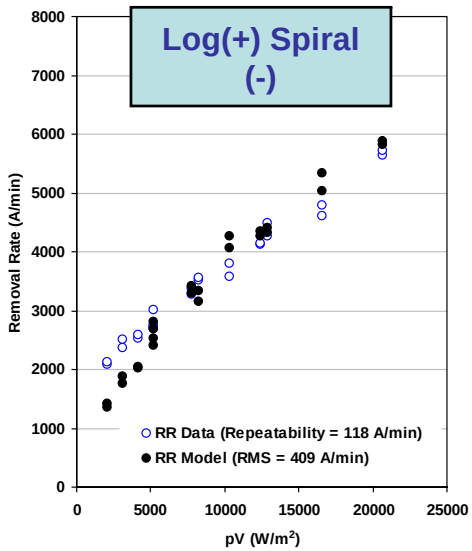
Task A – 5
Fundamental Pad Characterization

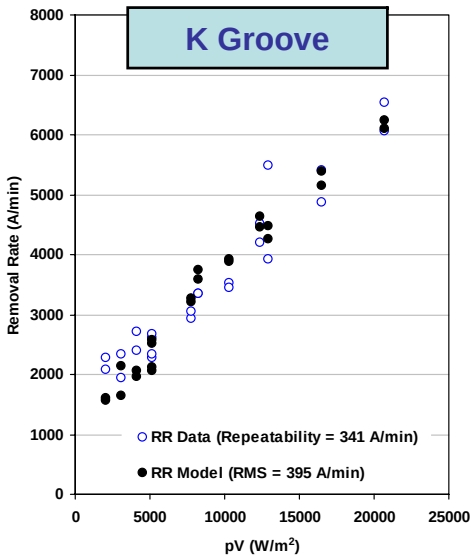




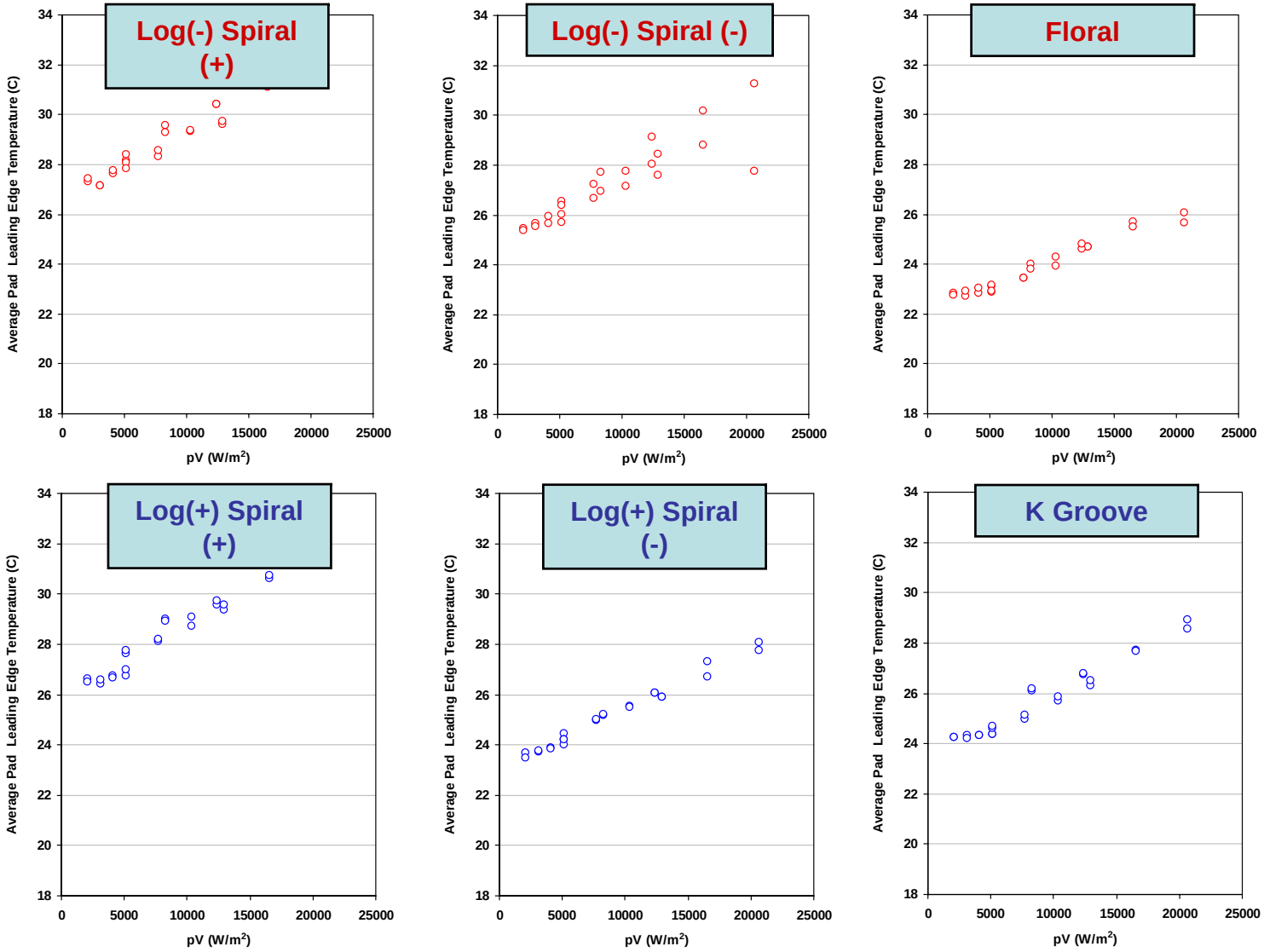




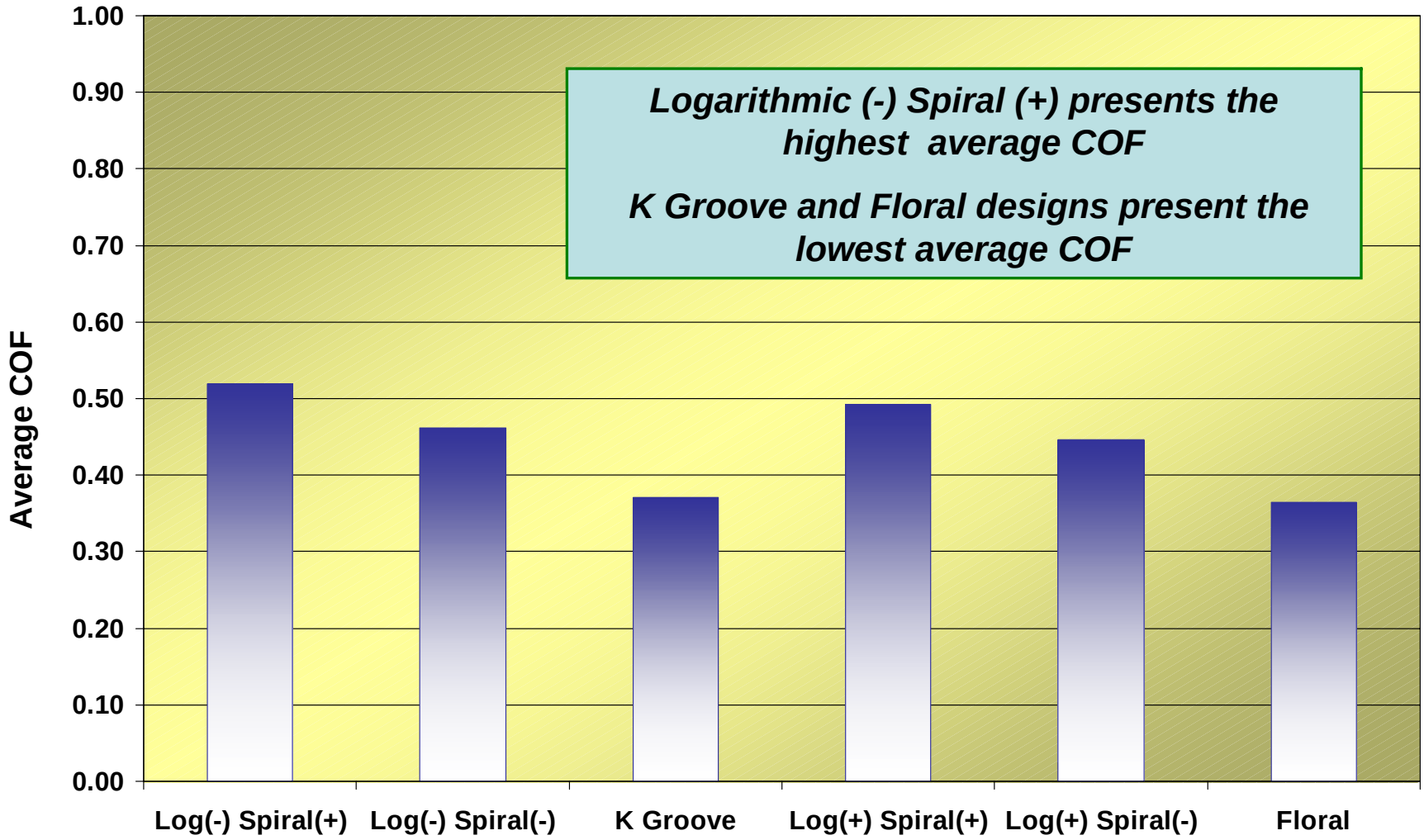




Task A – 5
Fundamental Pad Characterization



Task A – 5
Fundamental Pad Characterization



Task A – 5
Fundamental Pad Characterization

Misconception about COF and ULK Delamination

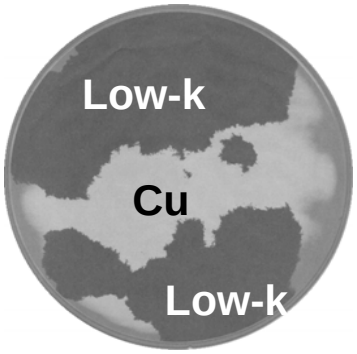
$$COF_{avg} = \frac{\overline{F}_{Shear}}{F_{Normal}}$$

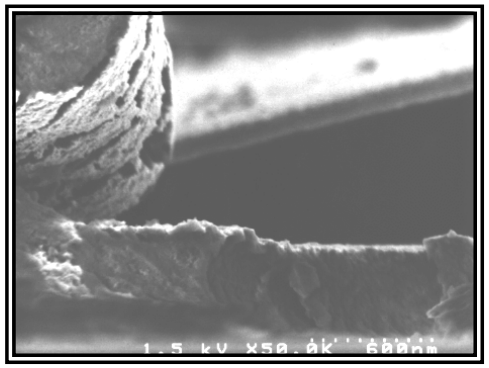
$$COF_{avg} \times F_{Normal} = \overline{F}_{Shear}$$

$$F_{Normal} \propto P_w$$

$$COF_{avg} \times P_w \propto \overline{F}_{Shear}$$

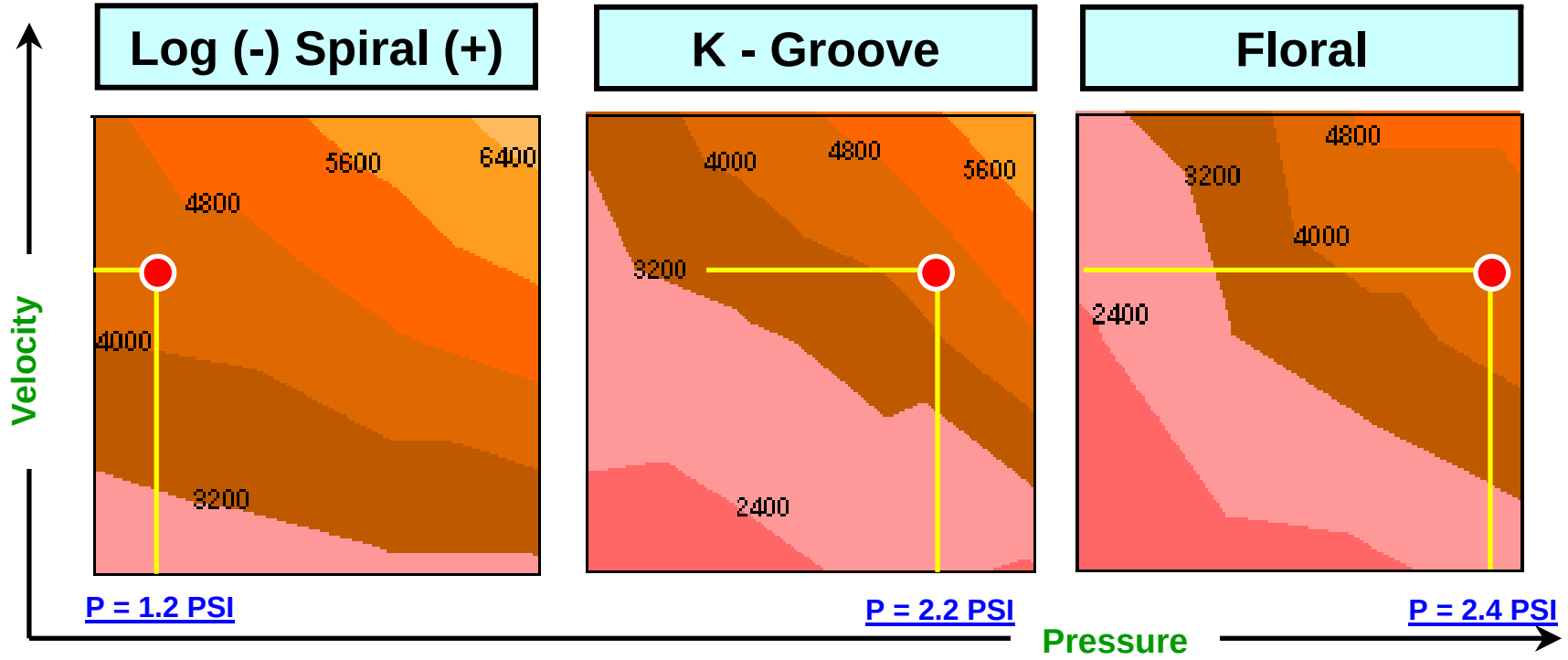
The photograph below and the SEM micrograph are courtesy of Hitachi Chemical





Task A – 5
Fundamental Pad Characterization

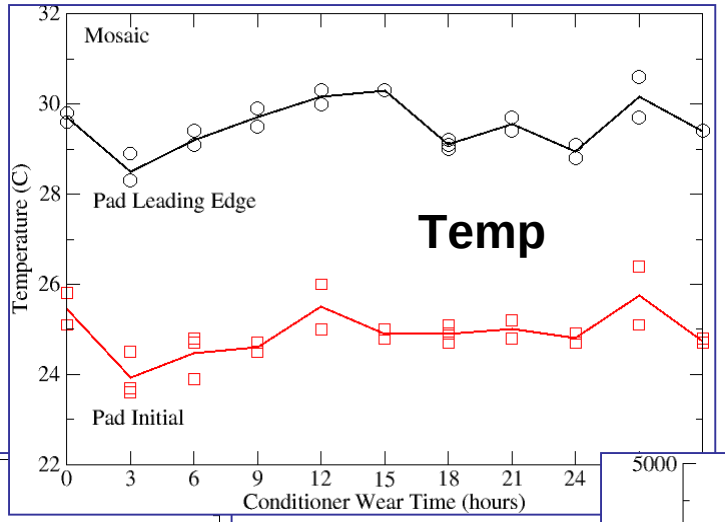
Power of Lim – Ashby Plots

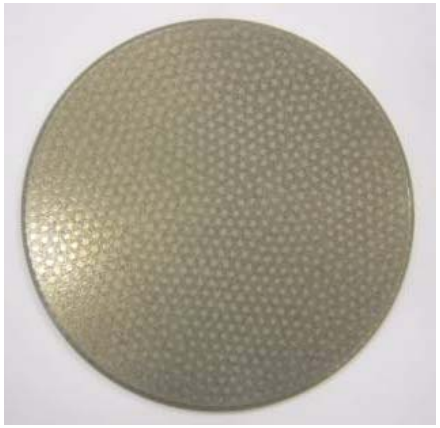


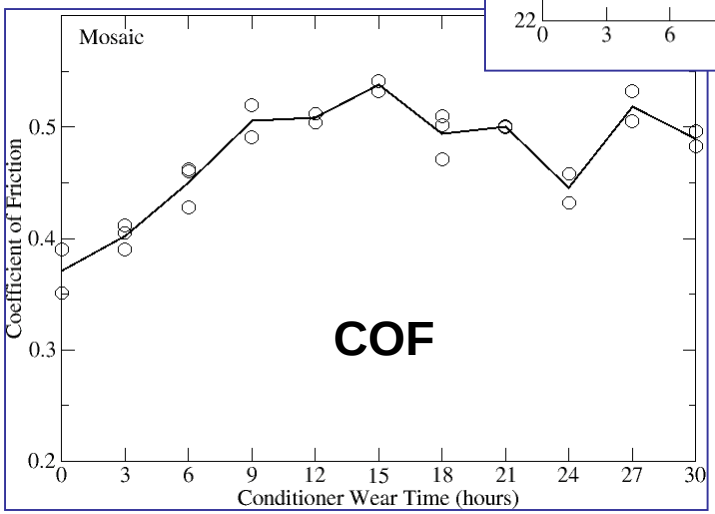
At a given RR, the Log (-) Spiral (+) is less dependent on P (at constant V)
This is an advantage in polishing ULK materials where low pressures are required

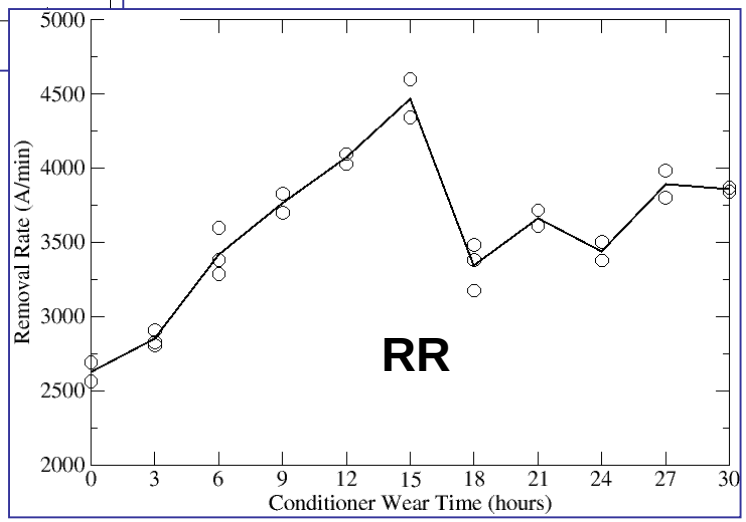
Task A – 8
Fundamental Characterization of Diamond Wear

COF, Temperature and Removal Rate are Tightly Correlated

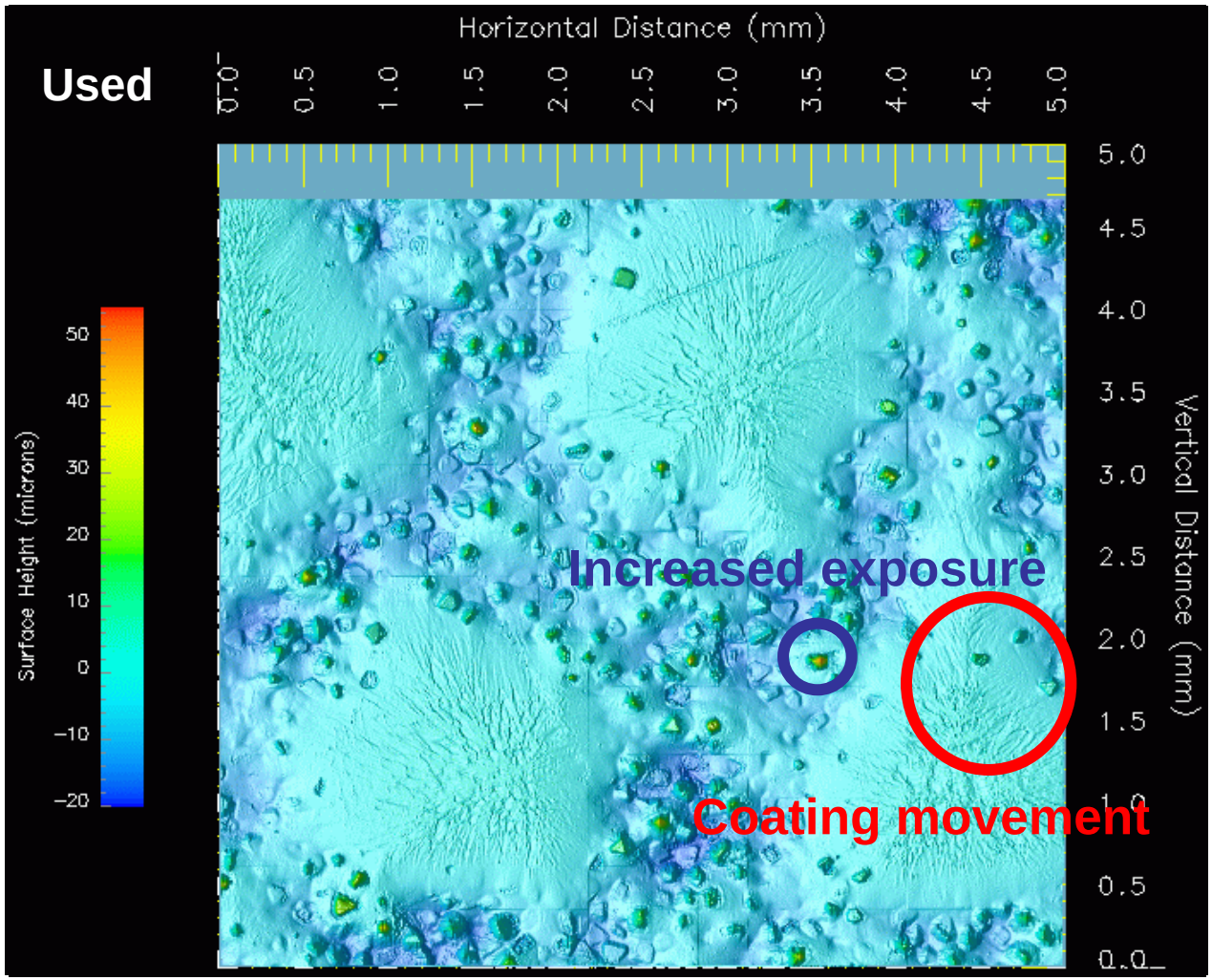






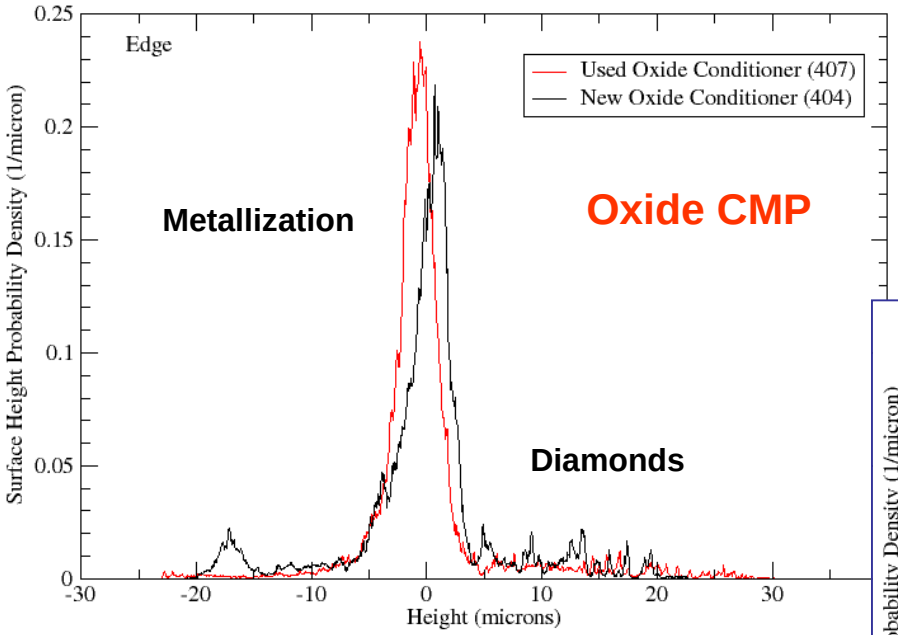


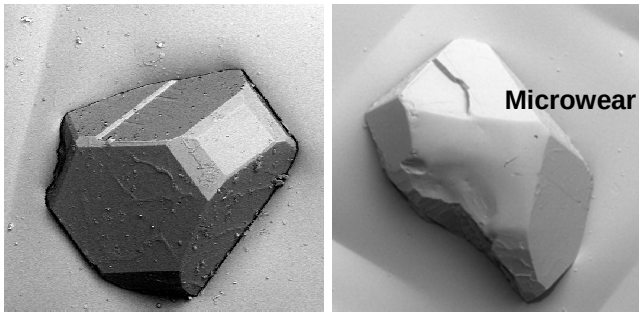
Task A – 8
Fundamental Characterization of Diamond Wear



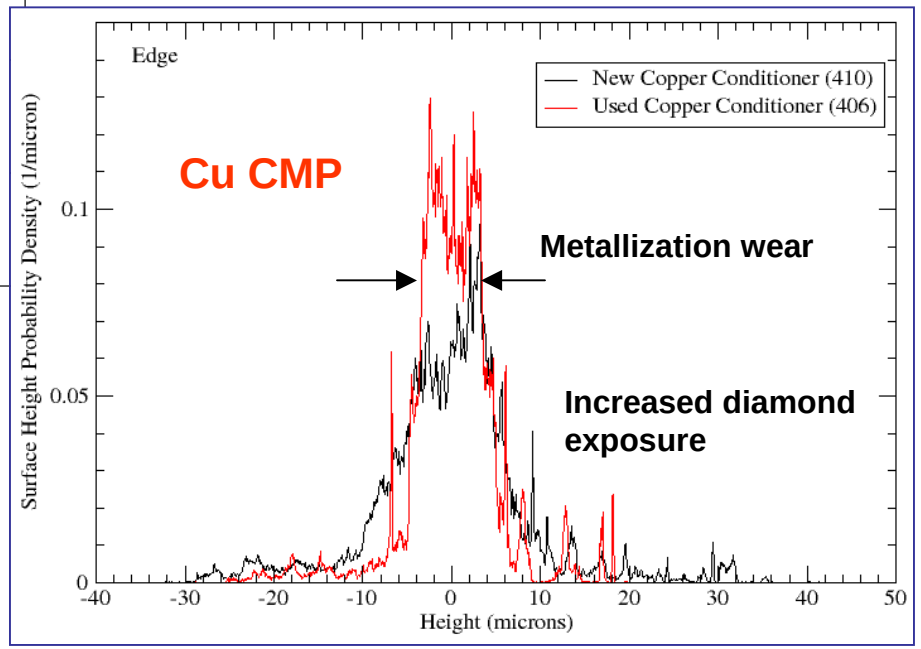
Task A – 8
Fundamental Characterization of Diamond Wear

New Vs. Used PDF Surface Height Comparisons



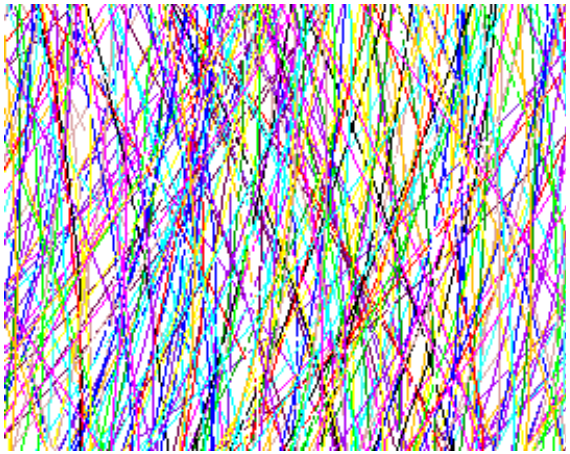


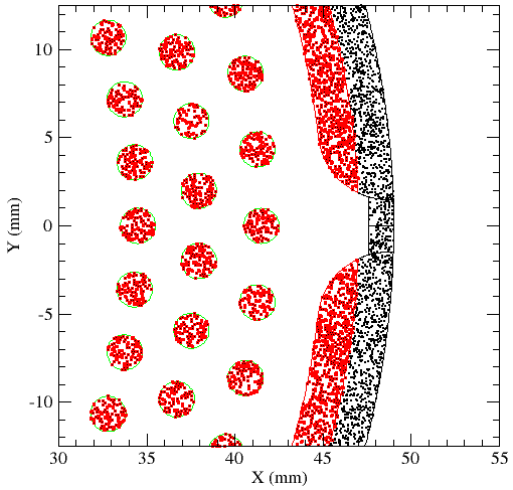
New Used

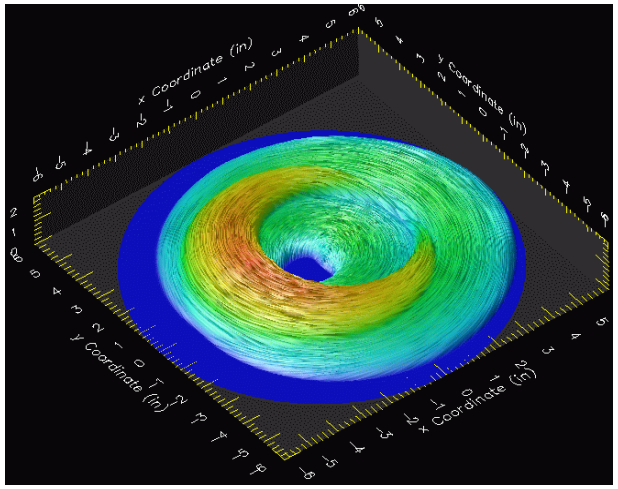


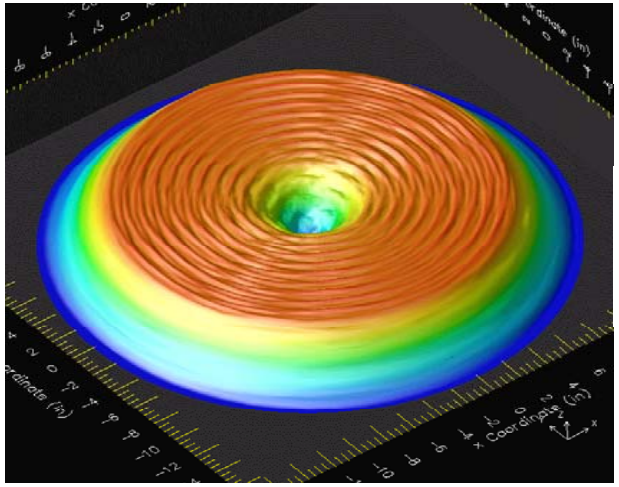
Task A – 8
Fundamental Characterization of Diamond Wear

Monte Carlo Simulation of Conditioning



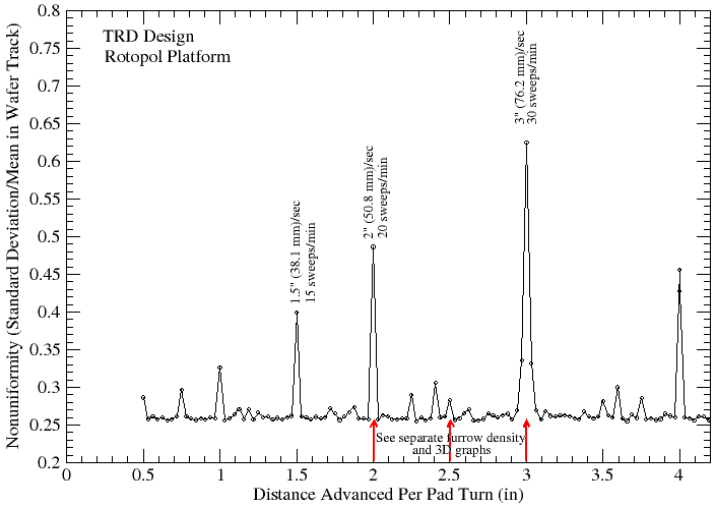


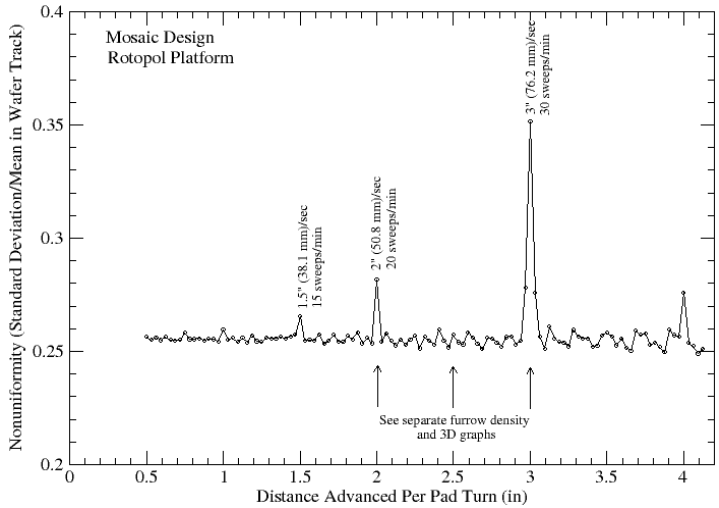


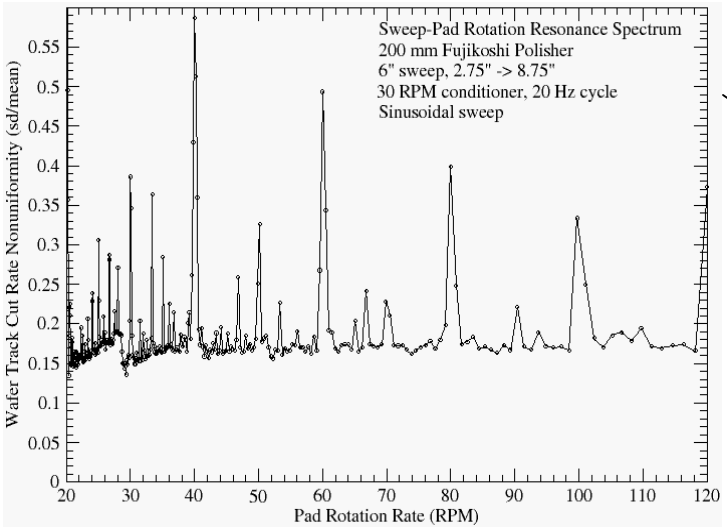


Task A – 8
Fundamental Characterization of Diamond Wear

Conditioning Uniformity Resonance Plots



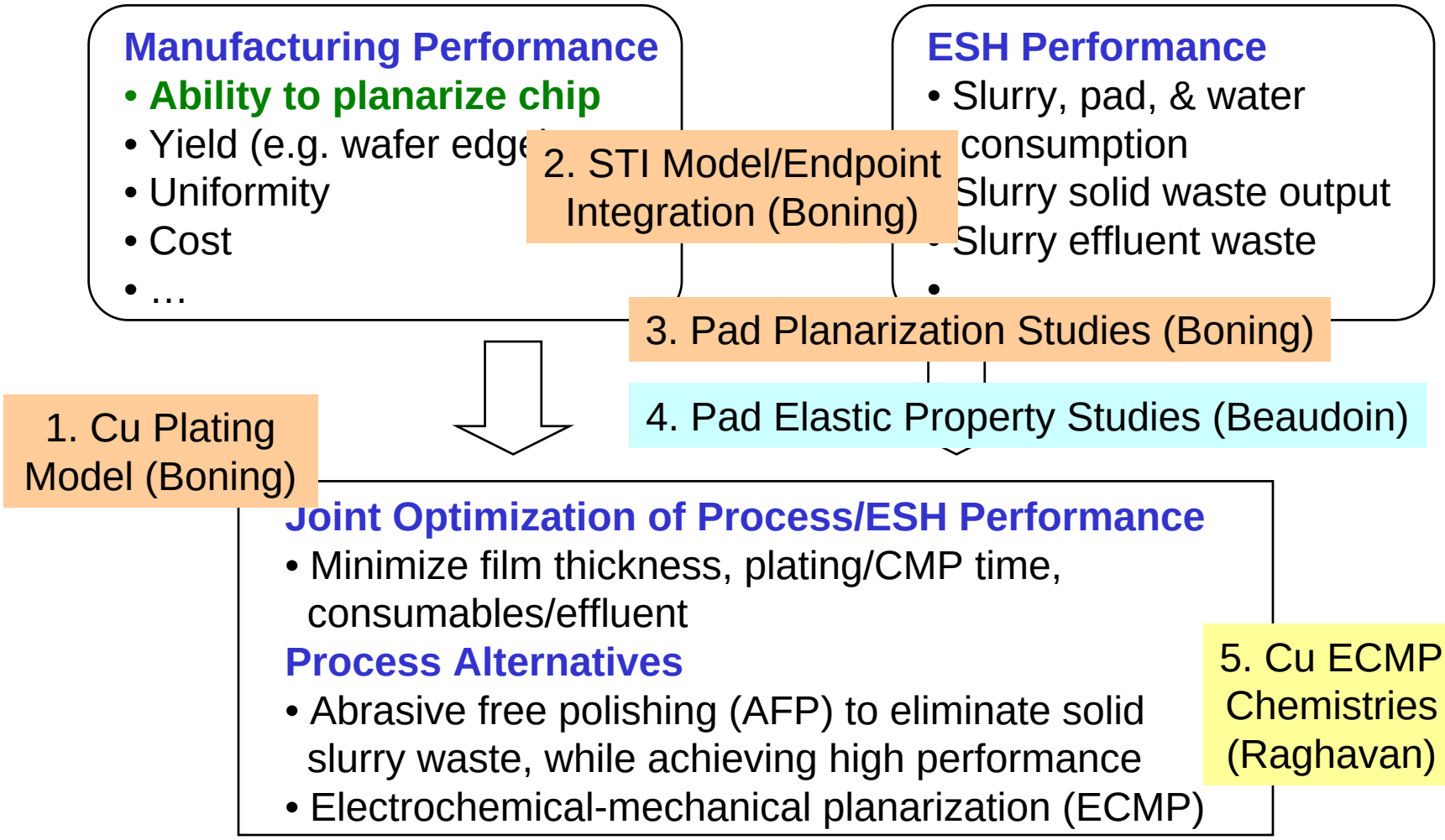




Different conditioners on same polisher

Same conditioner on different polishers

Planarization Modeling and Optimization

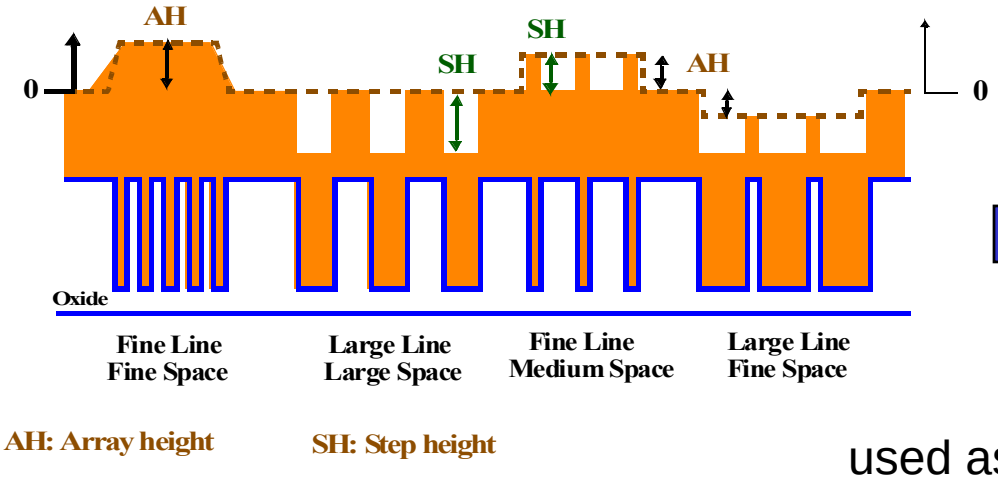


Planarization Modeling and Optimization
(Tasks A4-1 and A6-3)

- Faculty:
  - Prof. Duane Boning, MIT
- Students:
  - Hong Cai, PhD Candidate, MIT Mat. Sci. and Eng.
  - Daniel Truque, SM Candidate, MIT EECS
  - Xiaolin Xie, PhD Candidate, MIT Physics
- Research Objectives:
  - Process models to minimize slurry, pad, and water in CMP processes, with emphasis on pattern dependent effects in copper and shallow trench isolation (STI) CMP
  - Understand and optimize interactions between copper electroplating and planarization
  - Modeling for alternative pads, slurries, and processes (ECMP)

1. Coupled Plating and Planarization

ELECTROPLATING:

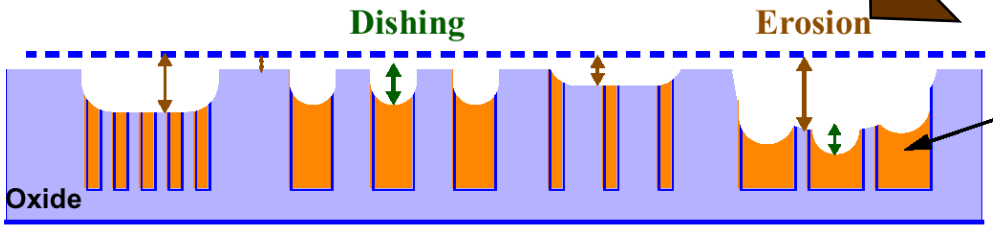


Plating Model Output:

Map across chip of
- array heights
- step heights

used as input to CMP model

COPPER CMP:



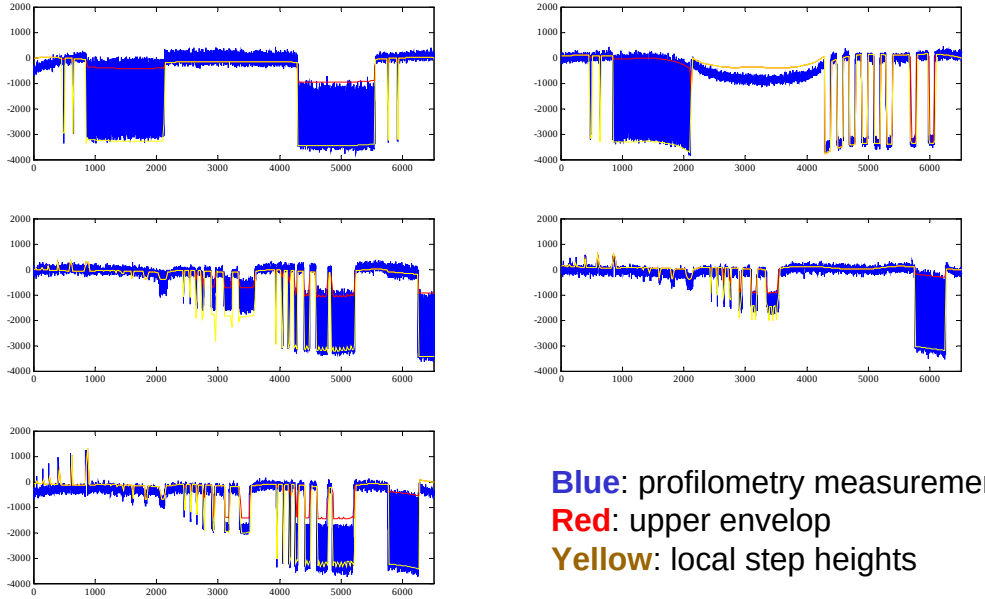
CMP Model Output:

Map across chip of
- dishing of copper
- erosion of dielectric

New Development: Time-Stepping Plating Model

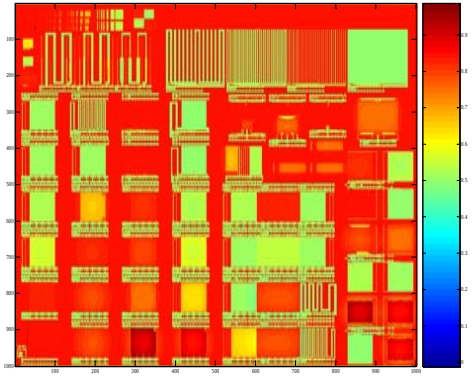
- Goals:
  - Jointly design/optimize the plating/CMP process
  - Requires model of thickness and time dependencies
  - Improve plating model accuracy
- Approach: Approximate geometric model
  - Drawing from *feature-scale* physical models
  - Modifications to achieve *chip-scale* modeling ability and efficiency

Plated Structures – Profilometry Scans (Å)



Blue: profilometry measurements
Red: upper envelop
Yellow: local step heights

Thickness (Å)



Chip-Scale Plating Simulation

2. STI Model/Endpoint Integration

- Endpoint detection needed in STI CMP
  - Reduce polish time/consumption; reduce dishing/erosion
- Objective: to understand and model friction force evolution during CMP, and relate to motor current signal
- Model Assumption: Friction proportional to
  - Topography roughness
  - Coefficient of friction for different %areas exposed during topography evolution
- Approach:
  - Patterned wafer CMP model calibrated with polished wafer measurements
  - Wafer surface evolution is predicated with the calibrated CMP model
  - Friction is estimated with friction model
- Experiments:
  - Different STI processes/ceria slurries
    - Different oxide/nitride coefficient of friction ratios

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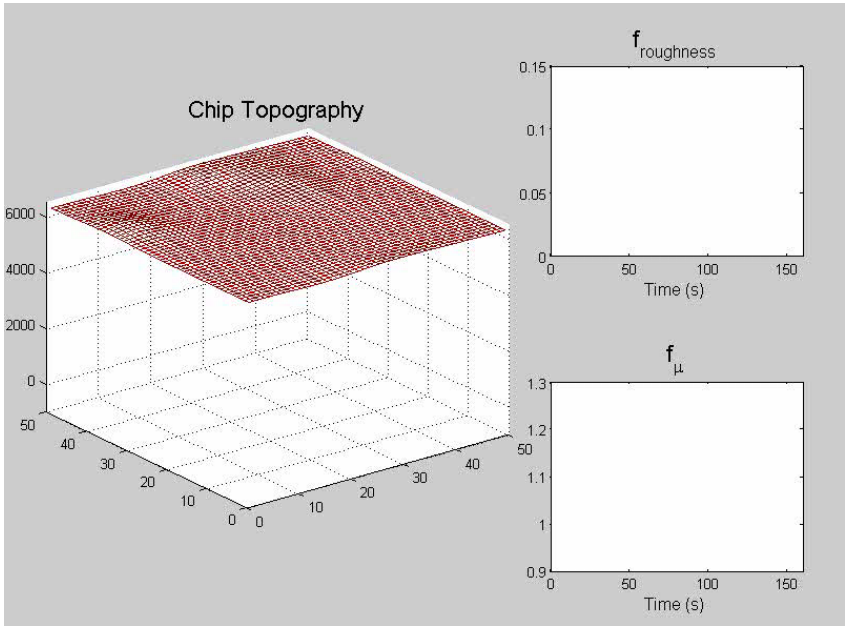
  - Reduce polish time/consumption; reduce dishing/erosion
- Objective: to understand and model friction force evolution during CMP, and relate to motor current signal
- Model Assumption: Friction proportional to
  - Topography roughness: $f_{roughness}$
  - Coefficient of friction for different %areas exposed during topography evolution: f_{μ}



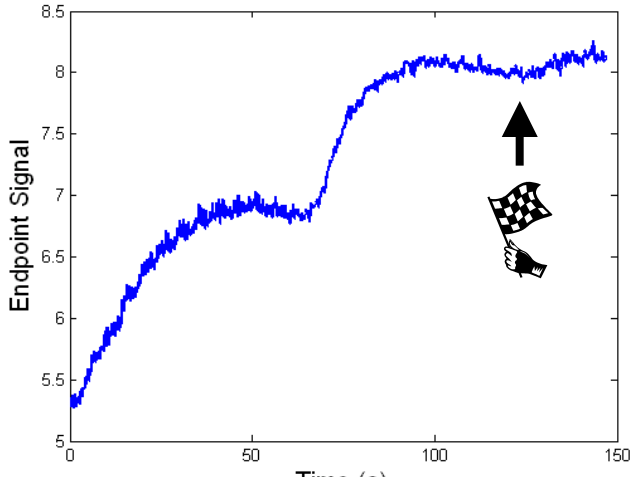
- Approach:
  - Patterned wafer CMP model calibrated with polished wafer measurements
  - Wafer surface evolution is predicated with the calibrated CMP model
  - Friction is estimated with friction model
- Experiments:
  - Different STI processes/ceria slurries
    - Different oxide/nitride coefficient of friction ratios

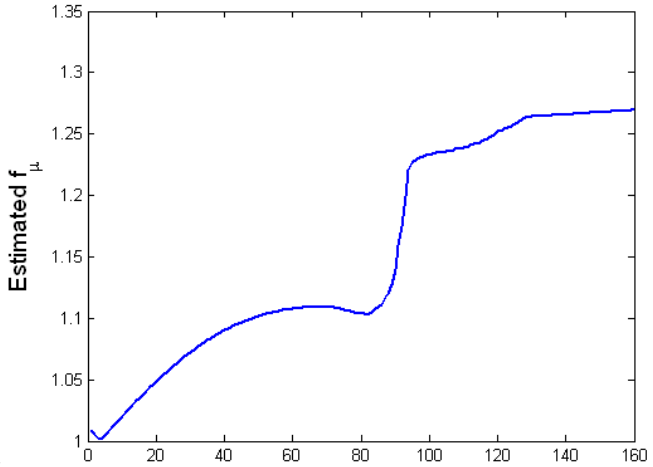
Comparison: Measured vs. Simulated Friction

Measured Motor Current

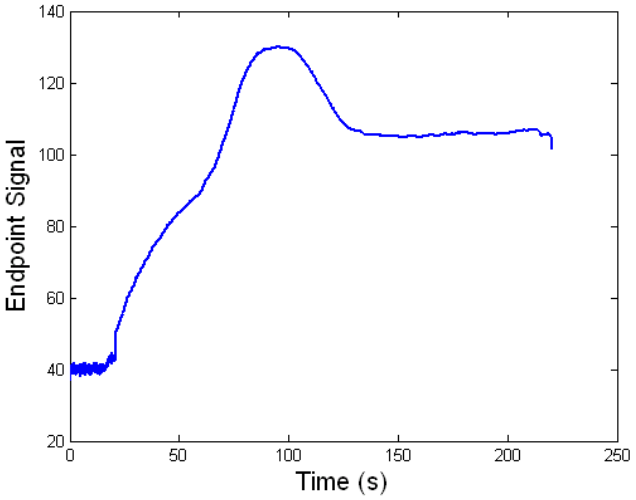
Predicted Friction

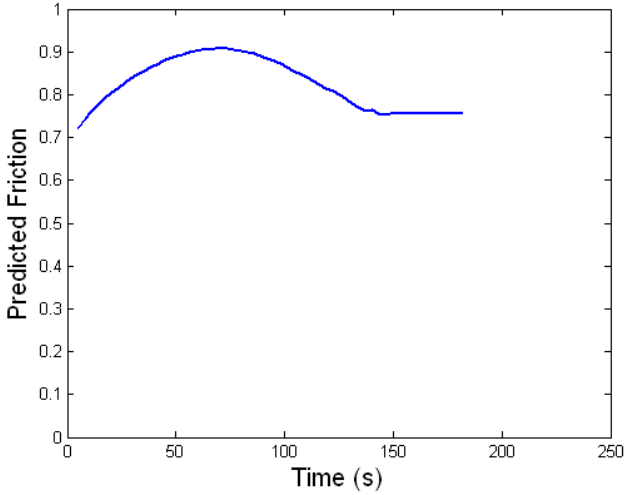
Process 1





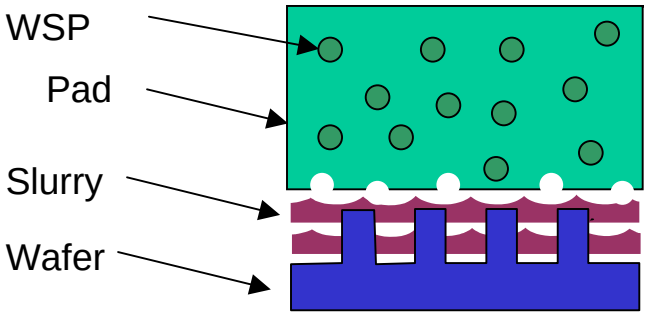
Process 2



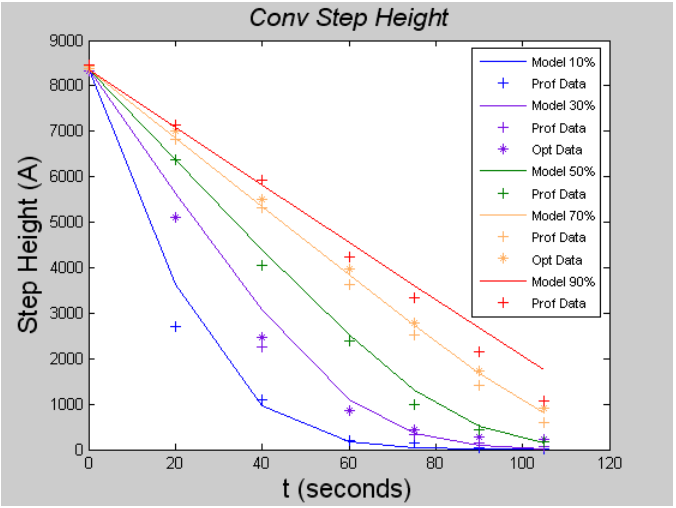


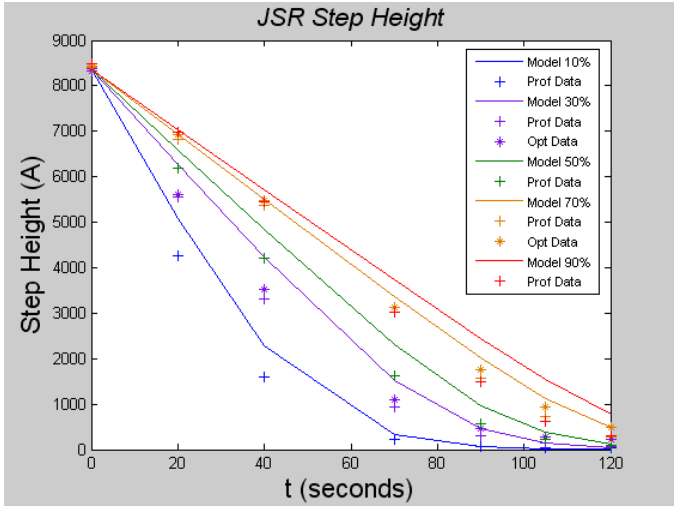
3. Pad Planarization Performance Modeling

Novel Pad with Water Soluble Particles (WSP)



- **Goal:** Understand how pad parameters, such as stiffness, pore size and distribution, relate to pad planarization performance
- **Observations**
  - ❑ Both pads polish low pattern density areas faster than high pattern density areas
    - Fundamental pattern density dependency
  - ❑ Novel pad exhibits *less* pattern dependency
    - a smaller spread in the times required to planarize 10% and 90% pattern density structures



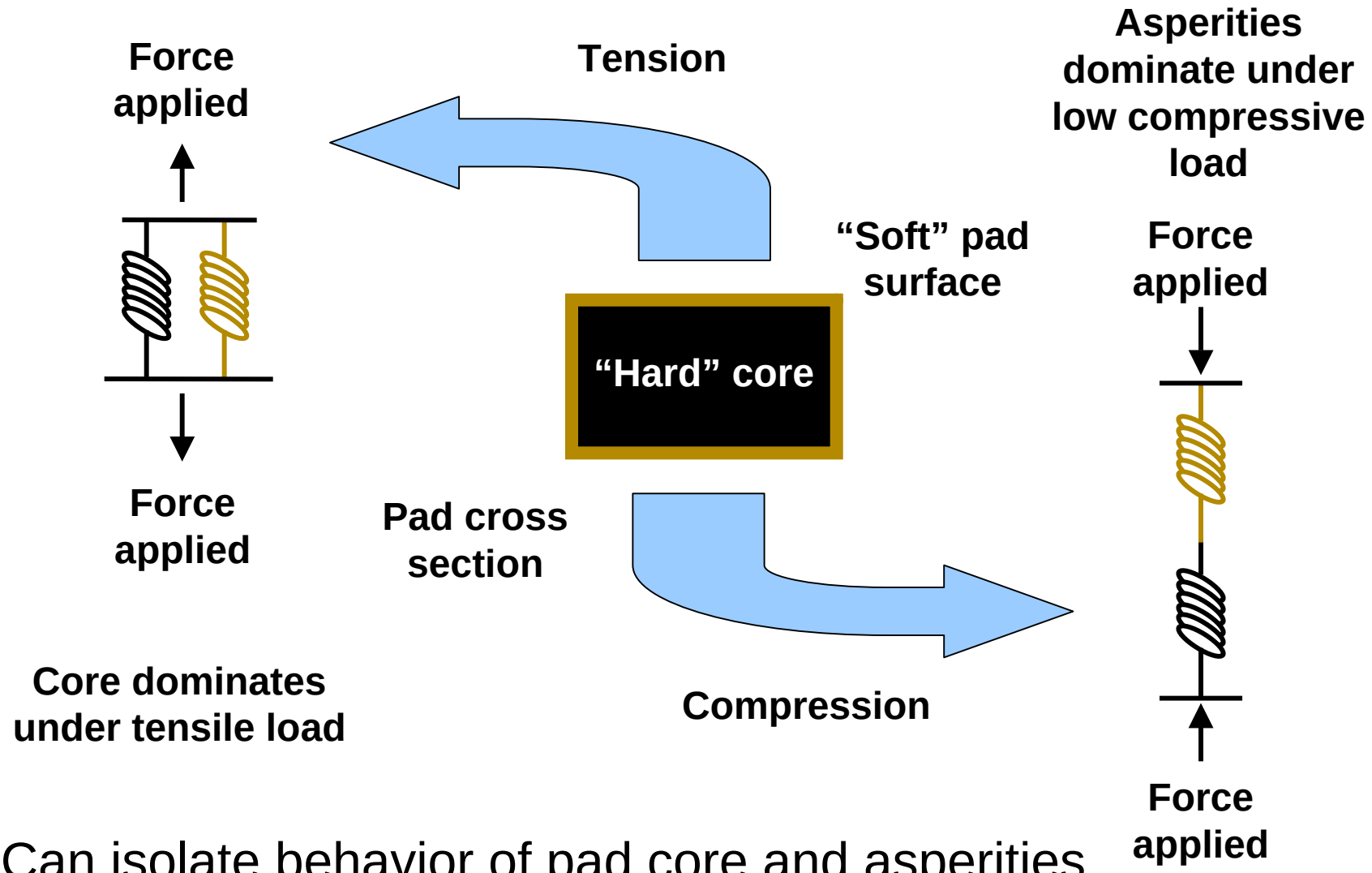


Collaboration with JSR

Copper Planarization – Pad/Process Studies (Task A9)

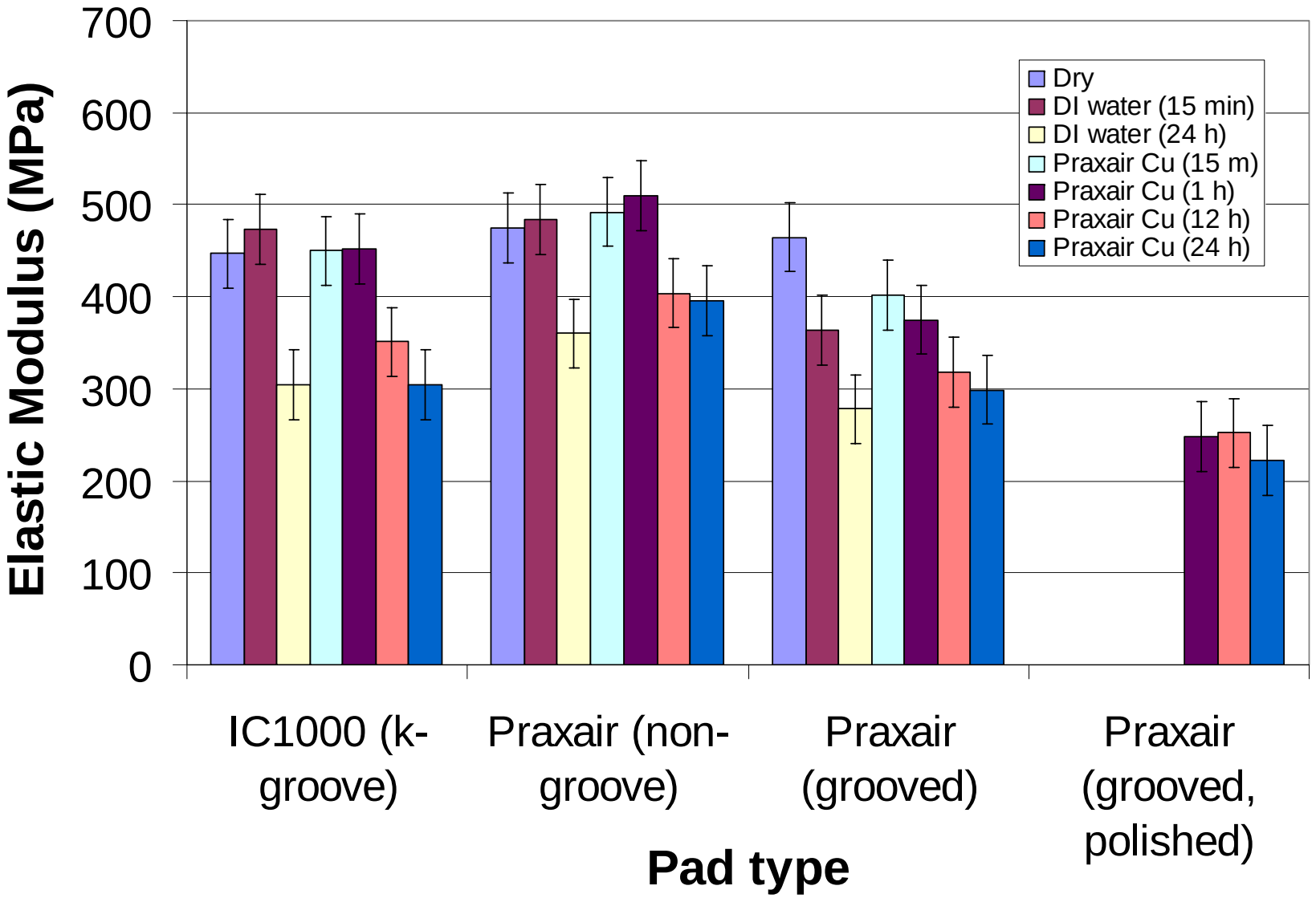
- Faculty:
  - Prof. Steve Beaudoin, Purdue Chemical Engineering
- Students
  - Bum Soo Kim, Purdue, Chemical Engineering
  - Caitlin Kilroy, Purdue, Chemical Engineering
- Research Objectives:
  - Overall: understand/optimize Cu CMP protocols to reduce energy, water and chemical usage
  - Recent focus: Methods to decouple/study pad bulk and surface asperity elastic modulus properties
  - Current focus: Connect pad/slurry properties to pad/particle/wafer interactions and to planarization performance
- Acknowledgments
  - State of Indiana 21st Century Fund; Praxair Microelectronics

Interpretation: Pad Elastic Modulus Studies

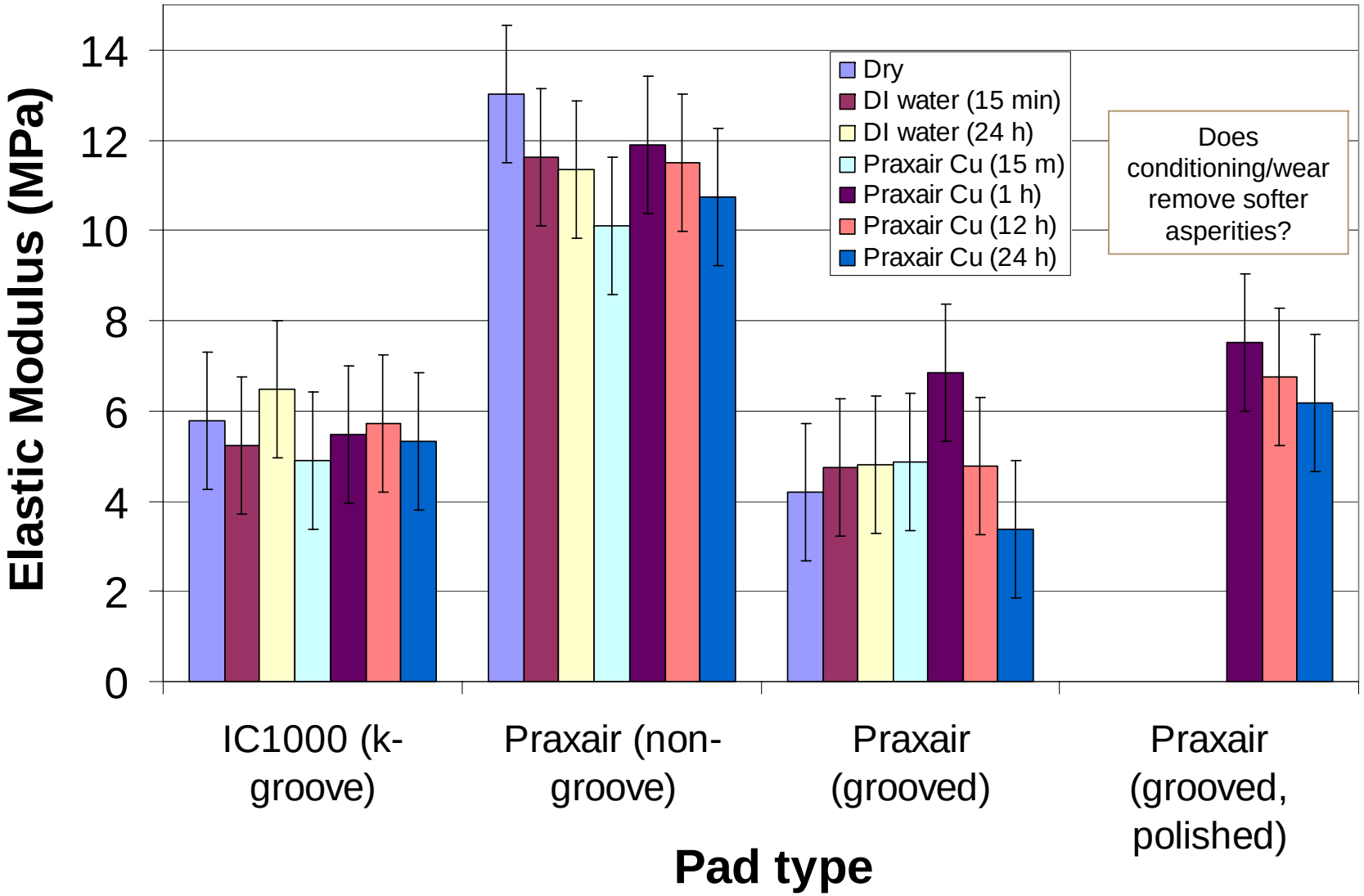


Can isolate behavior of pad core and asperities

Measured Elastic Modulus in Tension



Measured Elastic Modulus in Compression



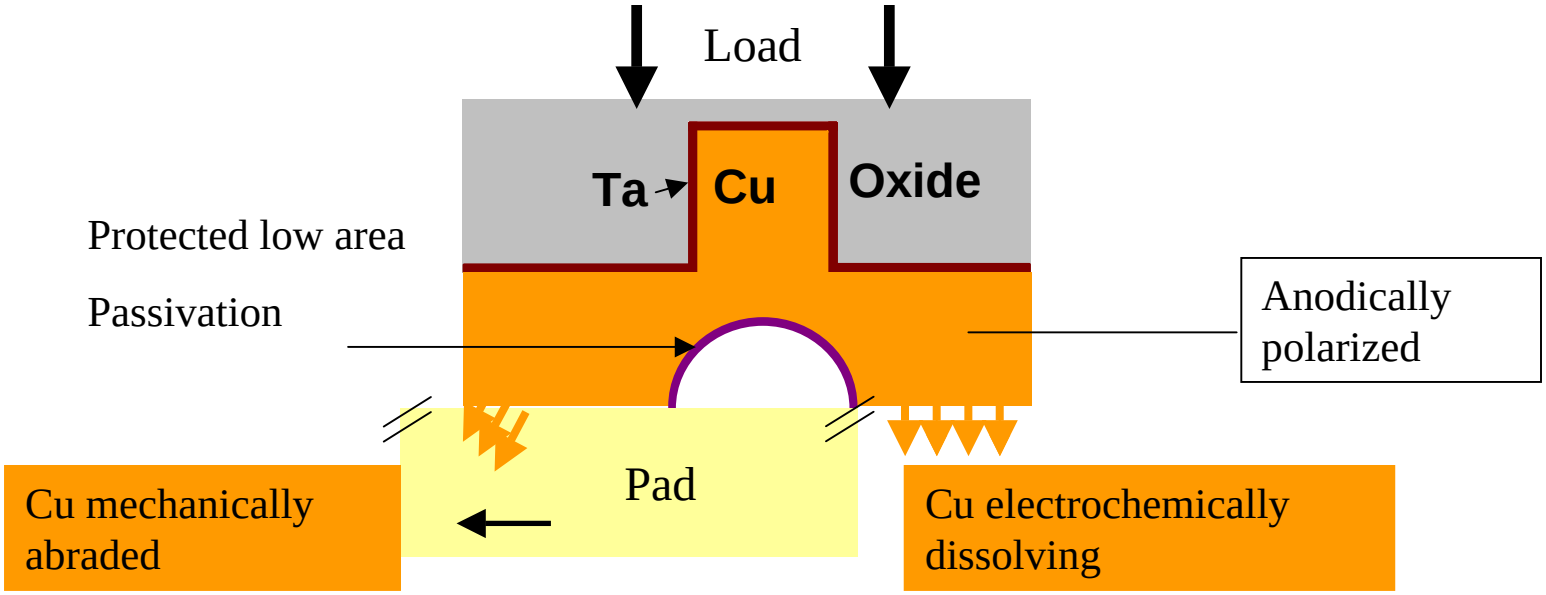
Interpretation: Pad Behavior

- Asperity layer and bulk pad studied
  - Effects of cyclical loading during CMP, soaking in slurries, and soaking in aqueous solutions studied
  - Asperity layer
    - Pad asperities undergo minor changes
    - Conditioning/polishing wear may increase effective modulus slightly
  - Bulk pad
    - Core region of pad becomes softer (lower modulus) with increased exposure to slurry, aqueous solution, or polishing
    - Polishing accelerates reduction in modulus
- Implications
  - Pad conditioning may influence load/asperity, but may not influence mechanical properties of individual asperities
  - Pad break-in periods may reflect combined evolution of pad bulk modulus and pad asperity contact area

Electrochemical Mechanical Planarization (ECMP) of Copper (Task A6)

- Faculty:
  - Prof. Srini Raghavan, U. Arizona, Materials Science & Engineering
- Students
  - Viral Lowalekar, U. Arizona, Materials Science & Engineering
  - Ashok Muthukumaran, U. Arizona, Materials Science & Engineering
- Research Objectives:
  - Develop chemical systems suitable for ECMP of copper through electrochemical investigations
    - Identify inhibitors that can function effectively under anodic potential
  - Reduction in abrasives use/output, reduced cost, and low pressure polish
- Key Accomplishments:
  - Developed oxalic acid based chemical system containing a redox inhibitor (TSA) that is suitable for copper ECMP
  - Characterized the mechanism of inhibition by electrochemical investigations

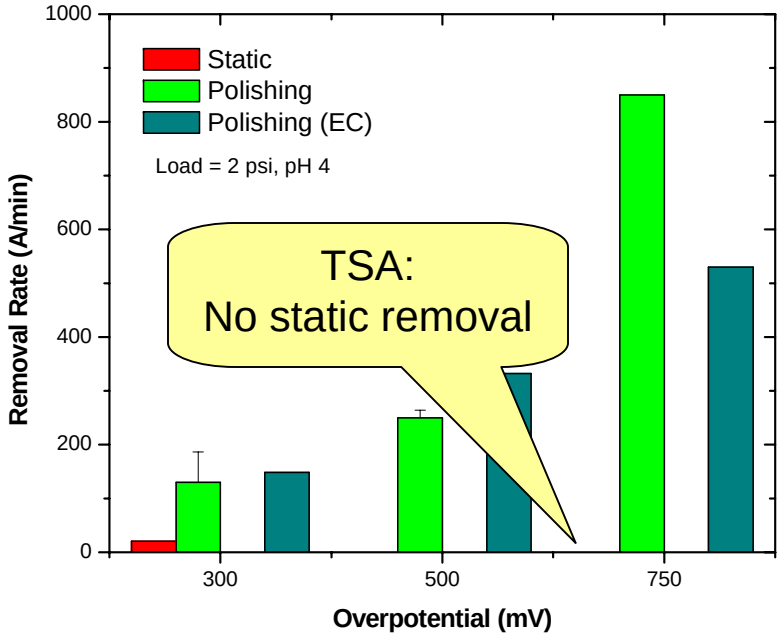
ECMP for Bulk Copper Removal

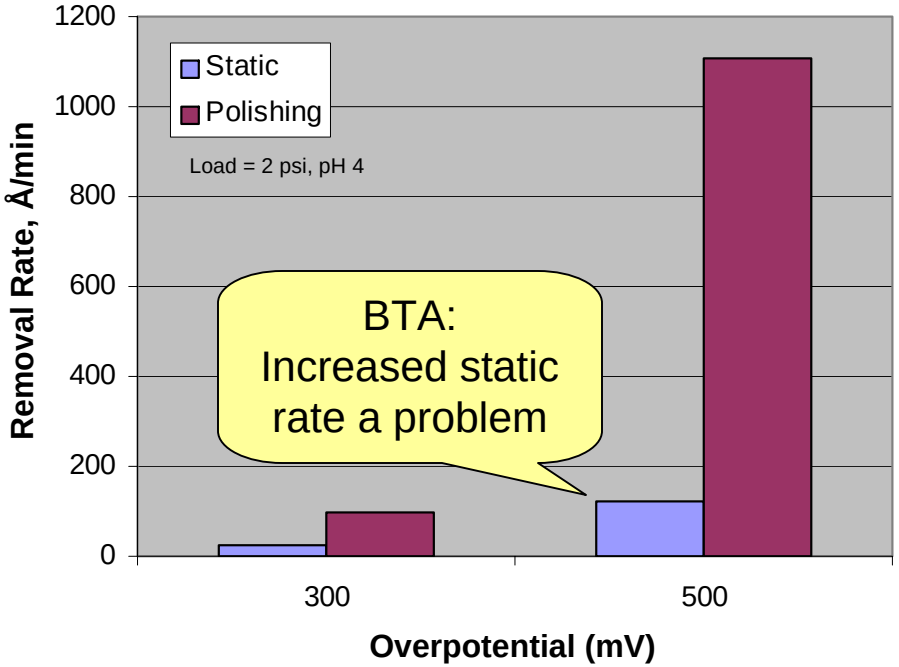


- Wafer is anodically biased during polishing in a solution at very low (~0.5 psi) pressure
- Passivating agent/corrosion inhibitor is added to protect low lying areas while higher areas are polished.
- Inhibitors must be stable at anodic overpotentials
  - **Efficiency of the most commonly used inhibitor BTA decreases with applied anodic potential**

ECMP of Copper in Oxalic Acid System - Comparison of TSA and BTA as Inhibitor

Removal rates determined by profilometry

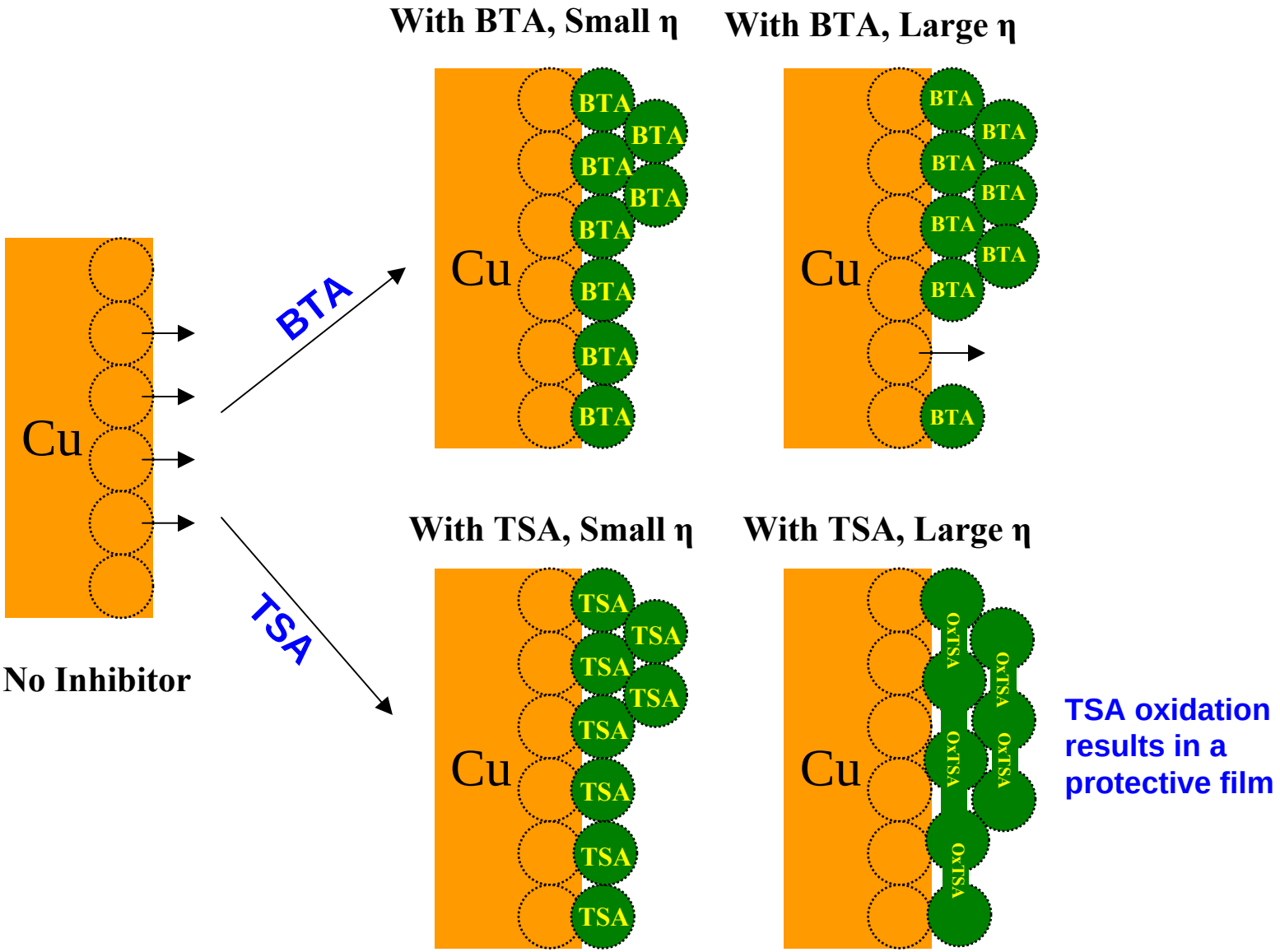




- 0.1 M Oxalic + 0.01 M TSA + 1% SiO_2
- Increase in overpotential increases Cu removal rates.
- *Unlike BTA*, no static removal seen at higher overpotentials.

- 0.1 M Oxalic + 0.001M BTA + 1%SiO_2
- Higher polishing and static removal rates with higher overpotential.

Proposed Inhibition Mechanism for BTA and TSA



Future Directions

- Continue work with redox inhibitors and study rate –planarity relationship
- Investigate the feasibility of removal of barrier layers (Ta, TaN, Ru) using ECMP technique.
  - 1:1 selectivity between Cu and barrier layer

The Means to Select New Materials and Devices Using ATDF at SEMATECH

Jeff Wetzel

jeff.wetzel@atdf.com

Manager, Emerging Technologies
Advanced Technology Development Facility

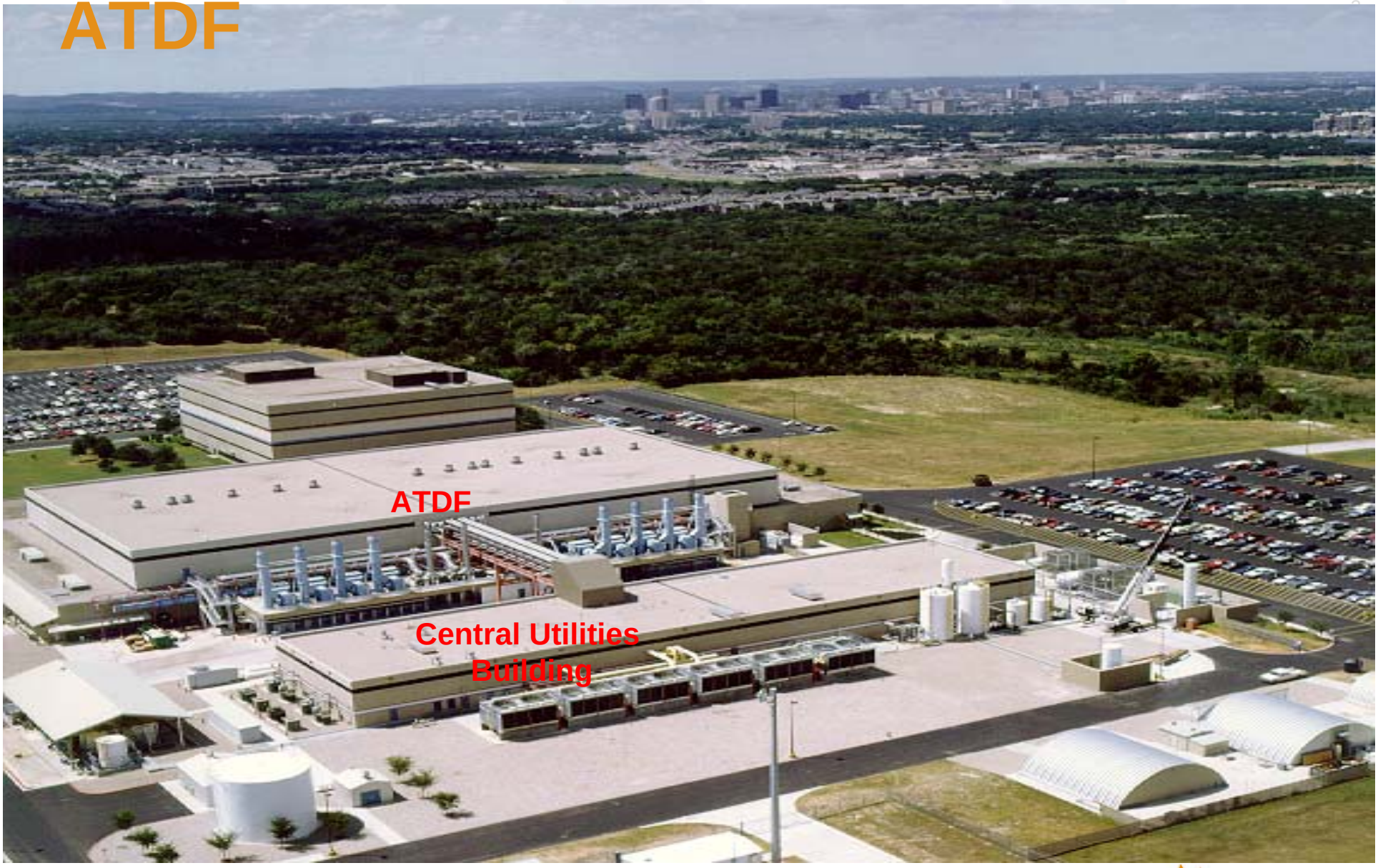
February 24, 2006

Where research meets manufacturing.

Outline

- ATDF Status in SEMATECH and Business Model
- Specific Examples
  - FEOL: Fermi-FET™
  - BEOL: Dual Damascene Imprint
- Summary

ATDF



Corporate Timeline

1988	SEMATECH founded
1996	I300I subsidiary started
1997	ATDF Test Wafer Services
1998	International members join
2001	BEOL Cu 300 mm capability
2003	First custom projects
	Customer can define own R&D program and protect developed IP
2004 (July)	**ATDF as independent for-profit subsidiary**

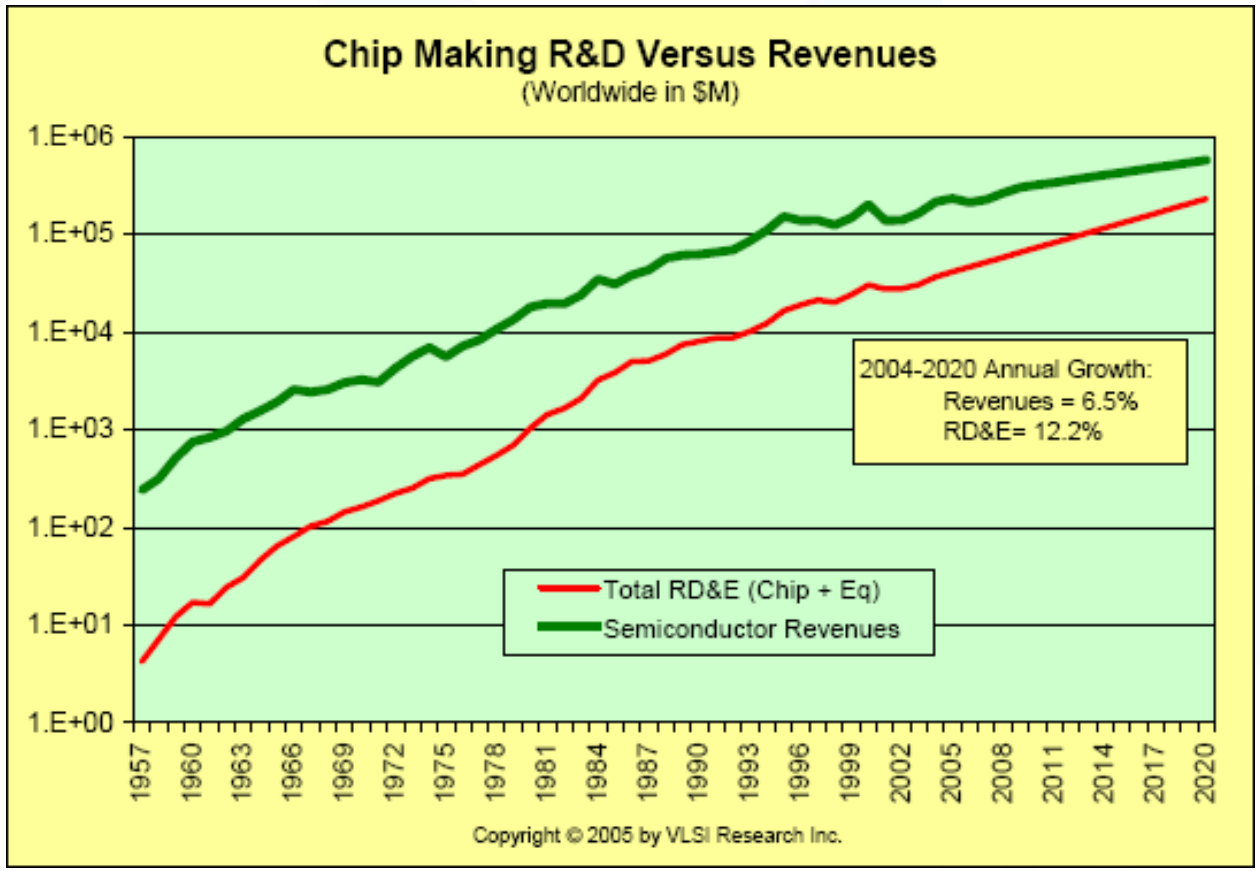
➔ ATDF is a SEMATECH-owned company with its own independent Board of Directors

Increase of R&D Cost

Many companies finding the traditional collaboration methods NOT worth the effort

- **R&D&E costs increasing at almost 2X the revenue rate**
- **300 mm R&D very expensive**
- **"Need new ways to make R&D more efficient…"**

D. Hutcheson (VLSI Research)



➢**R&D foundry is one solution, where chip makers and suppliers share R&D costs**

ATDF's R&D Foundry Vision

➔ To become the 1st 300 mm R&D foundry that serves our customers with

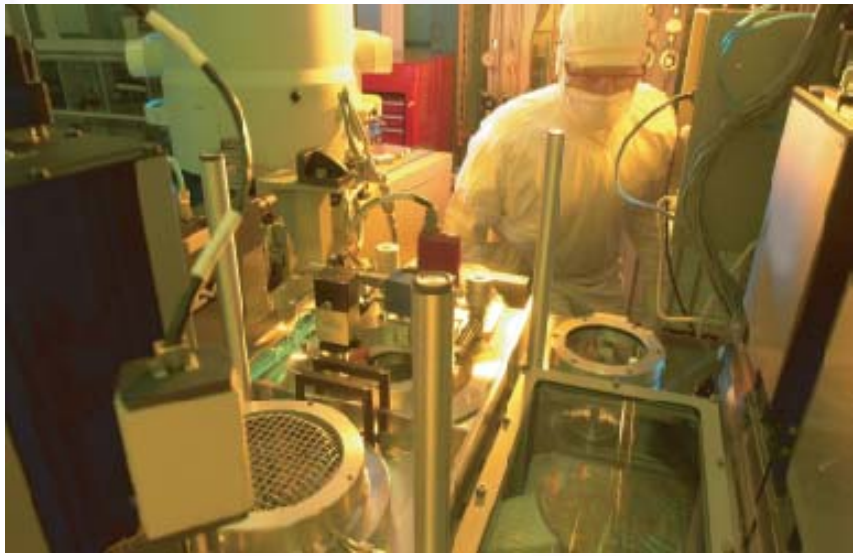
- ***IP Protection*** – Protection of IPs generated
- ***Full Customization*** – Customer defined projects w/ ATDF and/or other Partners
- ***Fast Learning*** – 6 cycles of R&D device learning per year
- ***Low Cost*** -- Low capital costs are passed on to customers. Per Wafer pricing

ATDF's Business

- Wafer Services
  - ATDF shipped 109,750 test wafers to suppliers, 2005
  - > 300 customers world wide, #1 test wafer supplier
  - Analytical Services
- Emerging Technologies
  - Major IDM makers outsource their R&D
  - Start-up companies prototype
- SEMATECH programs/AMRC support/SRC and universities
  - Front End of Line - Interconnect - Lithography
- Supplier programs
  - Cleanroom space made available for private use/access controlled
    - IP created by customer & protected
  - ATDF infrastructure available
    - TAP – Tool Access Program
- 300 mm start-up support

  Wafers to start-up equipment, training, best known methods for fab layout modeling support --Ti, AMD, IFX 300 mm start-up support

ATDF Infrastructure



- 62,000 sq ft (5800m2) cleanroom
  (42,000 sq ft of Class 1)
- ~ 200 process & analytical tools
- Complete 200 mm FEOL Flow
  - 300 mm conversion in 2007
- Complete 300 mm Cu/low-k multilevel interconnect
- Custom process design and flows
- 7 day/24 hour production
- ~ 11,000 wafer starts per month
- Equipment, process, and test devices have been developed or improved in the ATDF

Roadmap

	200mm	200mm	300mm
	l/s	l/s	l/s
	ATDF	**ATDF**	**ATDF**
	85nm Gate	**45nm Gate**	**32nm Gate**
	CMOS	**Current Tools**	**New Tools**
Production Year	end of 2004	Q1 of 2006	2007/2008
Active Pitch (nm)	700/700	250/250	100/150
N+ to P+ Space (nm)	N/A		
Gate Line/Space (nm)	100/900	65/250	45/200
Gate Physical (nm)	85	45	32
Contact size (nm)	350	150	90
Metal 1 Line/Space (nr	350/350	150/150	100/100
Via 1 size (nm)	N/A	250	90
Metal 2 Line/space (nr	N/A	250/250	100/100

Established 200 mm Baselines:

- Planar CMOS 85 nm Lg

- Planar CMOS Biaxially Strained Si 85 nm Lg

-TriGate and FinFET (MuGFET) CMOS (45/65 Fin/Gate)

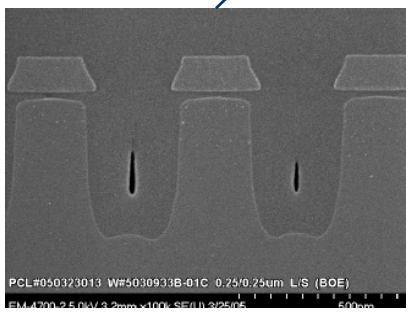
300 mm Baseline:

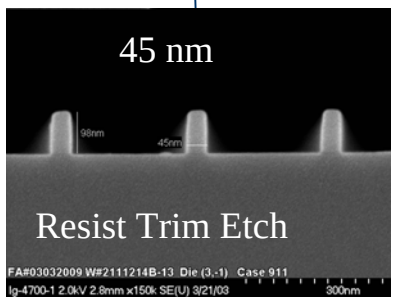
130 nm Cu/Low-K Dual Damascene

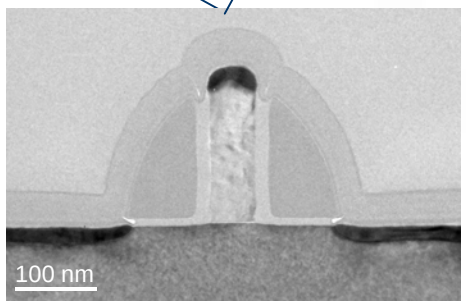
Platform

New Process, Material, Ideas

SSi SOX	Gap Fill CMP	Hi-K FUSI	Local Strain XMOS	New Material	ALD CNT
Si	Isolation	Gate stack	Transistor	Silicide	BEOL
Si SOI	STI	PNO Poly Si Metal gate	Planar MuGFET	NiSi CoSi	Cu, Lowk Al(Cu)



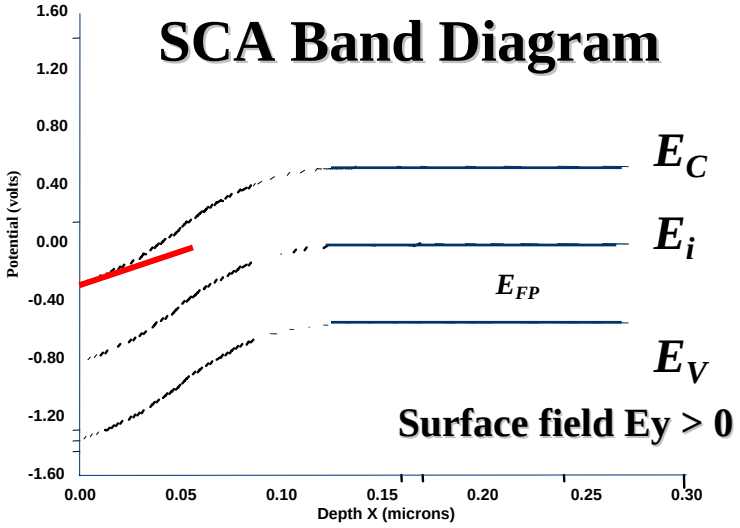


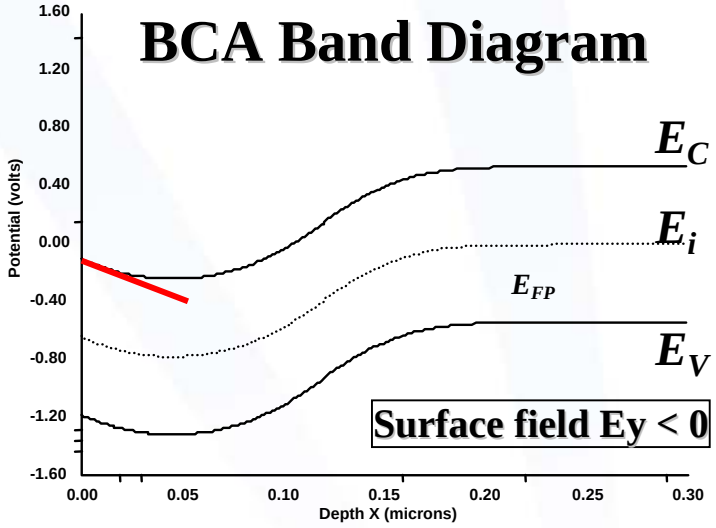


FEOL Example – Fermi-FET™

- Thunderbird Technologies, Inc., uses ATDF's 85 nm CMOS baseline.
  - STI, silicide, contact, M1 modules reused.
  - Gate stack is customized for desired workfunction.
  - Well, halo, channel implants optimized for enhanced performance, reduced leakage current for Lg=85 nm.
    - Thermal budget, implant conditions to be calibrated to provide device models (ongoing).
    - Spacer module optimized in context of implants, thermal budget.
  - "Foundary-friendly" process technology.

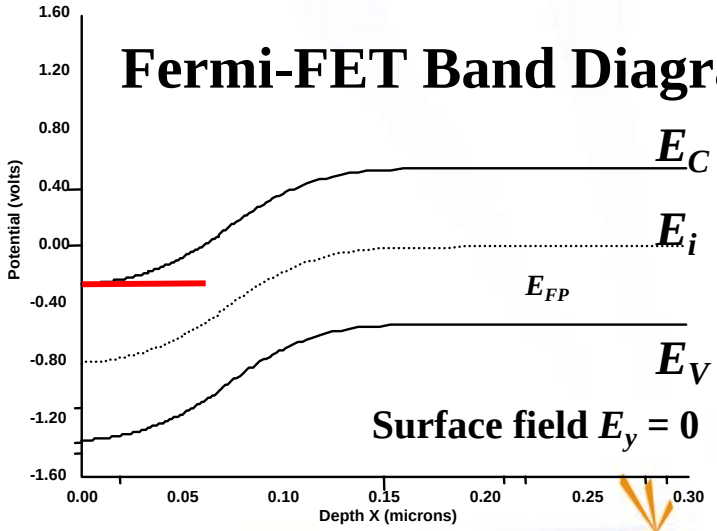
Higher Performance Devices
Fermi-FET 1



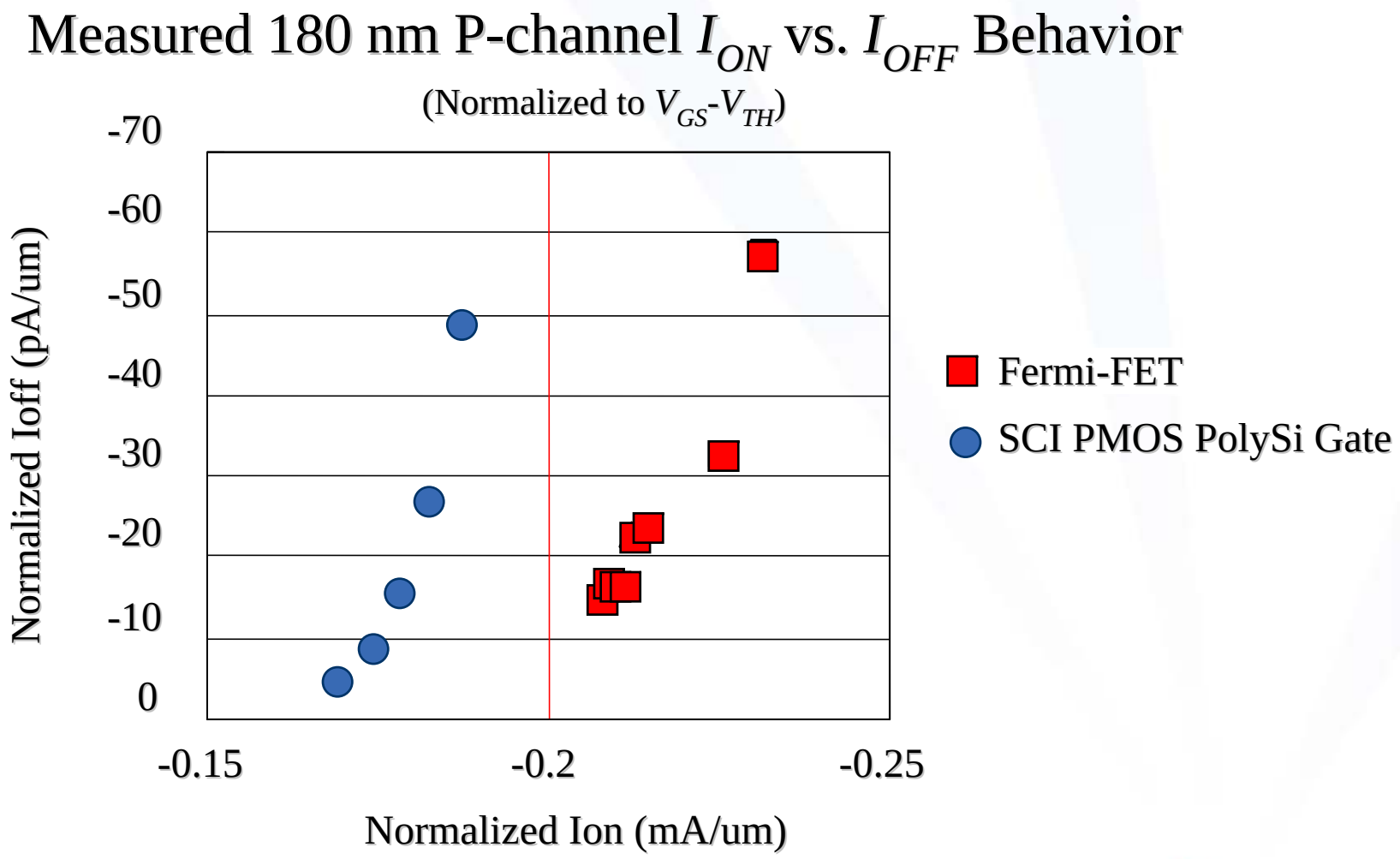


Band diagrams at V_G=V_{TH}

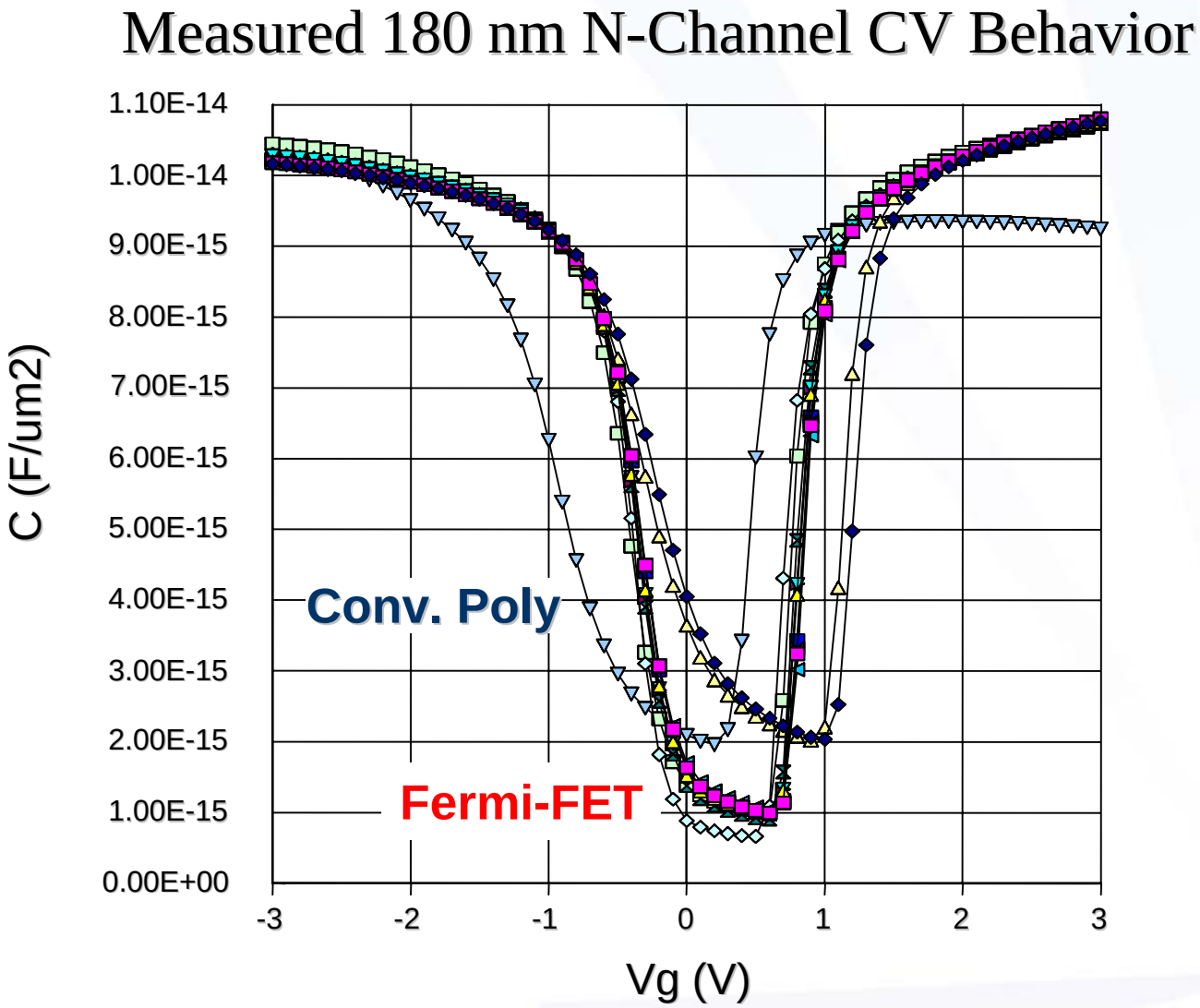
Fermi-FET device provides nearly *zero* surface field at threshold.



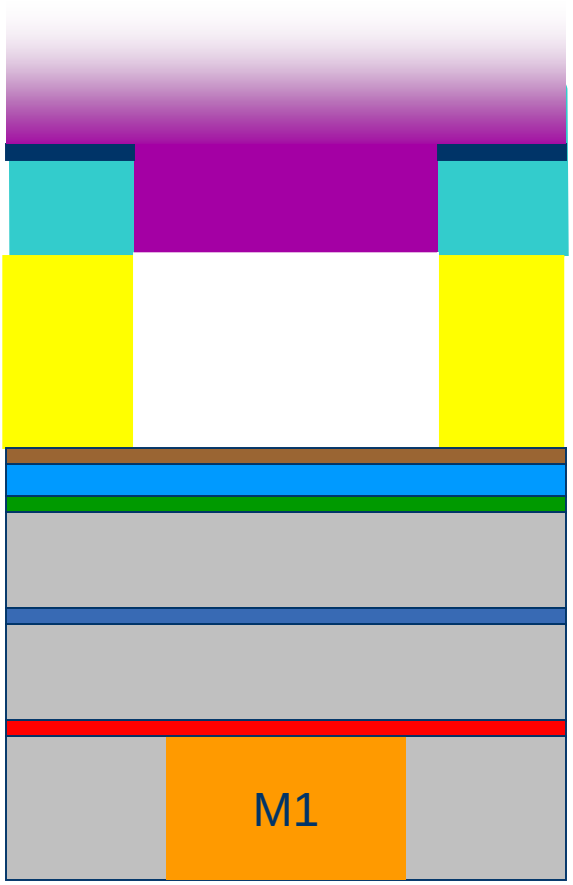
Higher Performance Devices
Fermi-FET 2



Higher Performance Devices
Fermi-FET 3



Dual Damascene Process Overview
SEMATECH's "Dual Top Hard Mask" Process

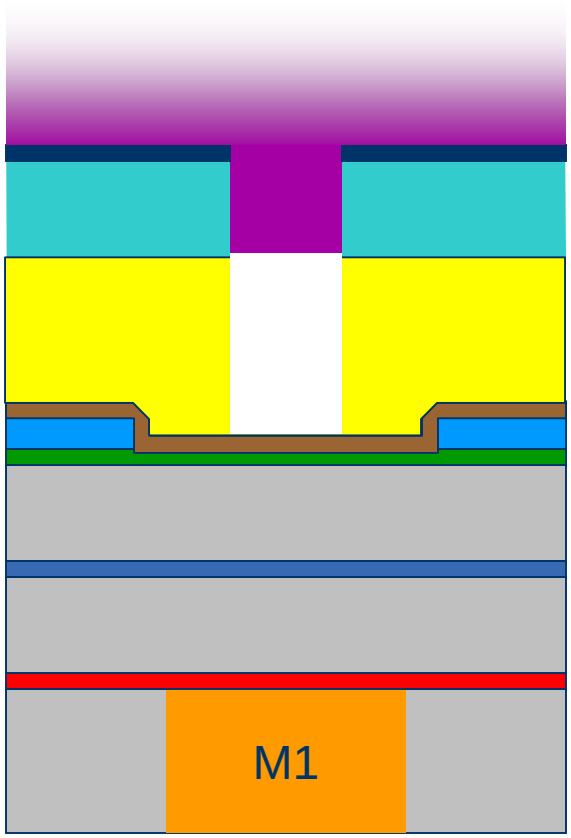


Expose
Develop

- Photoresist
- BARC
- Top Hard Mask
- Bottom Hard Mask
- Low-K Metal ILD
- Etch Stop
- Low-k Via ILD
- Copper Barrier

# of process steps: 10

Dual Damascene Process Overview
SEMATECH's "Dual Top Hard Mask" Process



Expose

Develop

Ash resist

Photoresist

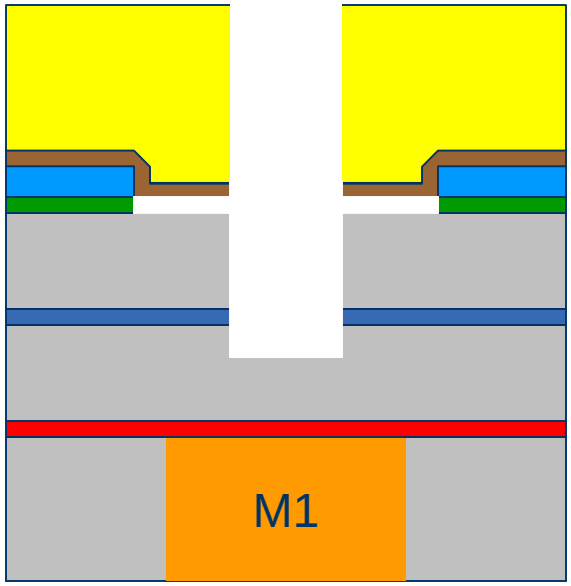
Etch Trench Hard Mask

BARC

# of process steps: 16

Dual Damascene Process Overview
SEMATECH's "Dual Top Hard Mask" Process

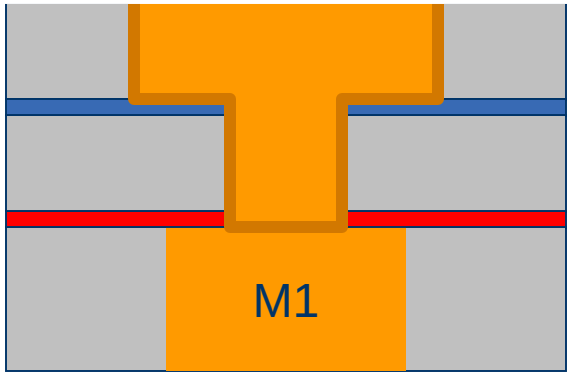
of process steps: 19



Ash & Trench Hard Mask Open
Etch Via Hard Mask
Etch Via & Trench Stop

Dual Damascene Process Overview
SEMATECH's "Dual Top Hard Mask" Process

of process steps: 23
x 8
184

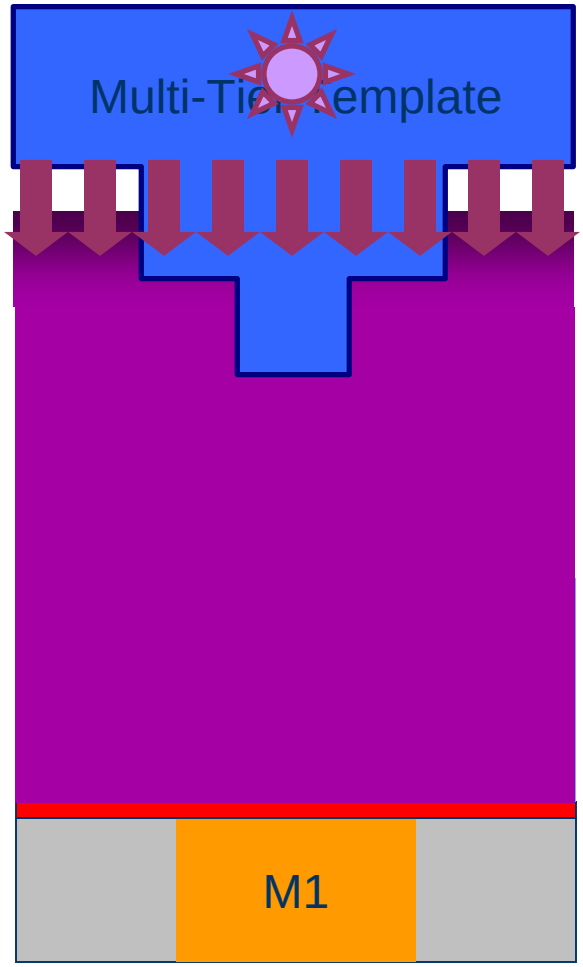


Copper Seed
CMP
Copper Plate

Trench & Via Etch

Barrier Etch

SFIL Damascene Process



# of process steps: 2

SFIL IMPRINTING
Release

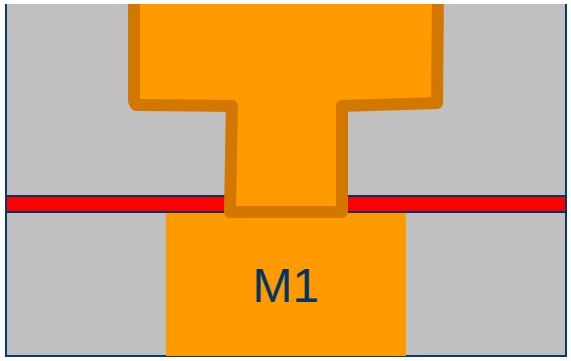
Etch Dielectric

Strip Precursor

Copper Barrier

SFIL Damascene Process

of process steps: 7
x 8
56



CMP
Copper Seed
Copper Plate
Residual Layer Etch
Barrier Etch

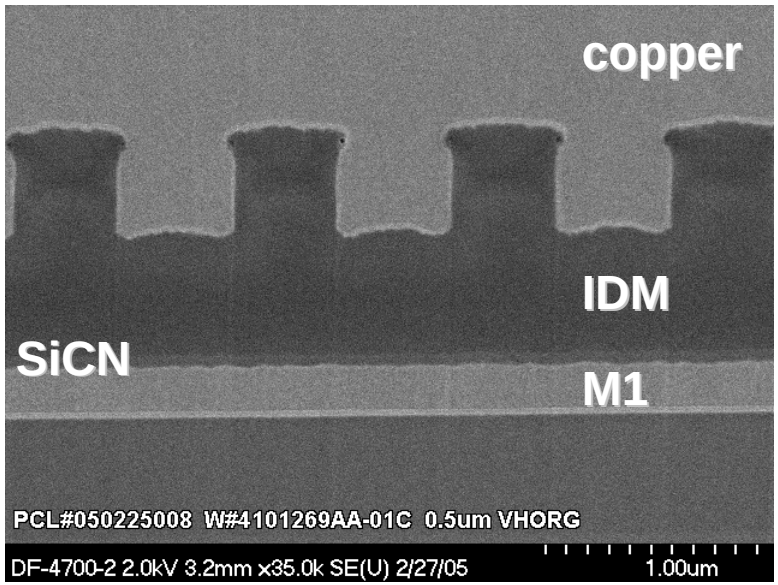
Savings of
184 – 56 = 128
steps

- Only one alignment step
- Trench-to-via alignment
  transferred from template
- No lithography over topography

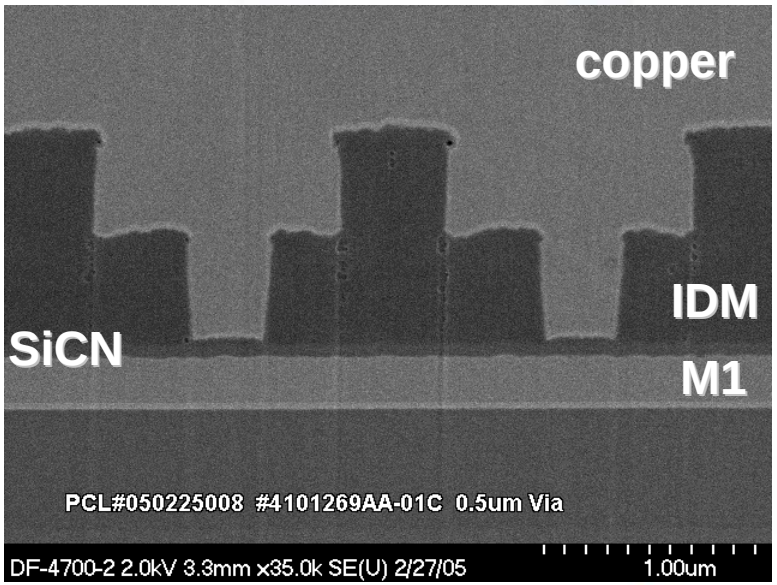
Copper Flow Integration

- Via opening etches (residual layer and barrier layer)
- Thermal stability (deposition and anneal steps)
- Adhesion & mechanical stability during CMP

M2 level Serpentine

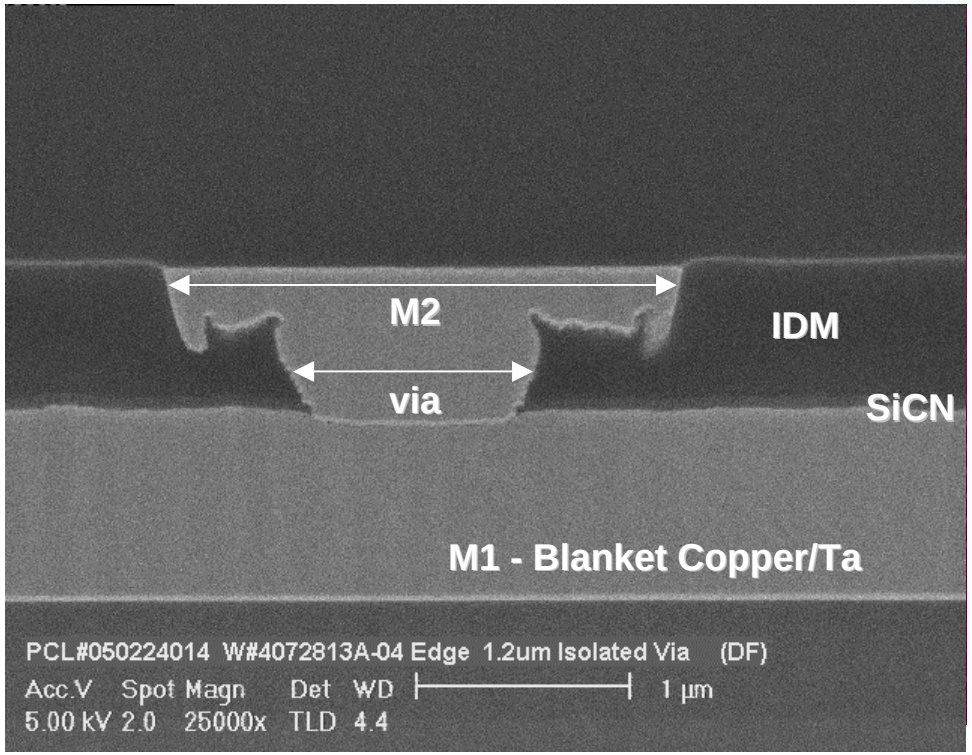


M2 & Via pattern

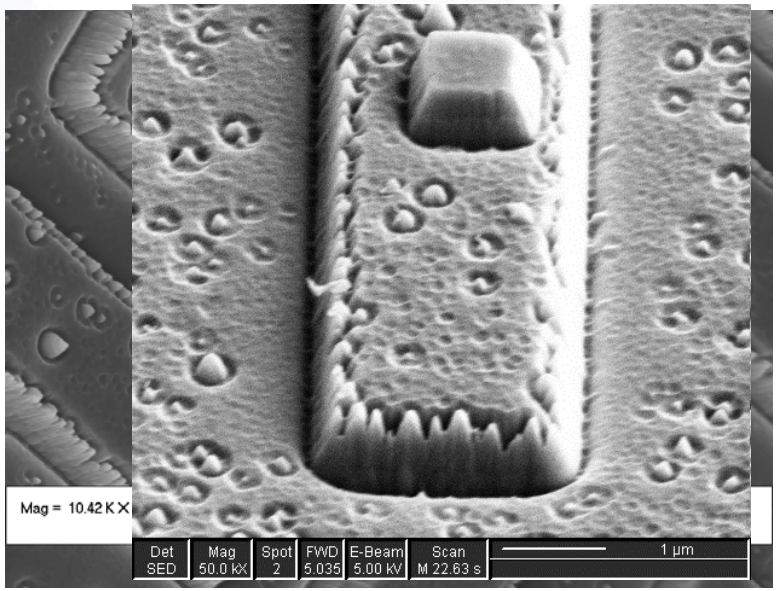


DuPont Photomasks Template

Post-CMP Features



Corresponding Template



LBNL Template

ATDF's Contributions to the Functional Resist Project

- Customized Test Vehicle Design
  - 810 GDS dataset created for DD processing in ATDF, based on 0.25 µm test vehicle.
  - Scaled to 0.25; 0.5; 1.0 and 2.0 µm features
  - M1 reticle and template, and M2/V1 template
- Integration and Process Engineering
  - Etch development for Cu open step
  - PVD barrier/seed development, low temp degas
  - RT recrystallation of plated Cu
  - Low down-force CMP of Cu and Ta
- Electrical Testing: in-line and bench test

Final Summary

- ATDF is a flexible R&D device foundary.
  - Operated as a Pilot Line in an IDM
  - Able to evaluate new materials and minimize/avoid risks associated with contamination to allow integration.
- Complete Process, Device and Materials Evaluations
  - Wafer process, in-line metrology, materials/process characterization, electrical testing, reliability testing.
- Ongoing in 2006:
  - Process simulation and calibration
  - Device simulation and calibration
  - Device Models

Appendix

- Process Capabilities
- Analytical Capabilties
- Test Capabilities

Acknowledgements

- Dr. Michael Dennen, Dr. Bill Richards, Dr. Drew Vinal of Thunderbird Technologies, Inc.
- Hideki Takeuchi, Dr. Shuji Ikeda of ATDF
- Dr. Michael Stewart of Molecular Imprints Inc., Dr. Grant Willson of U. of Texas at Austin.

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The Dual Damascene/SFIL work is an AMRC project presentation made possible, in part, by funding provided by SEMATECH.

Fermi-FET is a registered trademark of Thunderbird Technologies, Inc.

Process Capabilties (200mm)

- **Lithography**
  - 248 patterning (200 mm & 300 mm)
  - 193 patterning (200 mm & 300 mm)
- **Wet Processing/Cleaning**
  - Immersion (PreGate, Metals); Spray-FSI's (Doped, Undoped); Spray-SEZ (backside, Wedding Cake); Vapor HF (FSI)
- **Diffusion/Hot Processing**
  - Atmospheric (Anneals, Oxidation(wet/dry), LowK Cure)
  - Reduced Pressure (TEOS, LowK Cure)
- **Plasma Etch/Ash**
  - Poly (LAM, Applied Materials); Si (LAM, Applied Materials); Oxide (TEL, Applied Materials); Metal (LAM, Applied Materials)
  - Ash (ULVAC, Axcelis) – special processes for metals
- **Implant**
  - High Current (AMAT-Leap); Medium Current (ULVAC, Bridge tool, Quad)
  - Dose 1E11-1e16/ 200eV-80KeV; 1E11-1E14/3KeV-900KeV, max 60˚ tilt
- **Metals**
  - PVD* (Cu, Ta, TaN, Ti, TiN, Al, Mo, Co, Ni); ALD*; CVD W, TiN(Si); ECD Cu
- **PECVD** (SiN, TEOS, SiON, PSG, SiC, SiCN, SiCO)
- **Anneal –** Mattson Spike, Mattson Flash(private), AG8800 (lamp)
- **CMP –** Cu, Oxide (Applied Materials Mirra)

In-Line Metrology Capabilities

- Litho – Overlay, CD
  - Applied Materials CD SEM (expect a 2nd Applied Materials CD SEM)
- Films – thickness, RI, stress, multilayers, pattern recognition for features, composition
  - Spectroscopic ellipsometry
  - FTIR
  - Wafer curvature, wafer bow
  - AFM/Profilometer
  - X-ray reflectivity (specular and diffuse)
  - SAW
- Particles, defect review station
- SPC – tools are routinely qualified for particles and process and film parameters.
  - Eg, dep rate, etch rate and uniformity. Film thickness and uniformity.

Analytical Services

Capabilities

- Atomic Force Microscopy (AFM)
- FE Auger
- FE Scanning Electron Microscope (FE SEM)
- SEM EDS Analysis and OIM
- Secondary Ion Mass Spectroscopy (SIMS)
- Transmission Electron Microscopy (TEM/STEM)
- TEM/STEM EDS, EELS and Electron Diffraction
- Total X-Ray Fluorescence (TXRF)
- X-Ray Florescence (XRF)
- X-Ray Reflectometry (XRR)
- X-Ray Photoelectron Spectroscopy (XPS)
- VPD ICP-MS
- BEAT (Beveled Edge Analytical Technique)
- Atomic Absorption (AA)
- Hg-Probe CV - Analysis

Electrical Test Capabilities

Equipment:

- High volume automated in-line parametrics – 200 mm & 300 mm
- High volume automated IV & CV arrays with up to 60,000 lines of data
- IC-V software allows for fast custom test generation & auto testing
- 8753C Network Analyzer
- Data analysis tools
- Raw Data Extraction
- Hot chuck temperatures up to 300C
- Cold chuck temperatures down to L-He
- Engineering Stations

Algorithms:

- Wafer Level Reliability- HCI, NBTI, BTS, TDDB, GOI, RVB, EM
- Charge trapping, charge pumping /quasi-static Dit characterizations
- ID family of curves- IV,IDVD, IDVG, IGVG, Ion, Ioff, Isat, body bias
- Capacitance – multiple frequency 20Hz-110MHz

Materials Integration Challenges for Next-Generation Interconnects

Michael D. Goodner
Mansour Moinpour

Intel Corporation

2006 Review: NSF/SRC ERC for Environmentally Benign Semiconductor Manufacturing

February 23, 2006 – Tucson, Arizona

Agenda

- Motivation for low k materials
- Integration challenges with current materials
  - Pore sealing
  - Etch stop
- Next-generation interconnect options
- Focus areas for future development
- Summary

Contributors:

Boyan Boyanov, Grant Kloster, Bruce Block

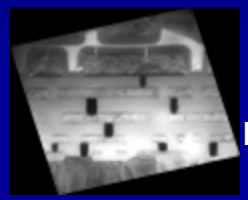
Interconnect Scaling & Future Options

1000 nm

Two Al Metal layers, BPSG

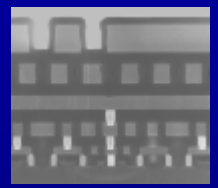
500 nm

ILD planarization, W plugs w etch back



350 nm

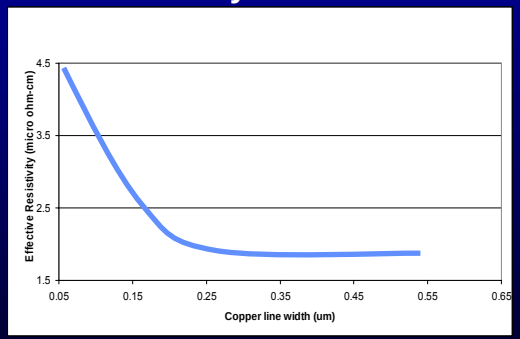
Four Al metal layers, W polish, PSG?

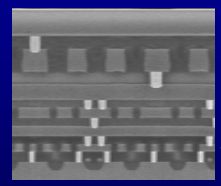


250 nm

Five Al metal layers, SiOF

Cu Resistivity vs Line Width



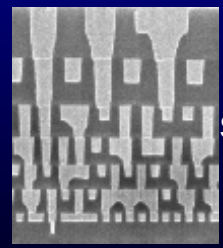


180 nm

Six Al Metal layers

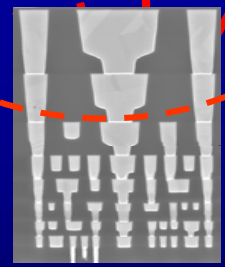
130 nm

Six Cu Layer



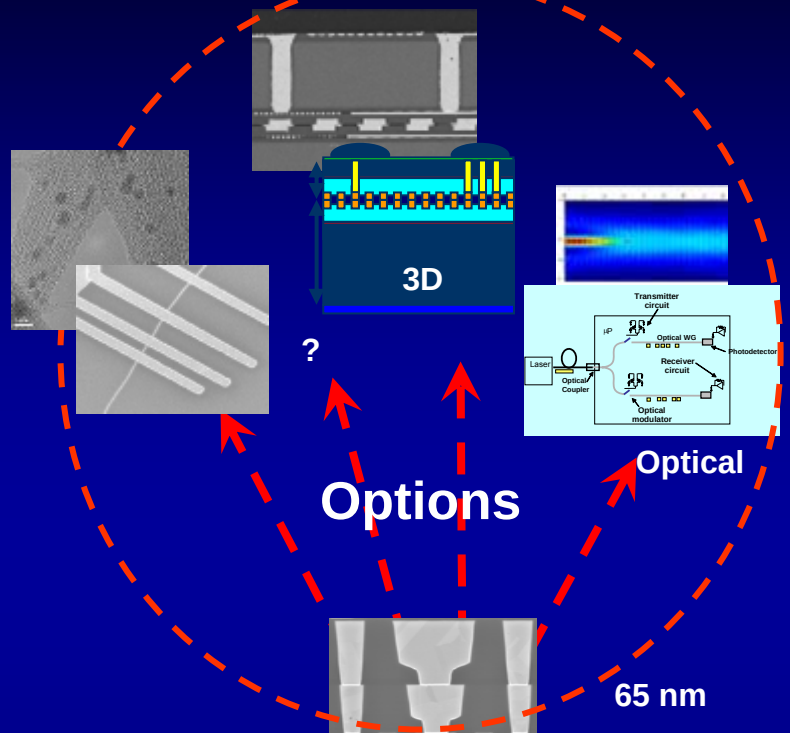
90 nm

Seven Cu Layer

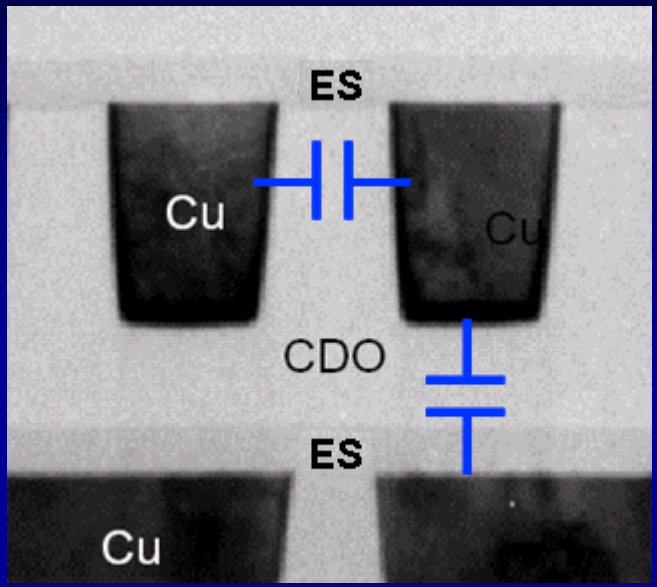


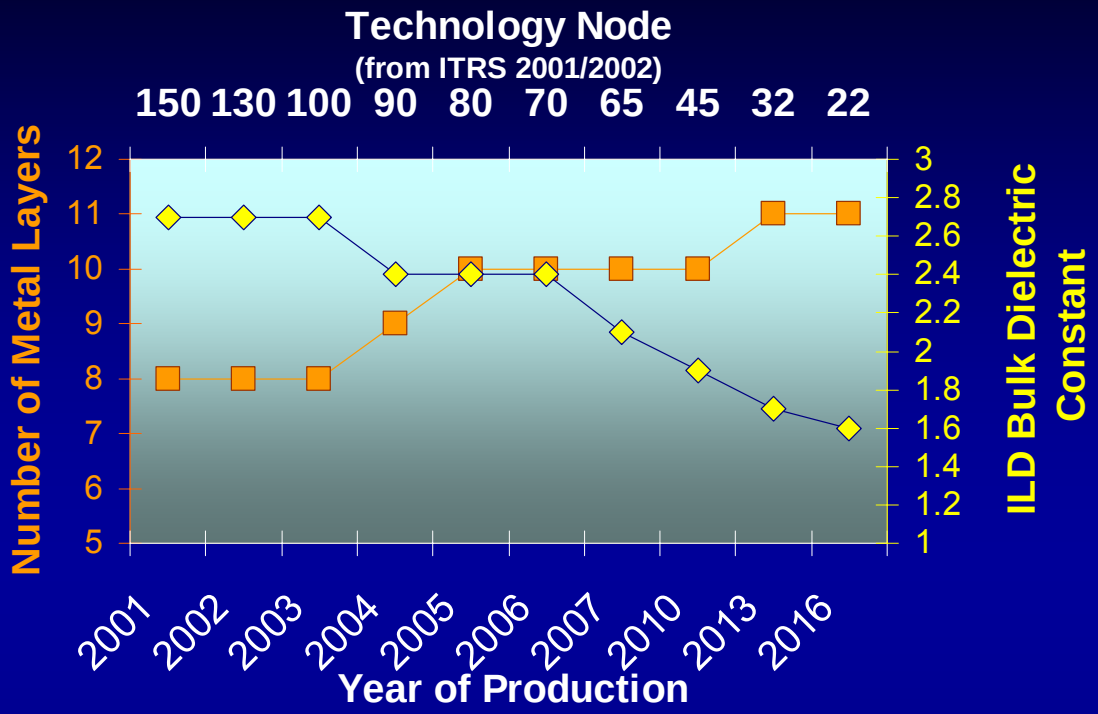
65 nm

Eight Cu Layer



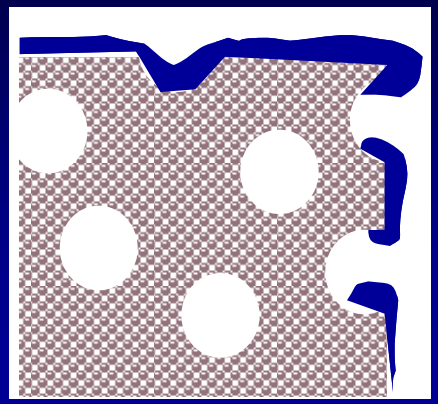
Motivation for Low-K



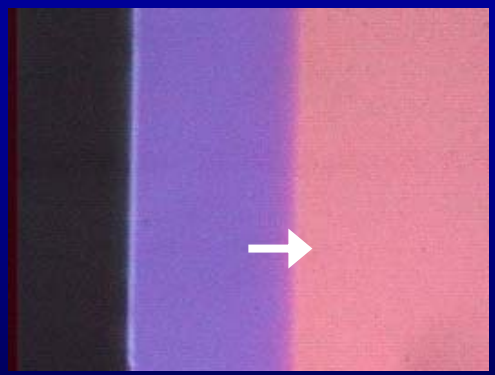


- Interconnect RC delay is now equal to or greater than front end delay effects
  - Cu provides lower R than Al, but cannot be reduced each generation
  - Power, cross-talk and delay must be minimized by reducing ILD capacitance (k)
- Main approaches to achieve lower K are carbon doping and/or to introduce porosity
  - ⇨ Requires significant integration and provides limited extendibility

Challenges – Porous ILD



Poor barrier / seed coverage due to exposed pores



Precursor penetration: Toluene penetration is one method to determine porosity

Source: IMEC

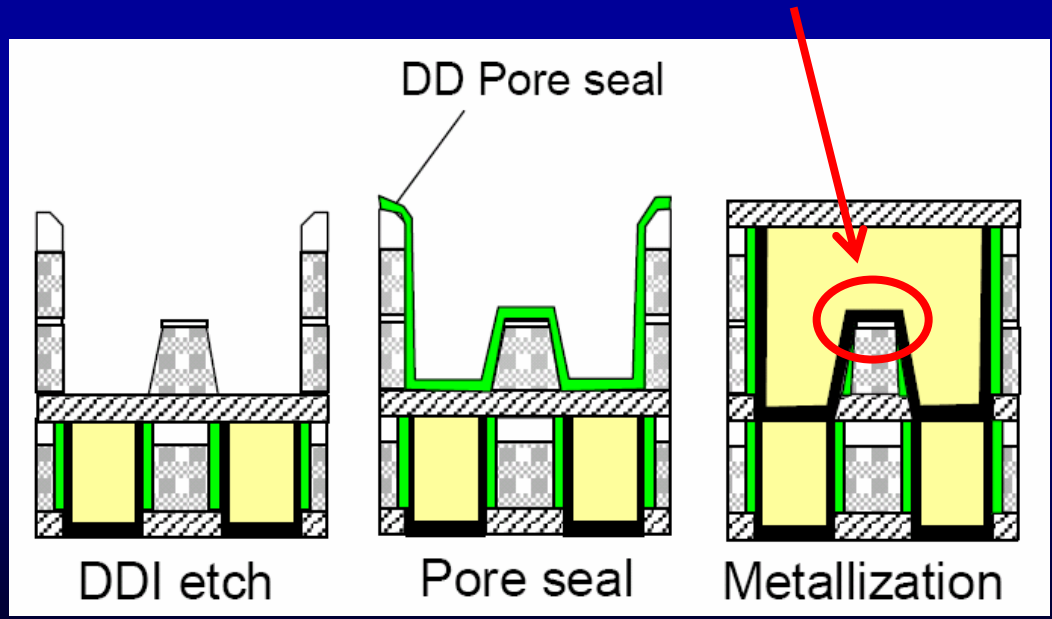
- Robust k < 2.4 film will likely be porous
- Metallization of porous ILD presents several challenges
  - Pores cause defects in barrier coverage → reliability failures
  - Increasing porosity (> 20-30%) leads to interconnected pores → ALD / CVD precursor penetration

Need solutions to minimize and/or eliminate Low K / Barrier interaction

Dual Damascene Pore Sealing

- Two primary routes for sealing porous dielectrics:
  - Plasma / beam treatments
  - Deposition of separate sealing layer
- Both have shortcomings:
  - Difficult to control sealing thickness of plasma & beam treatments, chemistry can be similar to damage layer
  - Non-selective deposition can leave trench bottoms exposed, unless trench ES is used
- For k_{ILD} = 2.4, 10nm trench ES increases k:
  - 2% for k = 3.0 ES
  - 8% for k = 5.5 ES

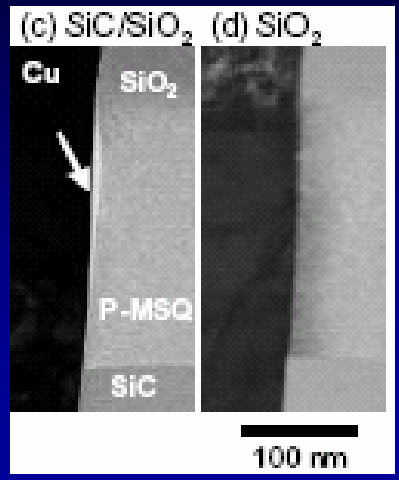
Need low-k pore sealing material selective to Cu / metal cap



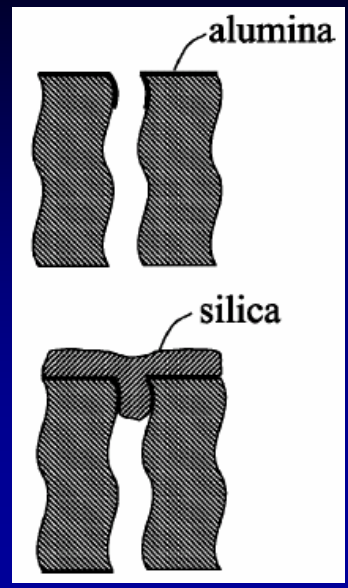
Ueki, *et al.*, 2004 Symposium on VLSI Technologies

Selective Pore Sealing

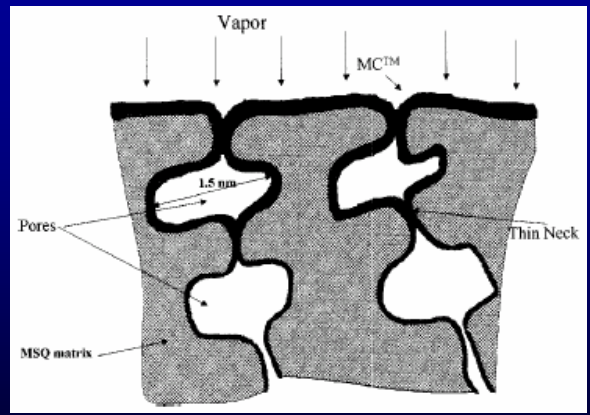
- Process and materials solutions being explored
- Process:
  - Etch byproduct redeposition
    - Concerns about surface roughness, adhesion and pinhole defects
- Materials:
  - ALD Silica
    - Conformal SiO_2 coatings with Al seed
    - Need to tailor penetration and metal selectivity
    - Larger k_{eff} impact than low k sealants
  - Parylene deposition
    - Selective to transition metals
    - Must limit penetration to minimize k impact



Furuya, *et al.*, 2004 IITC



de Rouffignac, *et al.*, Electrochem Solid-State Lett, (2004) v 7, pp G306-G308



Jezewski, J Electrochem Soc, (2004) v 151, pp F157-F161

Low K Etch Stop

- Limited but important options for low-k etch stop development
  - Thin etch stop
    - Reduction from 25nm to 10nm gives 6.8% reduction in k_{eff}
    - However, higher selectivity to low-k ILD is needed
  - Low K etch stop
    - Reduction from k ~ 5.5 to k ~ 3.0 gives 12.3% reduction in k_{eff}
    - Must have chemical diversity to maintain etch selectivity between ILD and ES
- Reducing k_{ES} provides biggest impact
  - Requires greatest material development

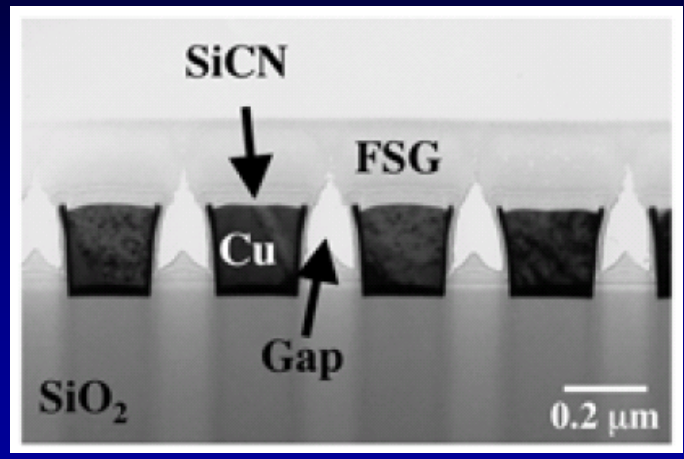
For k_{ILD} = 2.4 model system:

k_{ES}	thk_{ES} (nm)	k_{eff}	Δk_{eff} (%)
5.5	25	2.84	---
5.5	10	2.65	6.8
3.0	25	2.49	12.3
3.0	10	2.45	13.6

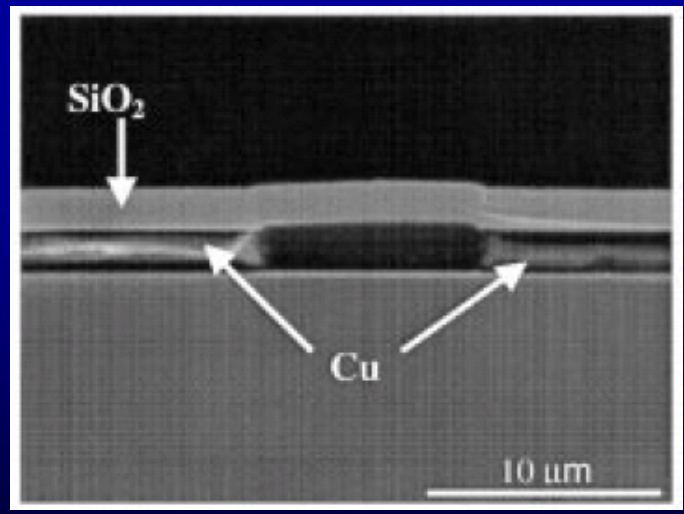
Low K hermetic ES development needed to realize largest potential gain with smallest process impact

Air-Gap: The lowest possible k

- Air-gap incorporates the limiting case $k_{ILD} \rightarrow 1$
- Two approaches to air-gap interconnects:
  - Process: Form air-gap through deposition properties
  - Materials: Remove sacrificial material downstream
- Both have significant challenges:
  - Structural integrity of final structure is questionable
  - Additional process steps add significant cost!
  - Multi-layer processing presents additional challenges…



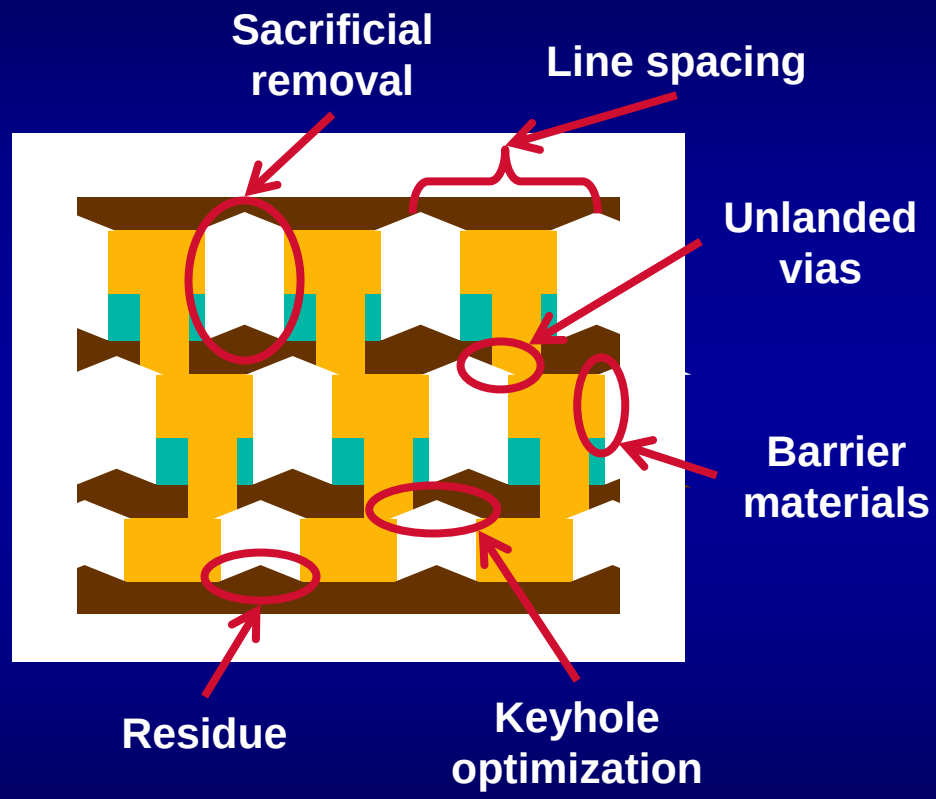
Noguchi, *et al.*, IEEE Transactions on Electron Devices (2005), v 52, n 3, pp 352-359



Bhusari, *et al.*, J. Microelectromechanical Systems, (2001), v 10, n 3, pp 400-408

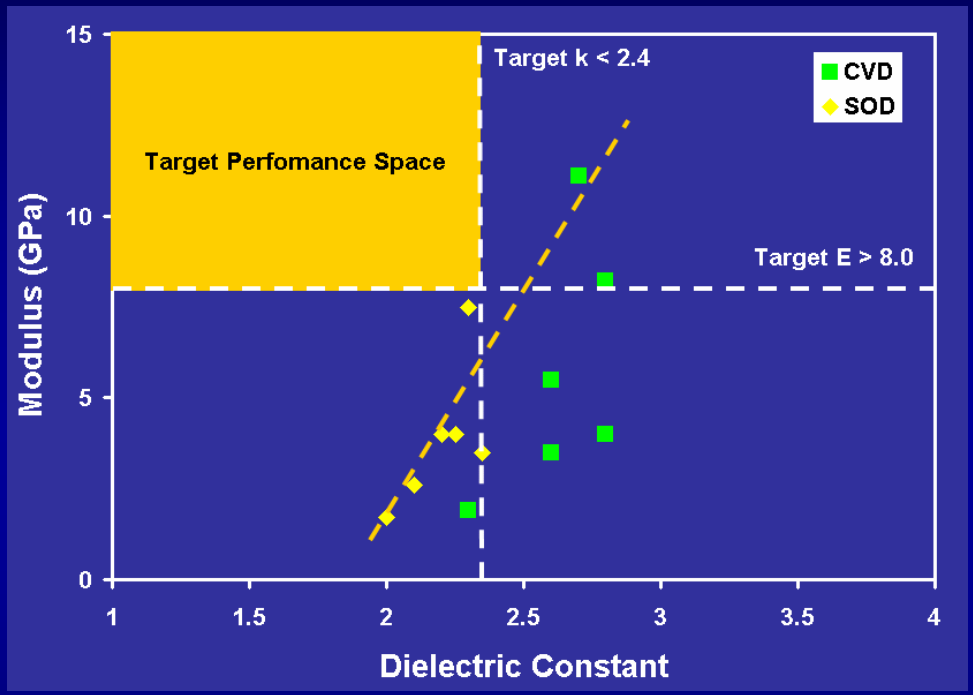
Multi-Level Air-Gap Challenges

- Common issues
  - Metal Barrier: Thick enough to prevent EM, but low R impact
  - Unlanded vias: If allowed, need film to land on
- For process-generated air-gap:
  - Keyhole needs to be optimized to ensure zero fill while maintaining ES integrity
  - Residue must be inert and immobile
  - Line spacing is restricted on all layers
- For sacrificial material air-gap:
  - Robust removal technique needed
  - Remove at each layer vs. EOL?



Need process *and* material innovations to enable air-gap

Novel Materials



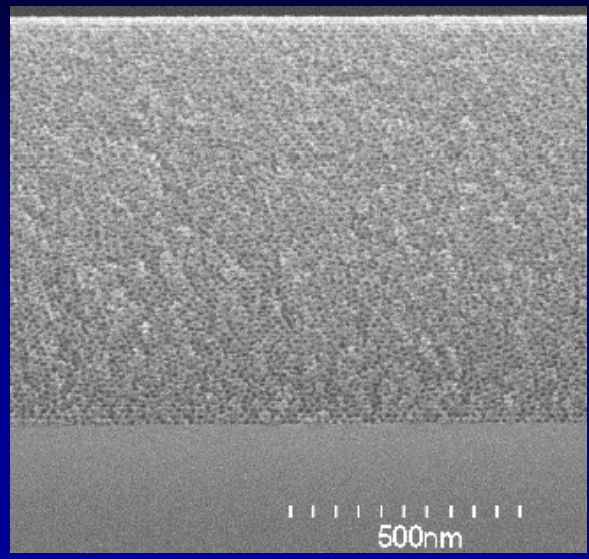
Source: Data from IMEC evaluations, used with permission

- Areas outlined so far do not address ultimate requirement: thermomechanical reliability
- Many CVD and SOD materials lie along (or below) same performance curve
  - Similar trends exist for hardness, cohesive strength
- Cure optimization is not sufficient to move into desired performance space

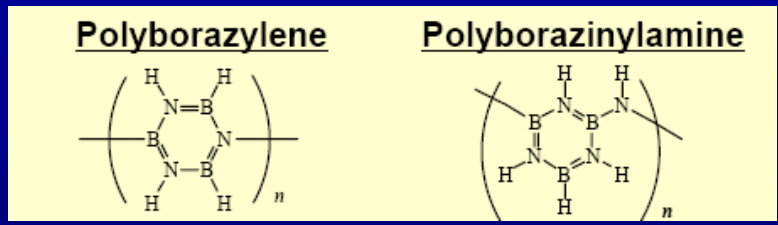
Need fundamental materials changes to enter new performance space

Novel Materials Development

- Several routes toward new E vs. k performance already being examined
- Templated materials
  - Ordered structure provides increased strength at low porosity
  - Feasibility has been demonstrated for zeolites as well as ordered sol-gel materials
    - Up to 5x increase in E for equivalent k
  - Pore sealing very important for zeolites due to high pore connectivity
  - All processes are spin-on, some based on supercritical CO_2
- Non-SiCOH materials
  - Various BN and BCN materials have been researched
  - Adhesion concerns must be addressed, etch and cleans impact understood
  - Potential route to new performance space for dense and microporous films



Pai, et al., Science, 2004, 303, 507-510

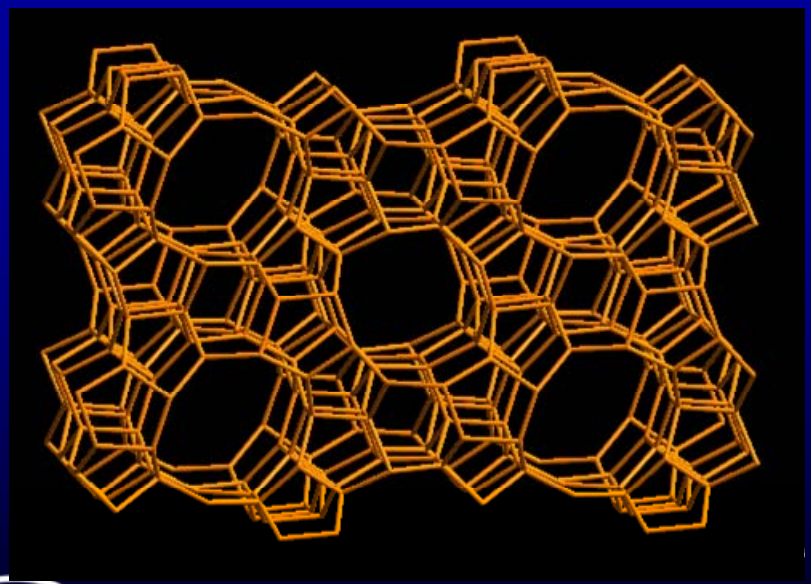


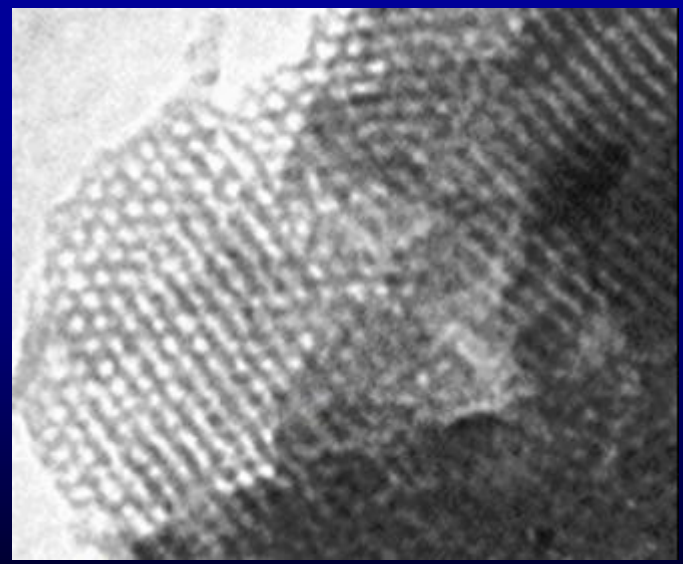
Material	k_{calc}
Polyphenylene	3.0
Polyborazylene	1.9
Polyborazinylamine	2.0

Data and figure from Kumada, *et al.*, 2004 ISMT Low K Symposium

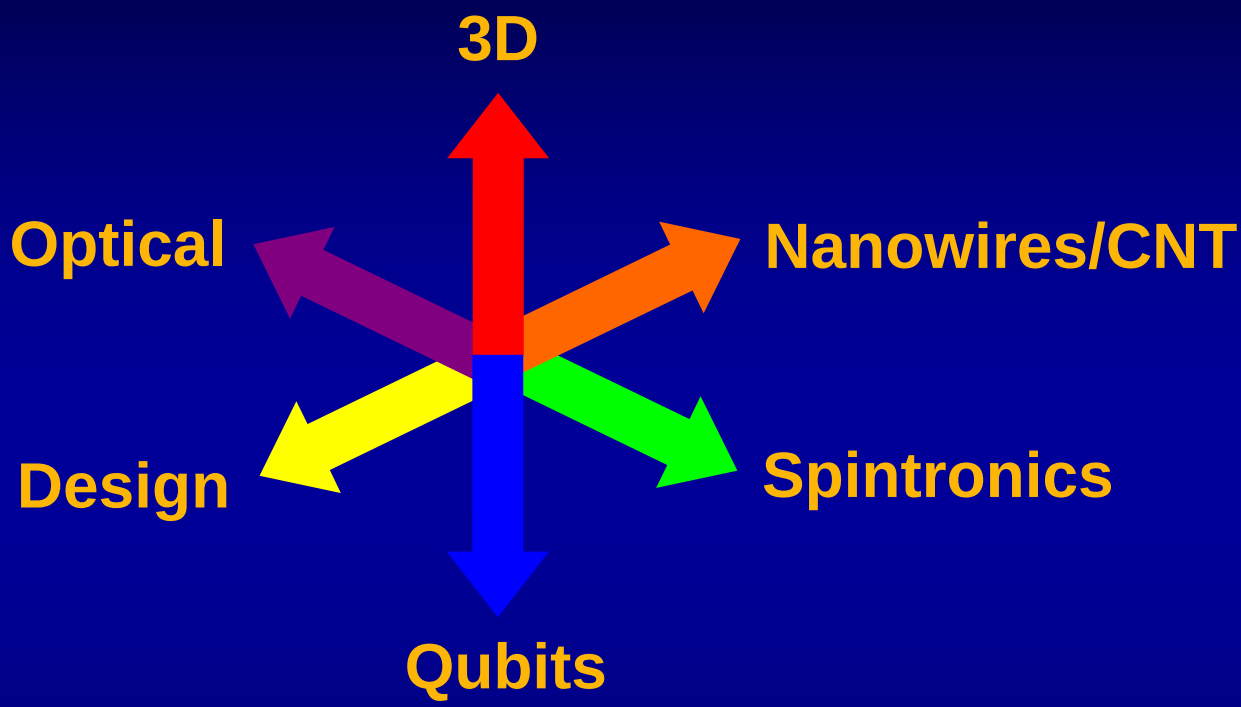
Templated Materials

- Templating allows materials with ordered porosity
  - Can achieve high porosity while maintaining mechanical strength
- Zeolites: class of naturally-occurring ordered porosity materials
  - Synthetic pure SiO_2 zeolite (silicalite) shows ~5x increase in modulus for equivalent k value (Wang, *et al.*, Adv. Mater. 2001)
  - Adding other metals (Al, Ti, Ge, Mn…) can increase strength further
- Currently, only available through spin-on sol-gel processing



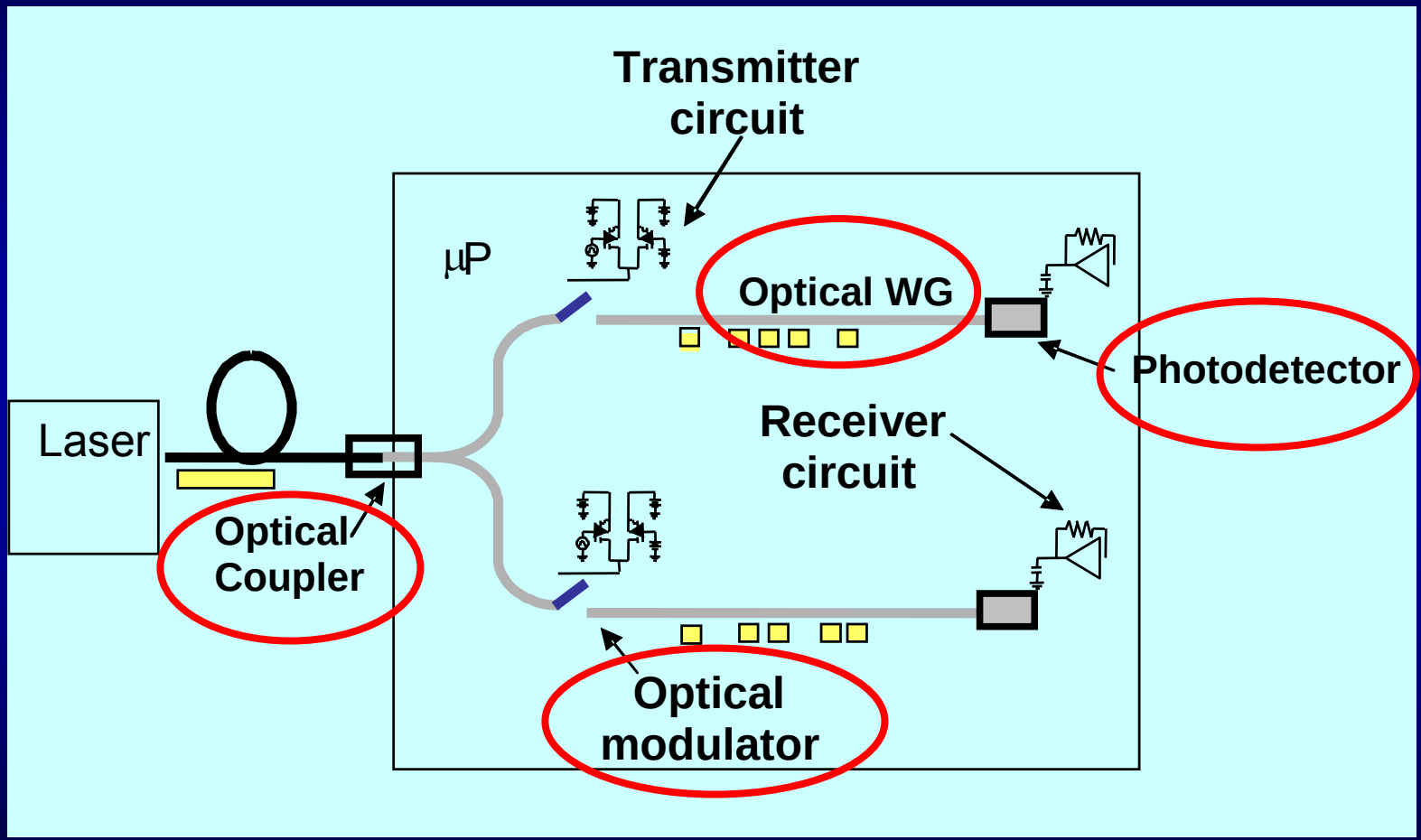


Beyond Cu / Low k Scaling ?



• Needs should drive choice with **large impact and appropriate timing**.

One Option: On Chip Optical Interconnects



Optical Building Blocks

CMOS Building Block Materials

	Waveguide or Cladding	Photo-detector	Modulator
SiO_2	✓		
Si_3N_4	✓		
Polyimide	✓		
SiCOH	✓		
Si	✓	✓	✓
Ge		✓	✓

New modulator materials are required

Candidate Modulator Materials

Material	Effect	Device Performance	Issues
Si	Free carrier	2.5 Gb/s – MZI (~1 cm)	•Speed •Optical loss
EO Polymer	Linear EO	100 Gb/s – MZI (>1cm) 4 Gb/s – ring resonator (100 um)	•Small effect •Thermal Stability •Poling
Ferroelectric Oxide	•Linear EO •Quadratic EO	40 Gb/s -$LiNbO_3$ MZI	•Deposition Temperature •Complex Materials •High Dielectric Constant

- On chip modulators are very immature
- Lots of materials issues with EO materials
- Key for OI technology

Focus Areas for Development

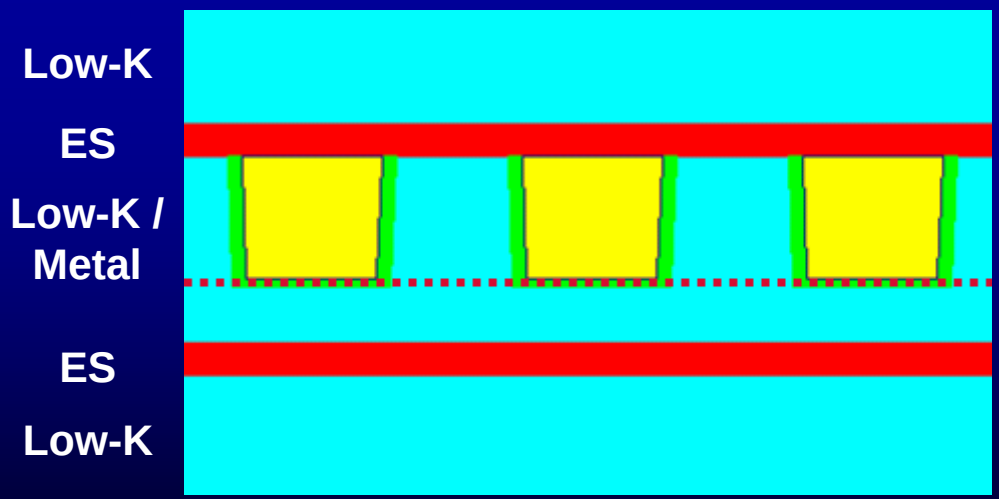
- Near-term (2-3 generations)
  - ILD repair / carbon restoration
  - Alternative cure characterization
  - Dual-damascene compatible pore sealing
- Longer term
  - Alternative materials (beyond SiCOH)
  - Templated / ordered materials
  - Alternative interconnect schemes
    - 3D, optical, nanotubes…

Summary

- Selective pore sealing or alternative process schemes needed to integrate porous materials
- Development of hermetic low k etch stop provides large gain for single-generation improvement
- New materials needed to make revolutionary move out of current performance space
- New interconnect options will generate new materials selection and integration challenges

Appendix – Model System

- Raphael™ simulations were used to calculate impact of different architecture / material combinations
- Basic system is three metal lines in low-k ILD; entire structure is on low-k base and capped with low-k
- Dimensions loosely based on 2004 ITRS
- Damage / pore sealing layer and trench ES added to some scenarios, ES thickness varied



- Dimensions:
  - ILD thickness: 135 nm
  - ES thickness: 25 nm
  - Metal pitch: 100 nm
  - Metal depth: 90 nm
  - Metal Top CD: 50 nm
  - MT Bottom CD: 47 nm
- Materials:
  - $k_{ILD} = 2.4$
  - $k_{ES} = 5.5$
  - $k_{OX} = 4.0$ (for damage / pore seal)
- k_{eff} for model system ⇨ 2.84

For further information on Intel's silicon technology and Moore's Law, please visit the Silicon Showcase at www.intel.com/research/silicon

Key Development Challenges for Planarization and Interconnects at the 32nm Node and Beyond

Mansour Moinpour, Michael D. Goodner

10th Annual Review of NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

Feb. 23-24 2006, Tucson AZ

Contributors: J. Blackwell, B. Boyanov, G. Ding, V. Dubin, P. Fischer, F. Gstrein, S. Johnston, G. Kloster, S. List, M. Garner

Silicon Scaling Introduces Numerous Material Challenges

- Lithography
- Transistors (not discussed here)
- Interconnects
  - CMP
  - Low K
  - Metallization
- What's beyond Cu/Low K?

Evolution of CMP

Logic Technology	Application	Equipment	Post-CMP Cleaning Processes
First Generation (0.8-0.5 um)	• Oxide (ILD)	Single platen, Single head, One step polishing	Wet station cleaning, DI wafer scrub
Second Generation (< 0.5 um)	• Oxide +ILD0 • W CMP + STI	Multiple platens & heads, Two-step polishing, End-point, On-board metrology	DI wafer scrub, NH_4OH clean
Third Generation (< 0.25 um)	• Oxide +ILD0 • W CMP + STI • Cu, doped ILD	Multiple platens & heads, Multi-step, End-point, On-board metrology, Integrated dry-in/dry-out, non-rotary (orbital, linear CMP)	DI wafer scrub, NH_4OH clean, HF-clean, Integrated dry-in/dry-out, new chemistries
Fourth Generation (< 0.15um)	• Oxide +ILD0 • W CMP + STI • Cu, doped ILD • Low-k, ULK, various barrier films	Multiple platens & heads, Multi-step, End-point, On-board metrology, Integrated dry-in/dry-out, non-rotary (orbital, linear CMP)	DI wafer scrub, NH_4OH clean, HF-clean, Integrated dry-in/dry-out, new chemistries (surfactants, chelating/complexing agents)

Increased Complexity In Materials & Surfaces

Increased Complexity In Post CMP Clean

M. Moinpour, A. Tregub, A, Oehler, and K. Cadien, "*Advances in CMP Consumables*", MRS Bulletin, October (2000)

Continuous Improvement Areas

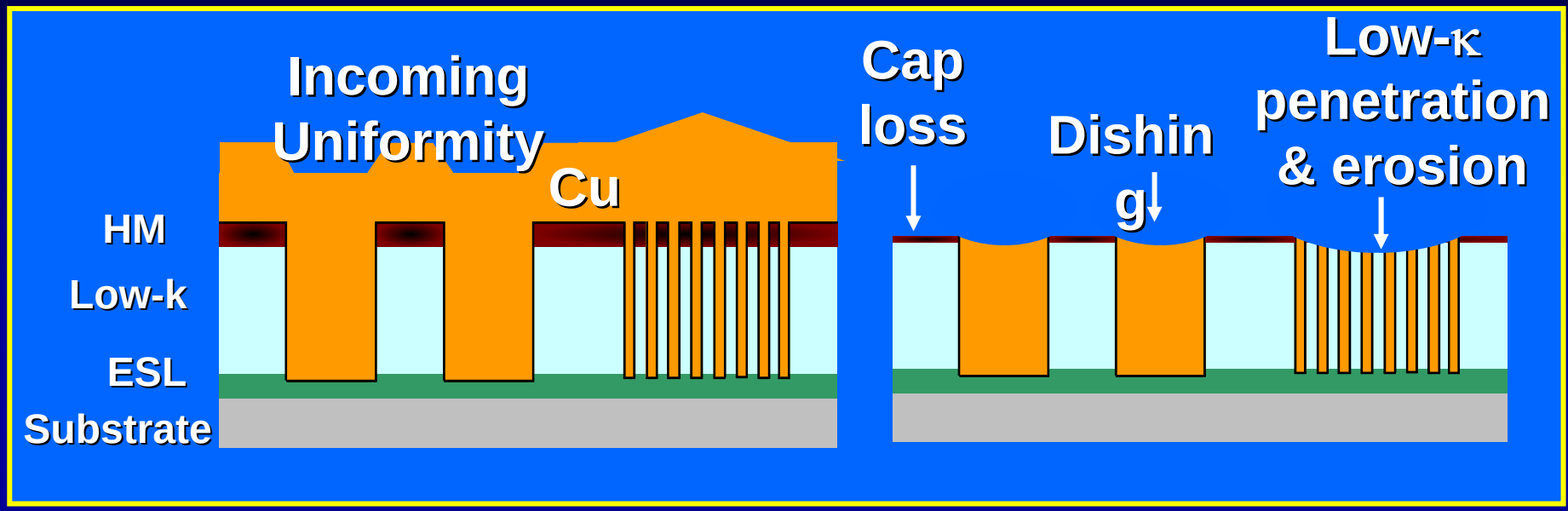
- Cost improvements
  - Raw consumable costs
  - More efficient pads, slurry, equipment
- Defect reduction
  - Improved quality control
  - Process control
  - Predictive monitors for pad slurry quality
  - More accurate particle metrology
- Improved topography control

  WID WIW

CMP Technology Trends

- Topography requirement trends with Moore's Law: 30% reduction every two years (Next Page)— CMP pace is critical in maintaining Moore's law.
- Materials that are subject to polish are diverging due to diverging application needs.
- Each application could deal with heterogeneous materials, leading to complex solutions.
- Key words for future CMP applications are versatility and tunability
- Nano particle engineering and characterization, complex chemistry and new metrology for new applications

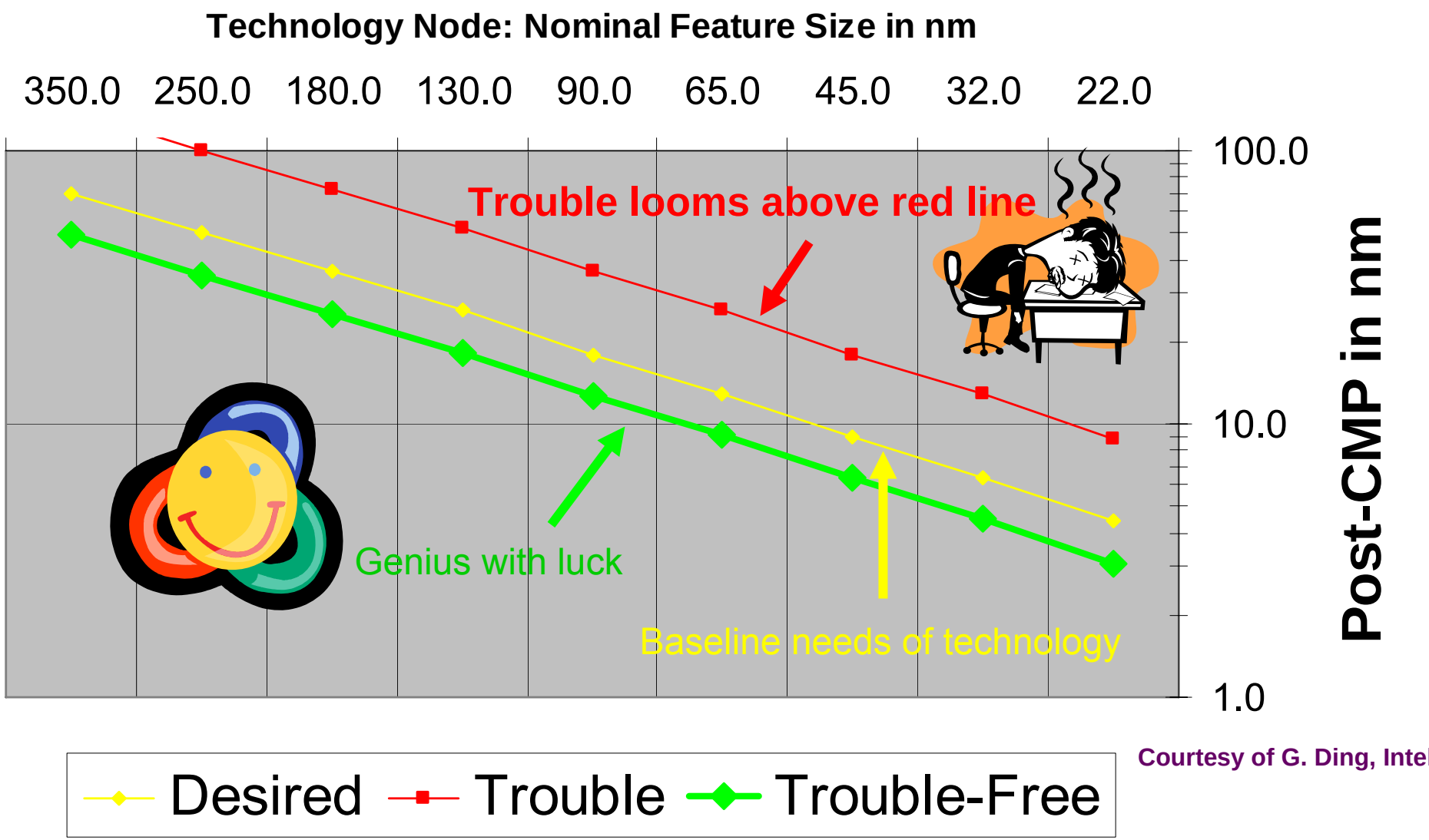
Pattern Dependent Concerns



- Independent of Cu/low-κ, Conventional CMP Metrics
- New Challenges
  - Mechanical Integrity Issues
  - Corrosion & Defectivity Concerns

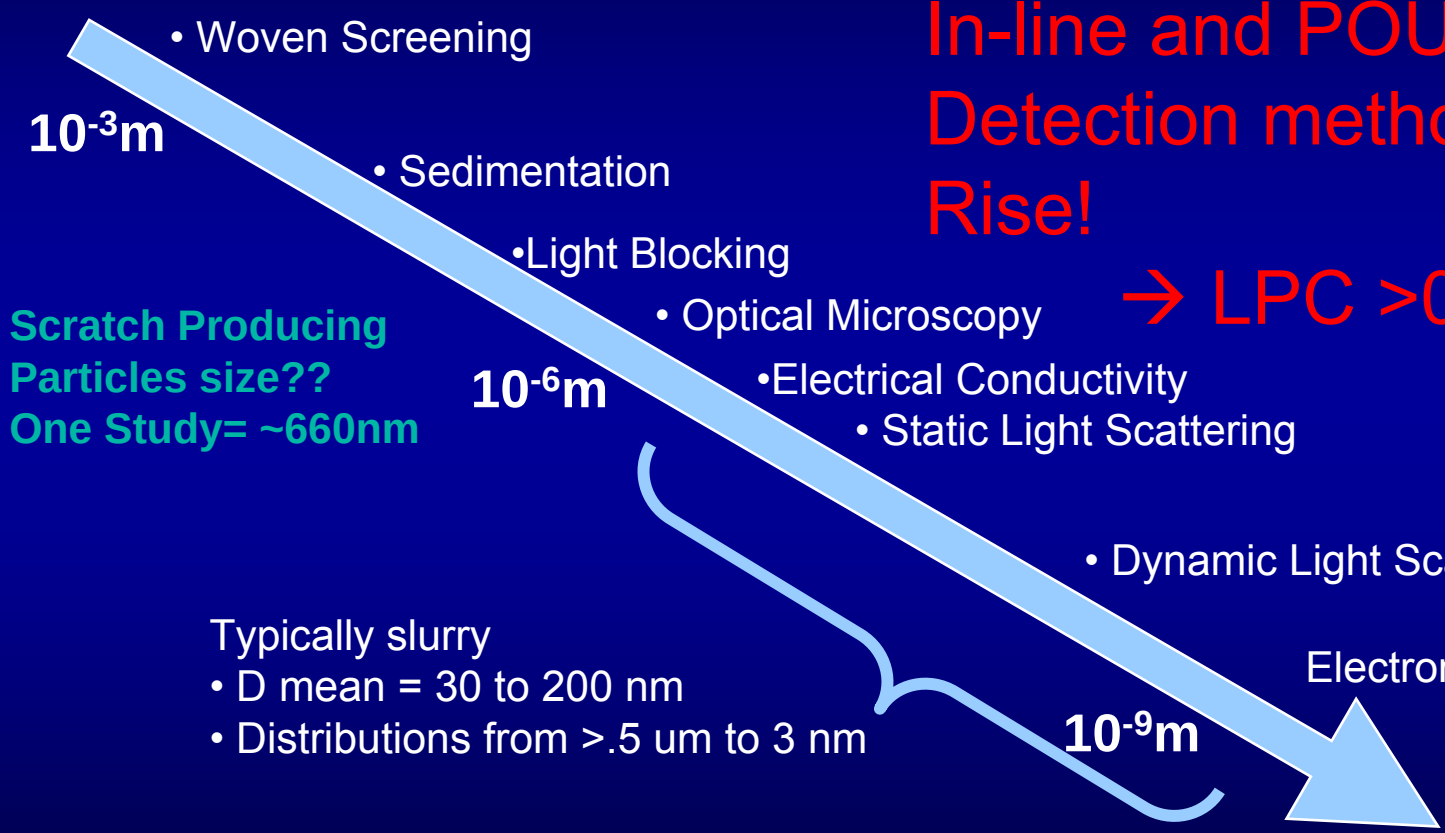
J. Lee & M. Moinpour, 2004 Spring MRS

Post CMP Topography: Critical Applications



Courtesy of G. Ding, Intel

Particle Sizing Techniques versus Lowest (best) resolutions



In-line and POU particle Detection methods on the Rise!

→ LPC >0.56 um

Scratch Producing Particles size?? One Study= ~660nm

Typically slurry
- D mean = 30 to 200 nm
- Distributions from >.5 um to 3 nm

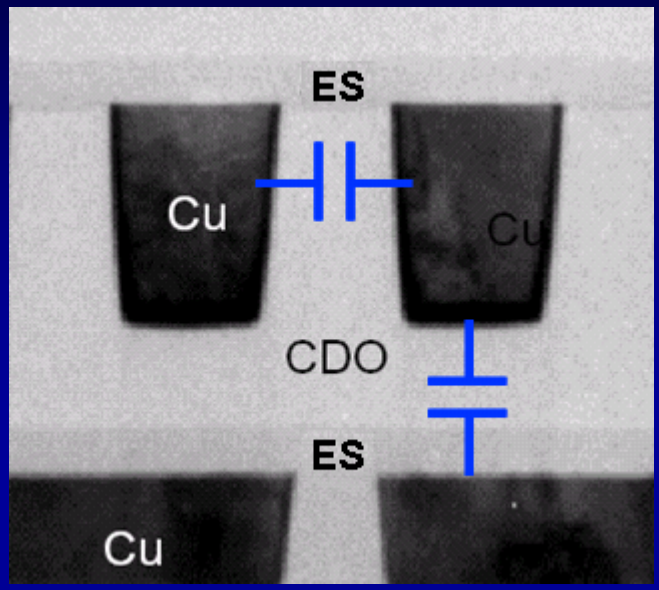
There is a continuing need for new, improved methodologies designed to analyze the particle properties critical to CMP

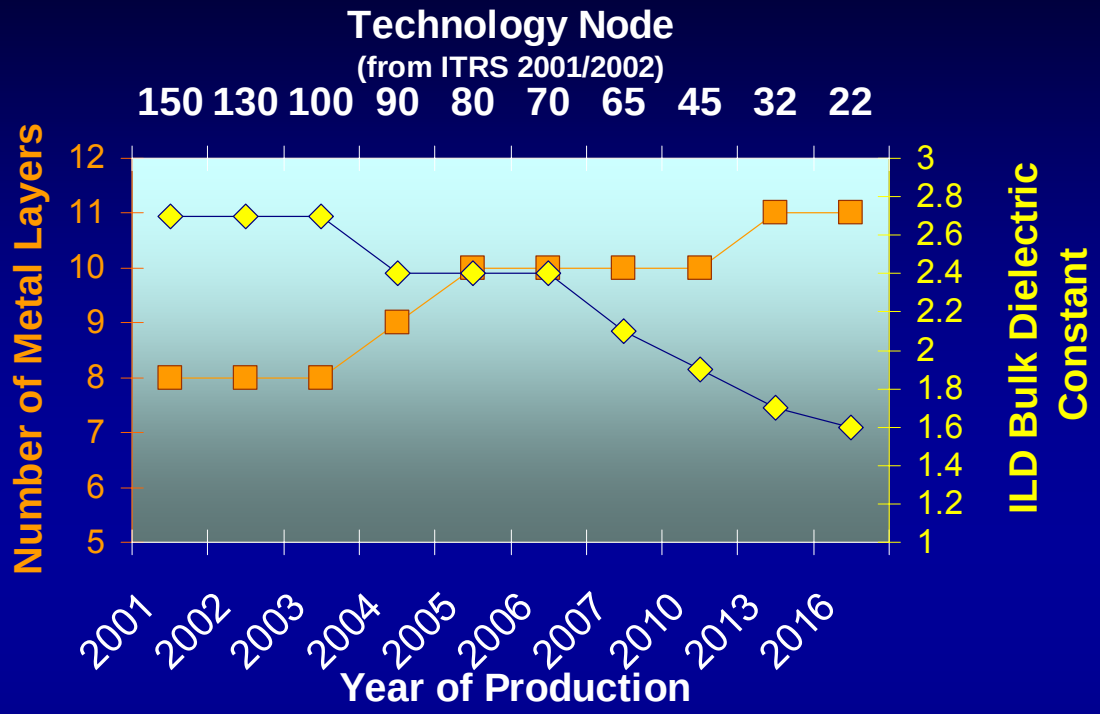
CMP: Fundamental Understanding

- **Fundamental understanding of CMP is still weak. Especially in areas of quantitative modeling with "C' contributions in CMP: chemical reactions, kinetics, and chemistry-related defects**
- **Need modeling that has predictive values to facilitate our understanding of new materials, consumables.**
- **Knowledge is primarily phenomenological and intuition-based, need to have a more systematic approach. A continued chance for academia to shine.**

CMP Fundamental Understanding:
Suitable domain for Universities & National Labs

Motivation for Low-K



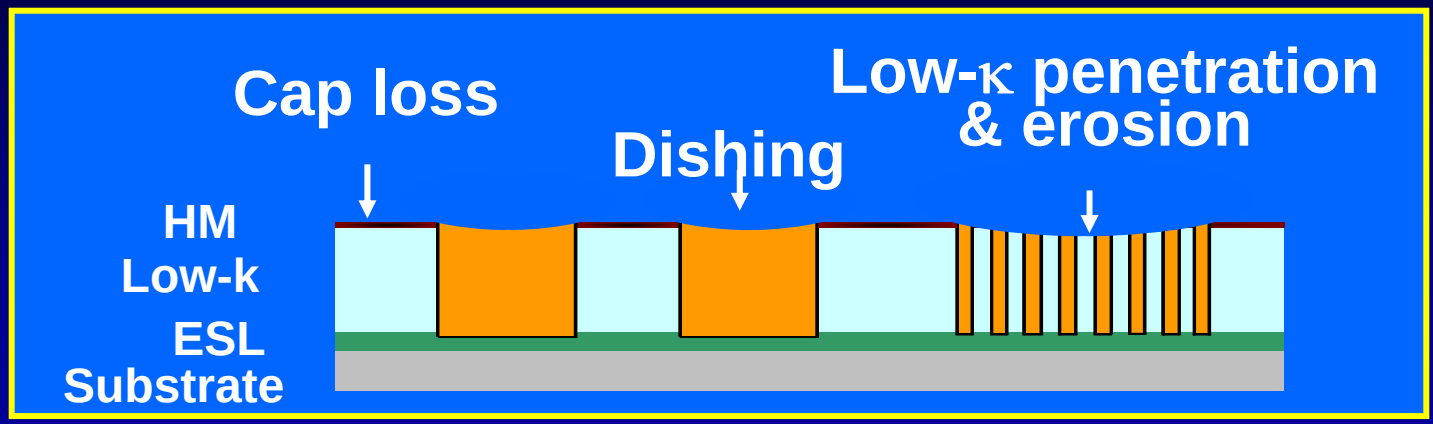


- Interconnect RC delay is now equal to or greater than front end delay effects
  - Cu provides lower R than Al, but cannot be reduced each generation
  - Power, cross-talk and delay must be minimized by reducing ILD capacitance (k)
- Main Approach to achieve lower K is Carbon Doping and/or to introduce porosity

J. Lee & M. Moinpour, 2004 Spring MRS

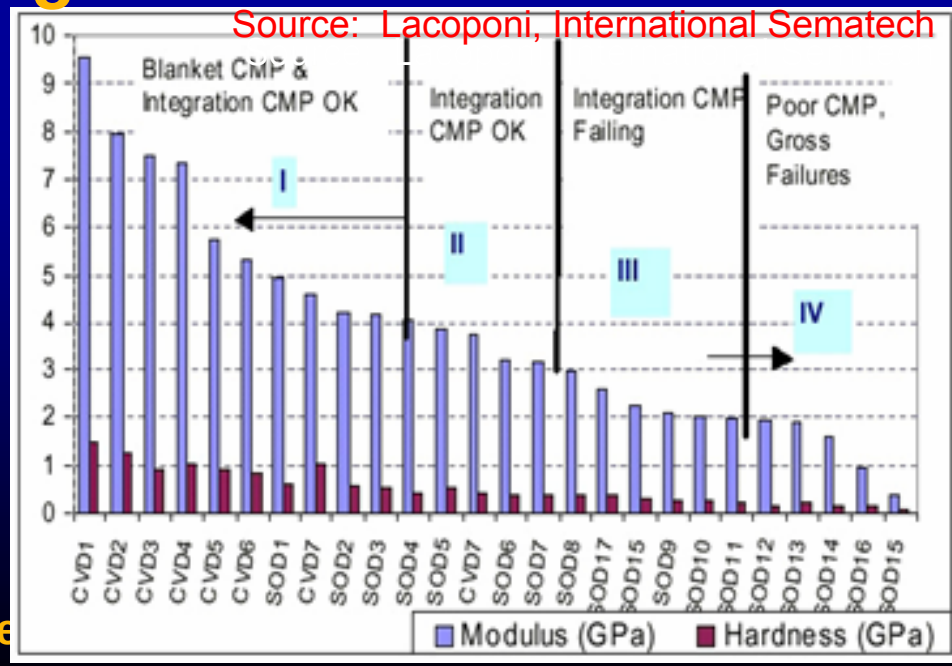
Scaling impacts on backend CMP

- Conventional Cu constraints

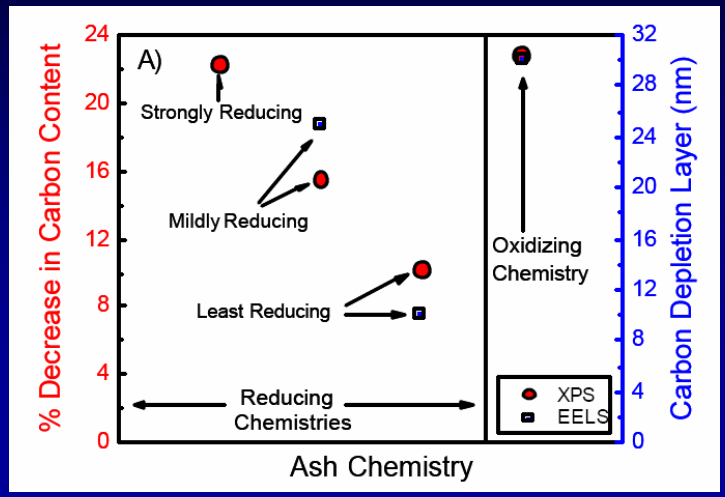


- Lower and ultra-low k bring additional excitement
  - –ILD loss control
  - –Defect concerns
  - –Mechanical integrity
    - Electro assisted CMP
    - Low P
    - Electropolish

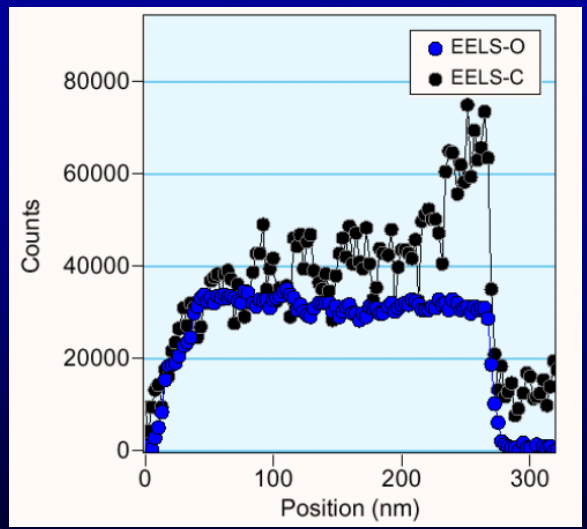
Source: Lacoponi, International Sematech



Challenges – Etch & Cleans



Dalton, *et al.*, 2004 IITC

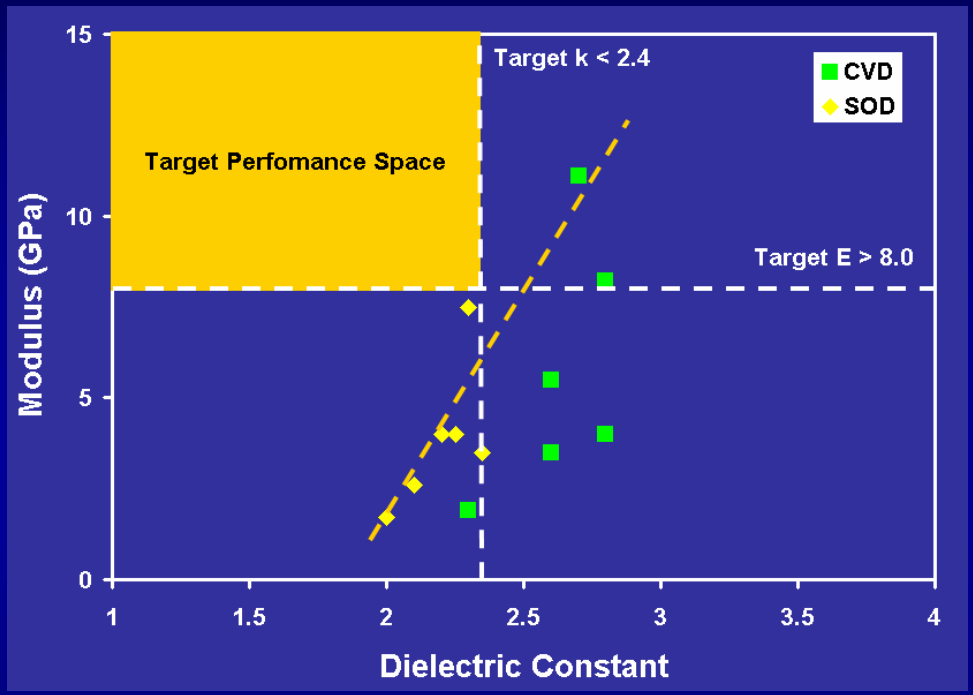


Dalton, *et al.*, 2004 IITC

- Dry etch → ILD damage → increase k
  - C depletion
  - Oxidation (introduction of –OH groups)
  - Film densification
- Wet etch → impact on k and film stability
  - Moisture uptake (significant k increase)

Need solutions to address both surface and bulk ILD damage

Novel Materials



Source: Data from IMEC evaluations, used with permission

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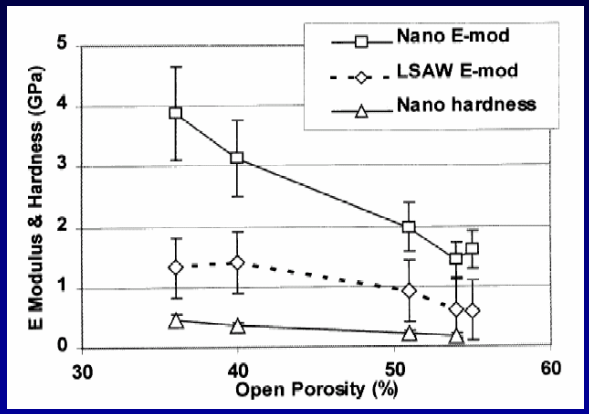
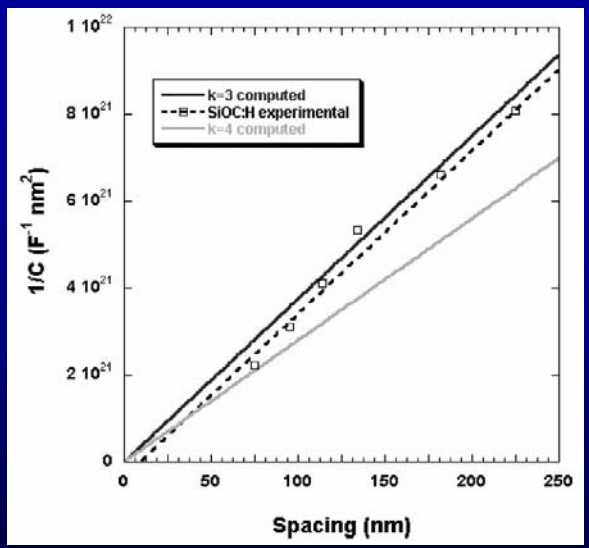
- Many CVD and SOD materials lie along (or below) same performance curve
  - Similar trends exist for hardness, cohesive strength
- Cure optimization is not sufficient to move into desired performance space

Need fundamental materials changes to enter new performance space

Metrology Development



Murray, *et al.*, Microelectronic Eng, 2002, 60, 133-141

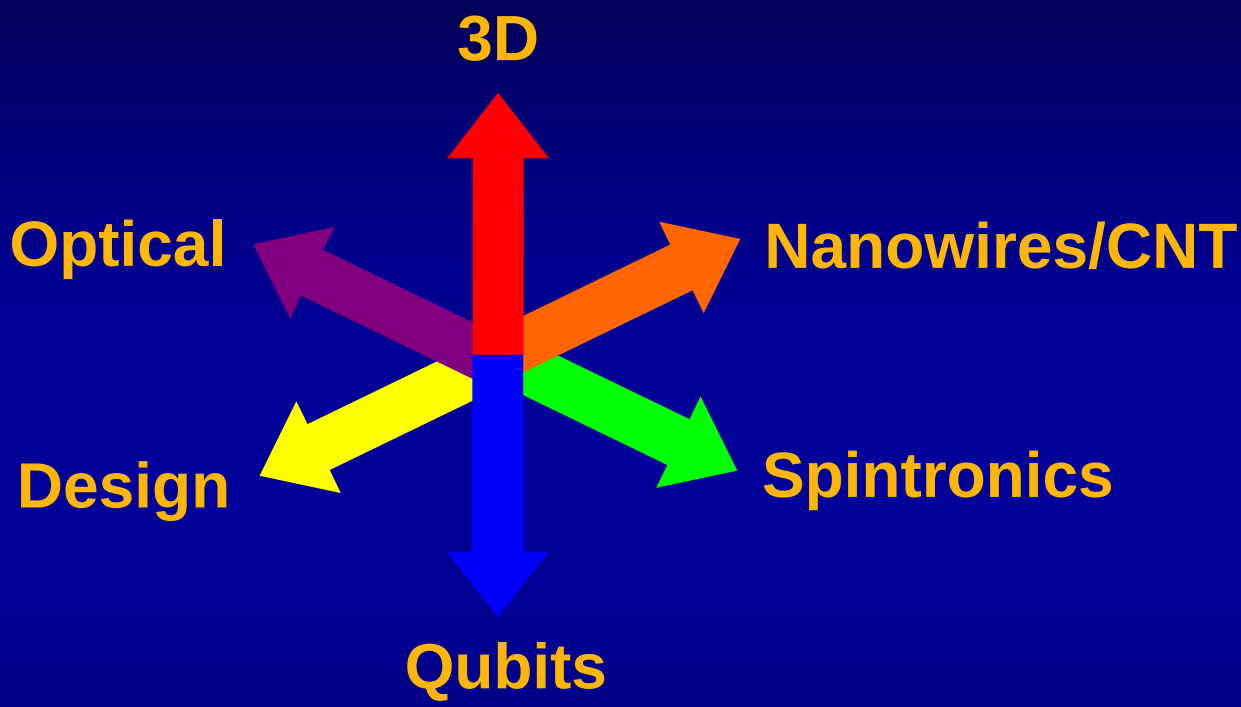


Iacopi, *et al.*, Electrochem Solid State Lett, 2004, 7, G79-G82

- Current methods for measuring mechanical properties
  - Require unrealistic film thickness
  - Give divergent results
- Dielectric damage and pore sealing require new techniques
  - HF decoration is qualitative only
  - EELS and e-test are time-consuming
  - E-test requires full patterning and passivation
- Fab-based real-time characterization techniques will provide significant benefits

New fab-based metrologies are needed for film screening and process control

Beyond Cu / Low k Scaling ?



• Needs should drive choice with **large impact and appropriate timing**.

Introduction – CNT Interconnects

- interconnects are key determinants of chip performance
- resistivity of Cu interconnects increases as dimensions decrease and hence poses a scaling and latency challenge
- SWNT exhibit ballistic electron transport with elastic scattering length up to 2 μm
- resistance of an ideal quantum wire is a multiple of e^2/h; the conductance of SWNT is $4e^2/h$; this corresponds to a resistance of 6.8 kΩ

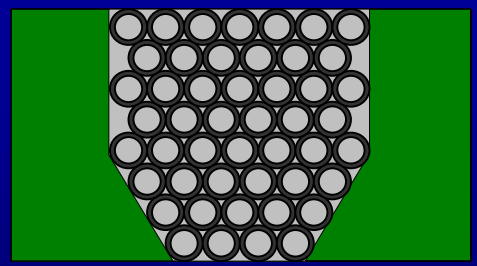
SWNT: 

$R_c = 6.8\ k\Omega$

Bundle of SWNT:

$R_c = 6.8/n\ k\Omega$

n … number of SWNTs in the bundle



- SWNT, current density without failure: 10^9 A/cm^2 (Cu 10^6 A/cm^2)
- SWNT: good mechanical stability (strength and toughness); enables new interlayer dielectric solutions

Courtesy of F. Gstrein & V. Dubin, Intel

Summary

- Silicon Nanotechnology is production reality and follows Moore's law
- New materials are needed for future technologies
  - Not much done/reported in CMP of new materials
- New Metrology needed for 32nm and beyond
- Pore Sealing, damage repair and controlling line resistance are among key challenges in conventional Cu/Low Integration schemes.
- Various options are being explored beyond Cu/Low K

Nano-material Innovation is Needed…..

QuickTime™ and a
TIFF (Uncompressed) decompressor
are needed to see this picture.

QuickTime™ and a
TIFF (Uncompressed) decompressor
are needed to see this picture.

Real-time measurements of pad deformation under the wafer during polish

Chris Rogers

Jon, Chris, Joe, Dewi, Jesse, Alicia, Ed, Scott, Cappy, Dan, Jim, Nicole

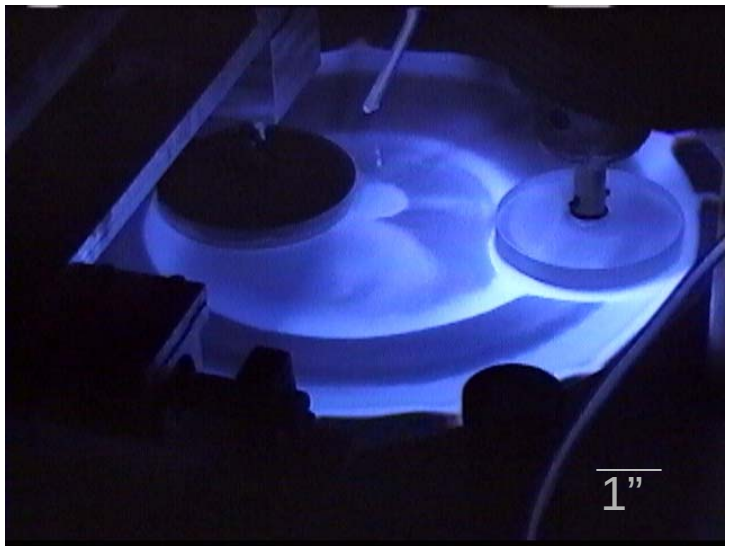
and

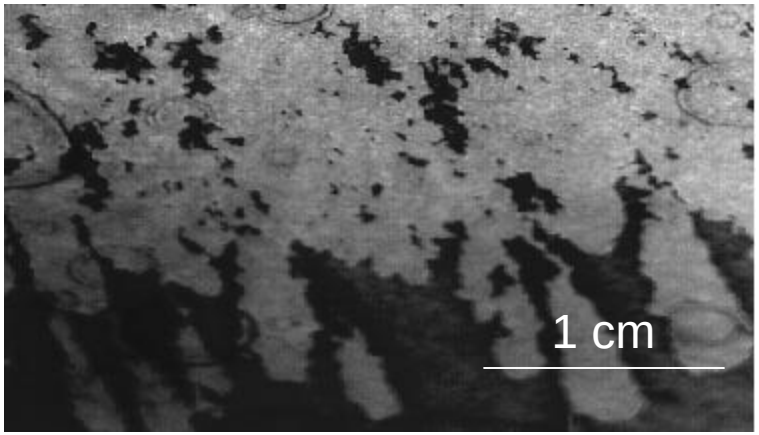
Vincent Manno, Ara Philipossian, Mansour Moinpour, Chris Barnes,Sam Anjur, Frank Kaufman

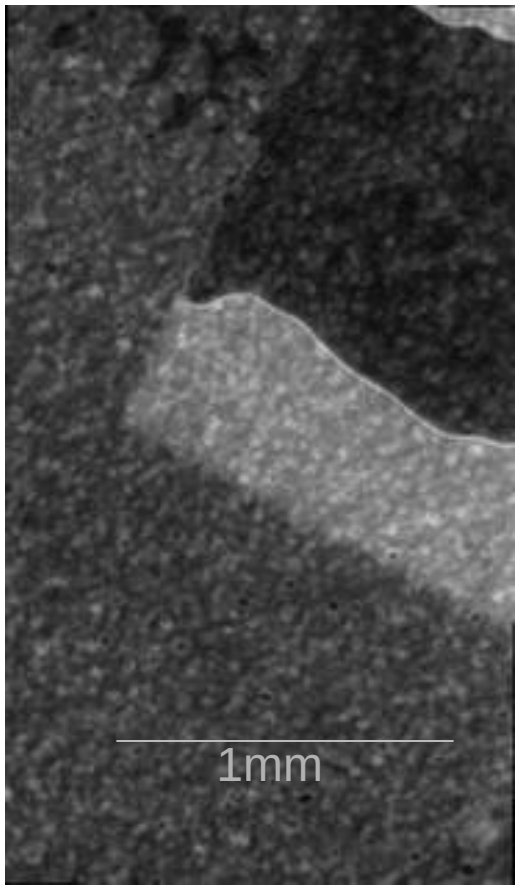
Cabot Microelectronics

intel

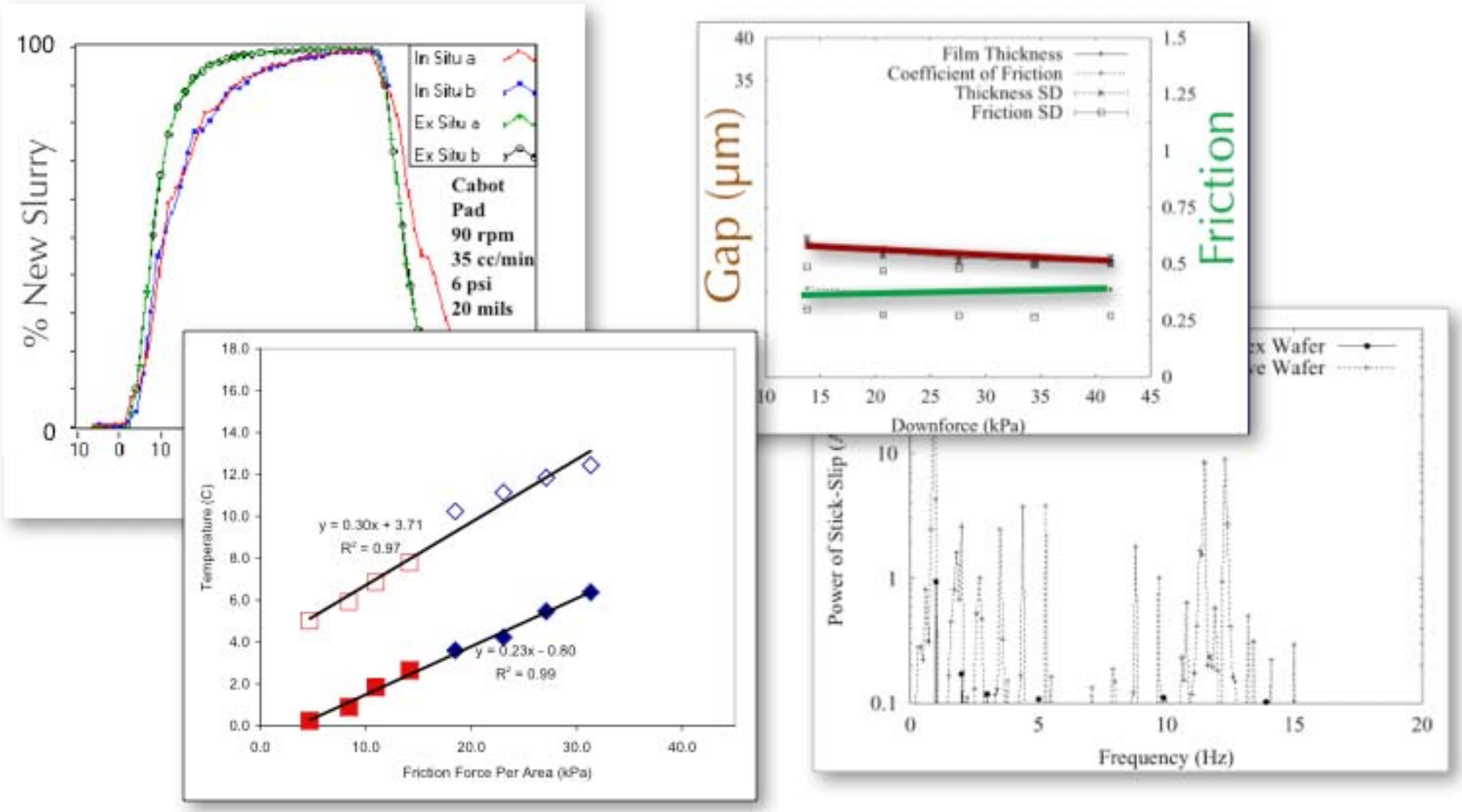
What are we looking at?



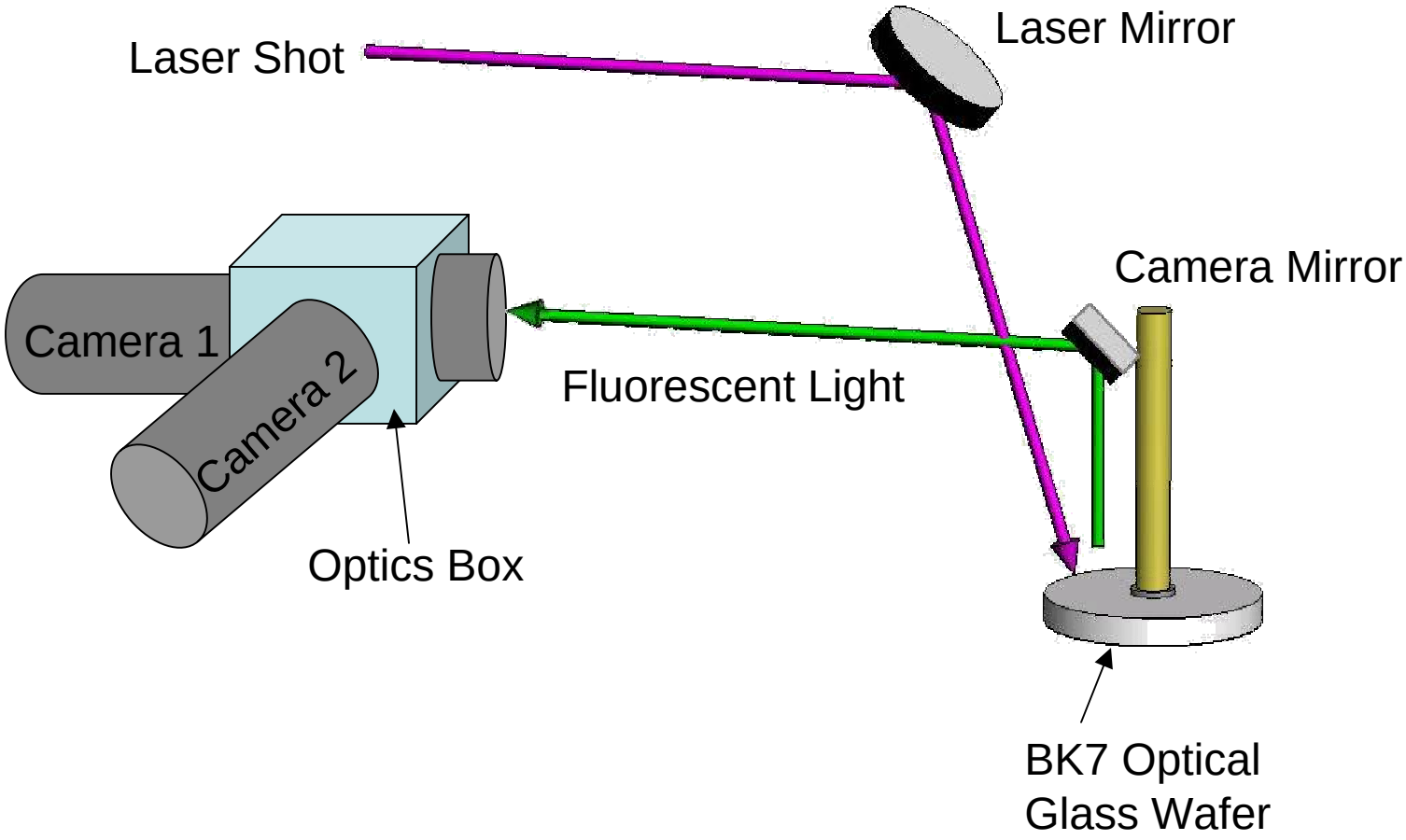




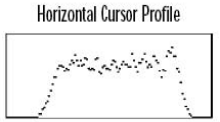
What have we seen?

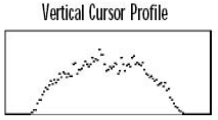


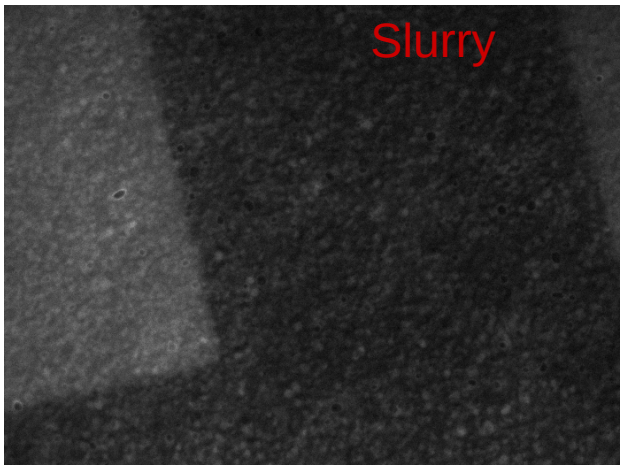
DELIF: How we see it

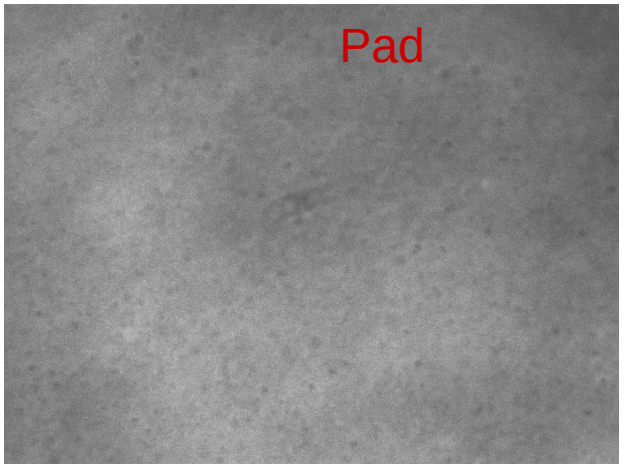


DELIF 2









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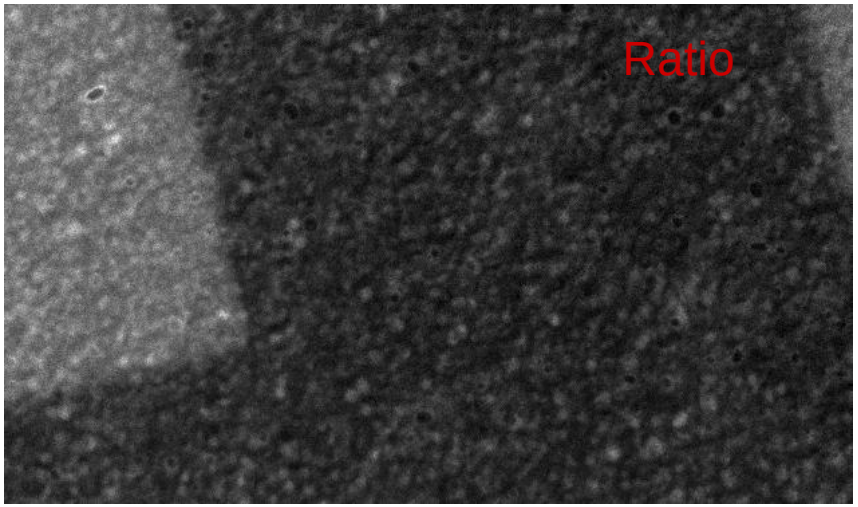


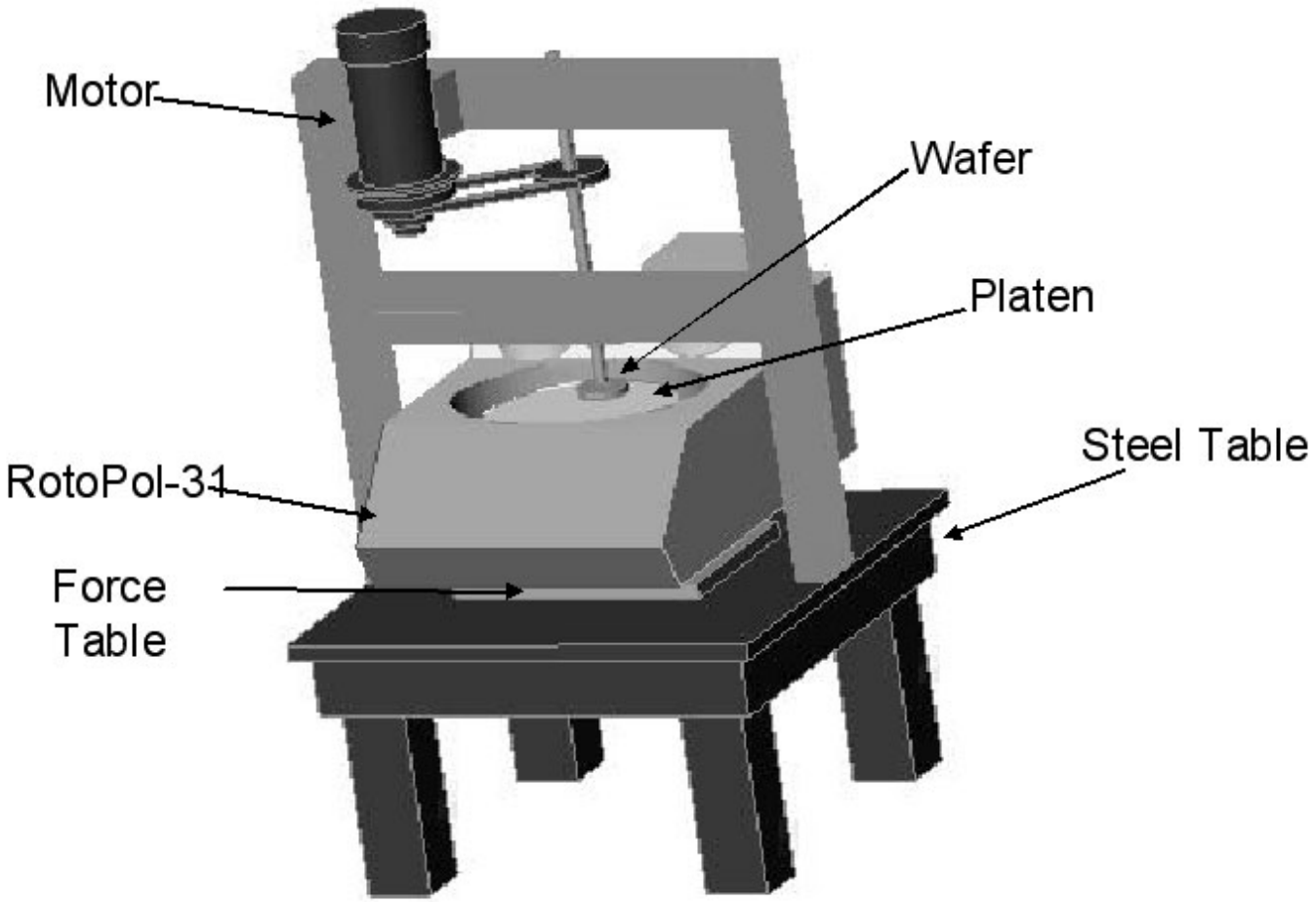
Division of 2 images cancels variations in image source intensity

Issues

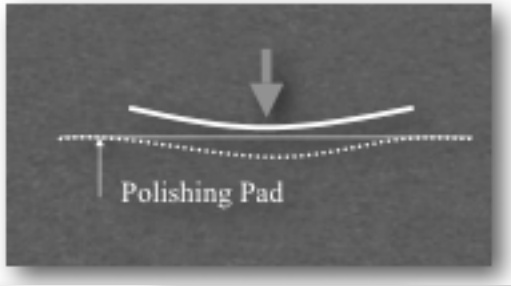
QuickTime™ and a
TIFF (LZW) decompressor
are needed to see this picture.

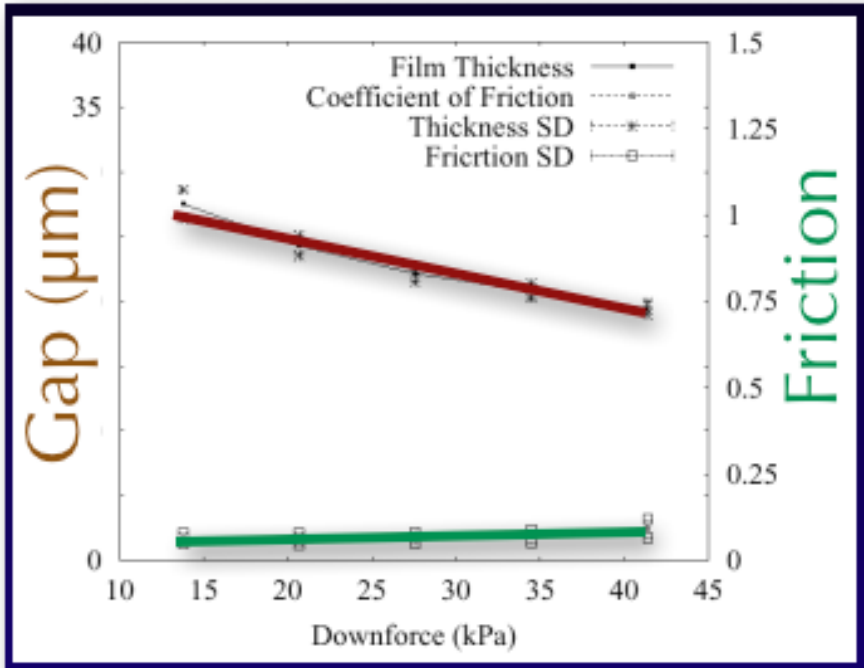
- Systematic Errors
  - I. Dyes have similar emission spectrum
  - II. Dye 1 absorbs emission from Dye 2
  - III. Emission is a function of the scalar
- Photo-bleaching
- Photo-degradation on the pads

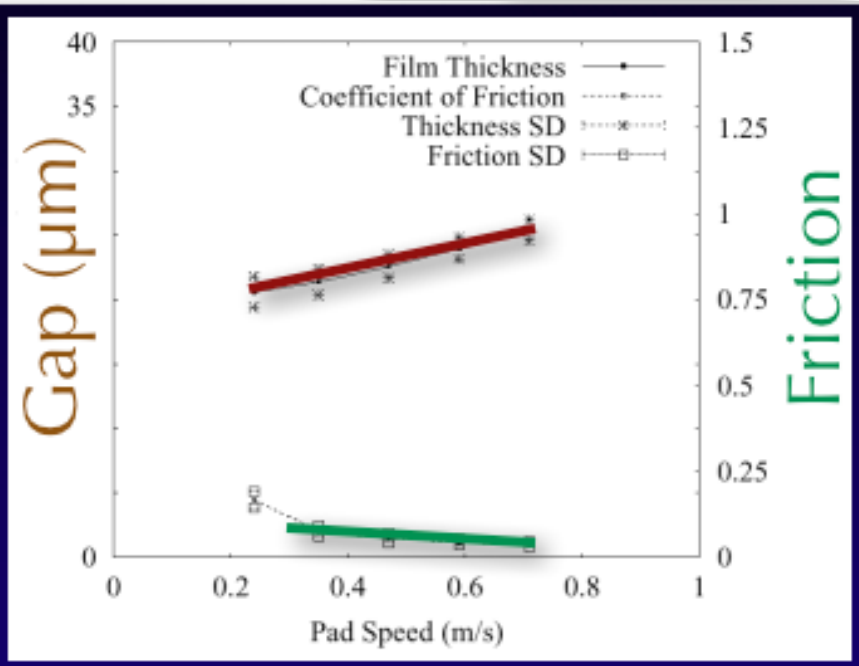
Rig



Friction







$F_{df}\uparrow \Downarrow h\downarrow$

$\Downarrow C_f\uparrow$

60 rpm (0.47 m/s) pad speed

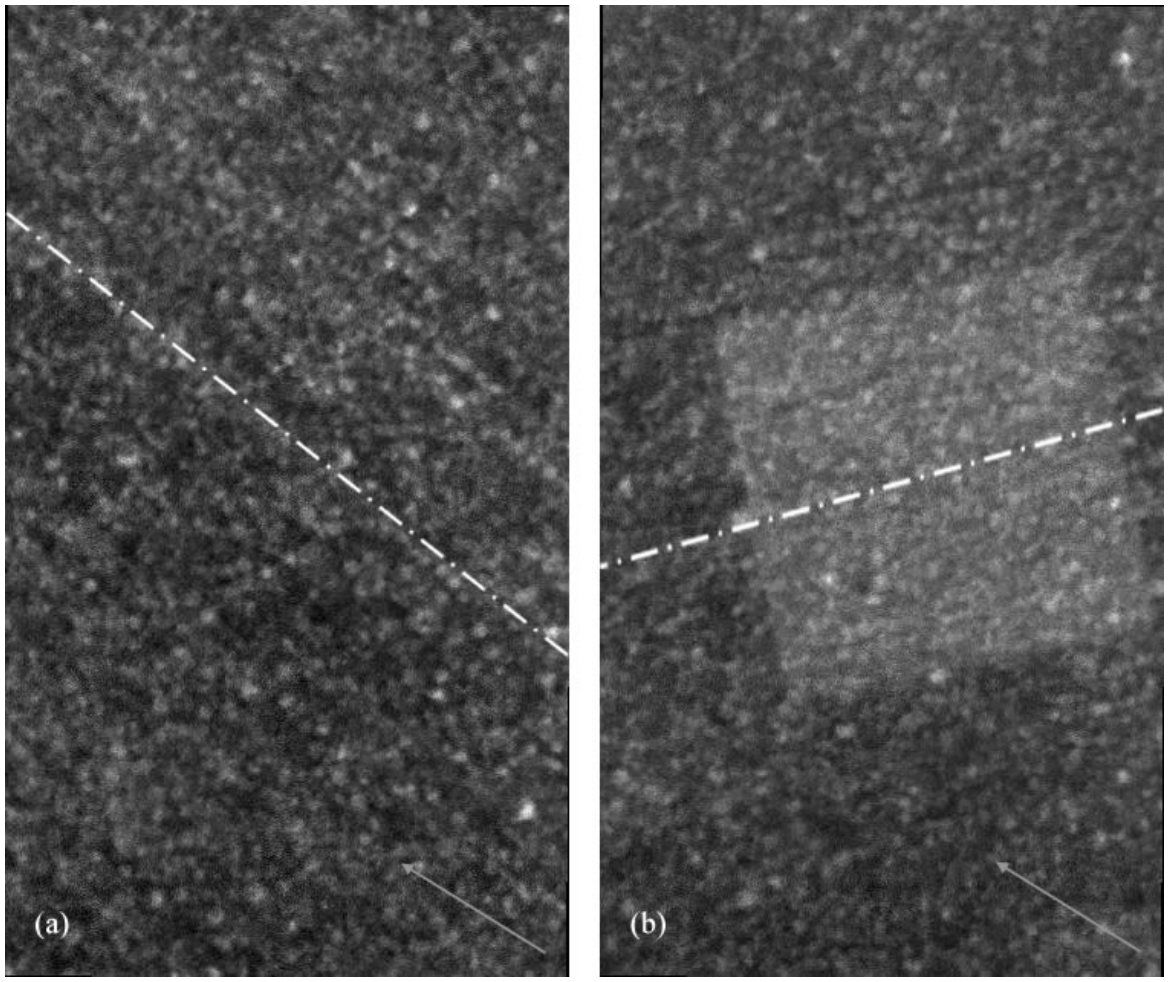
$U\uparrow \Downarrow h\uparrow$

$\Downarrow C_f\downarrow$

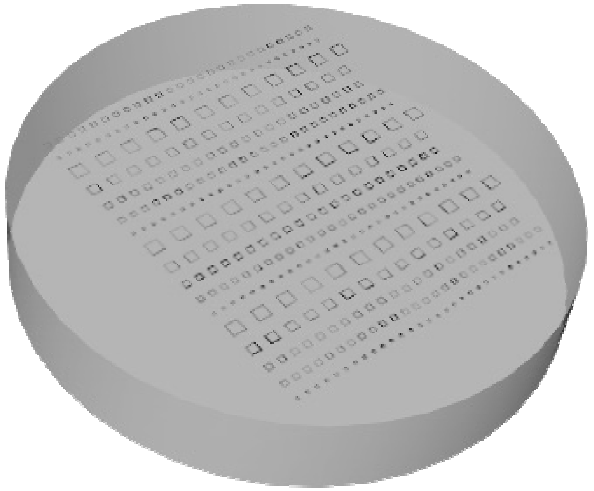
4 psi (27.6 kPa) downforce

-Average of 3 data sets

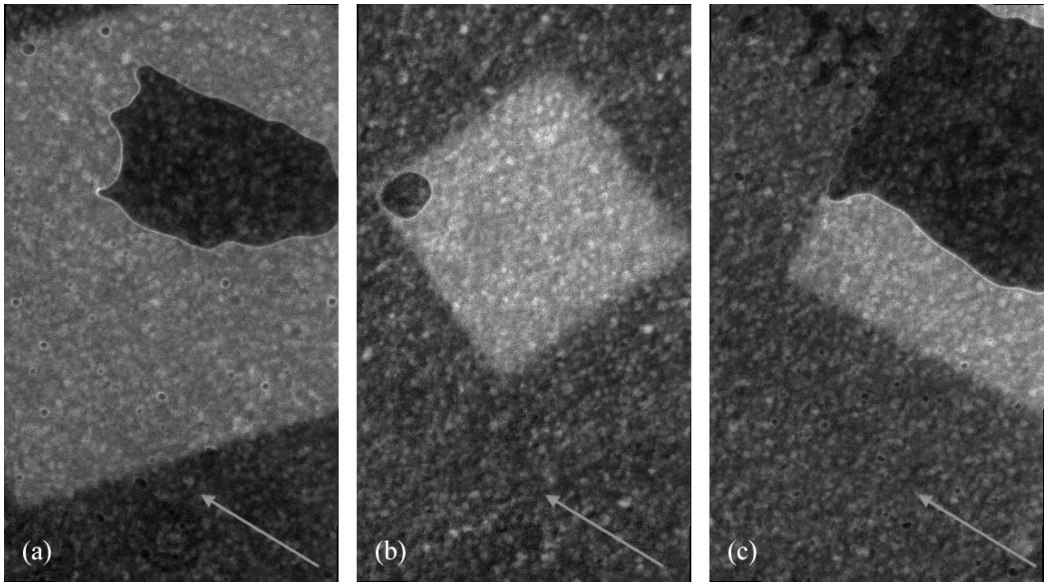
Under the Wafer: Conditioner



(a) Flat wafer
(b) 14 um deep 1mm^2 square well

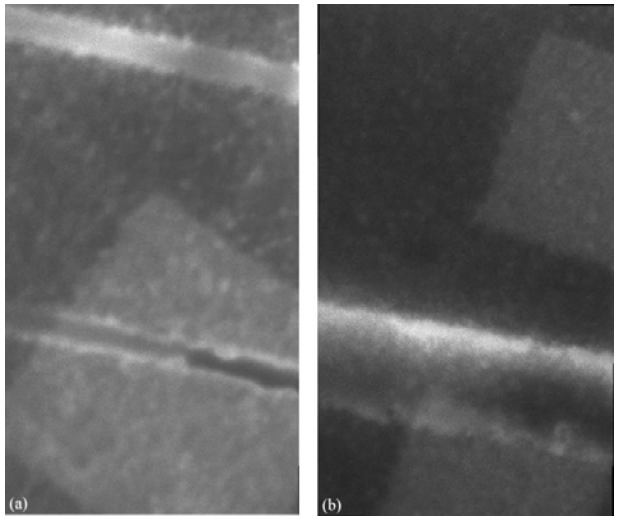


Under the Wafer: Air Pockets



Low Resolution

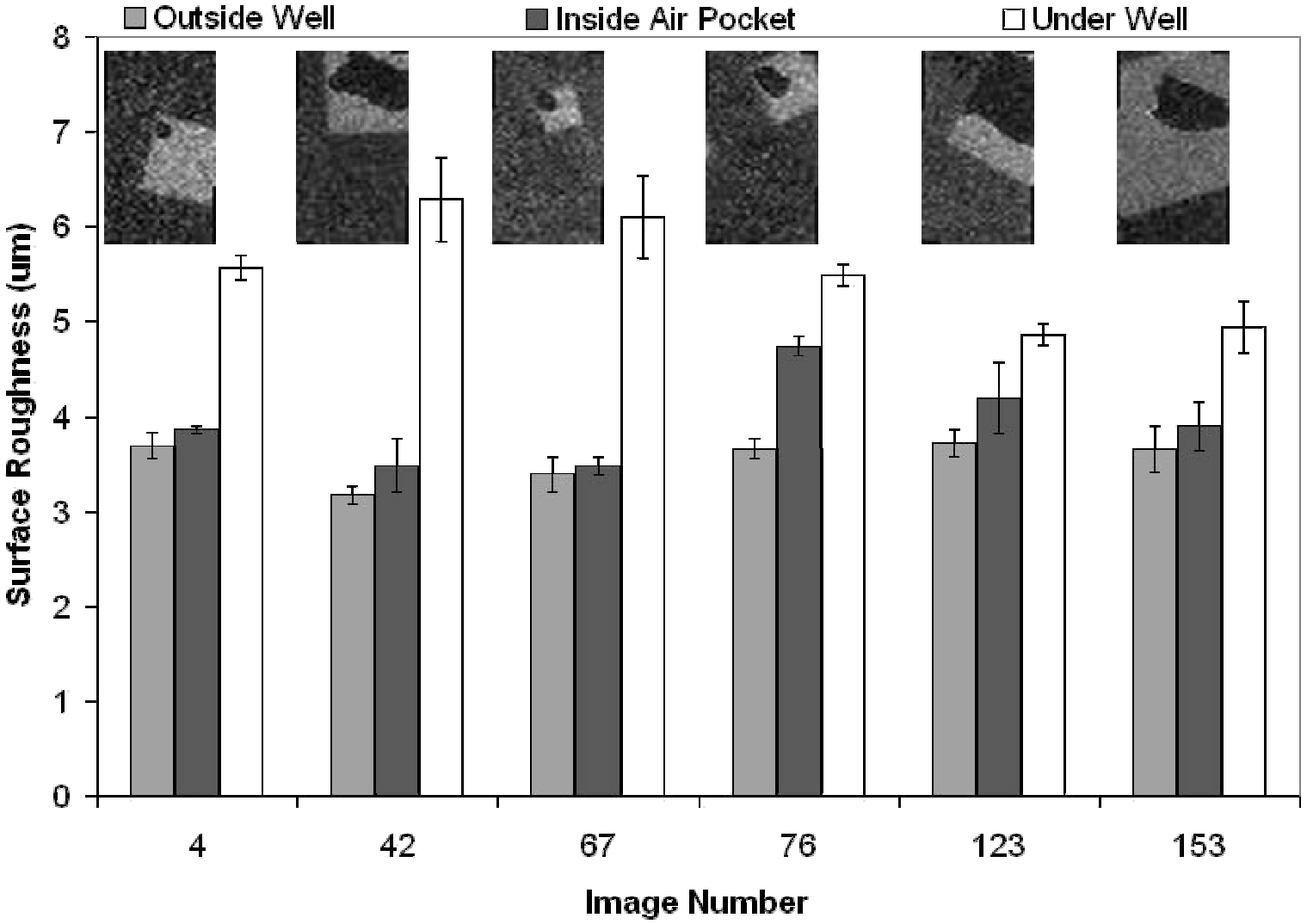
High Resolution



Air pockets get trapped in features

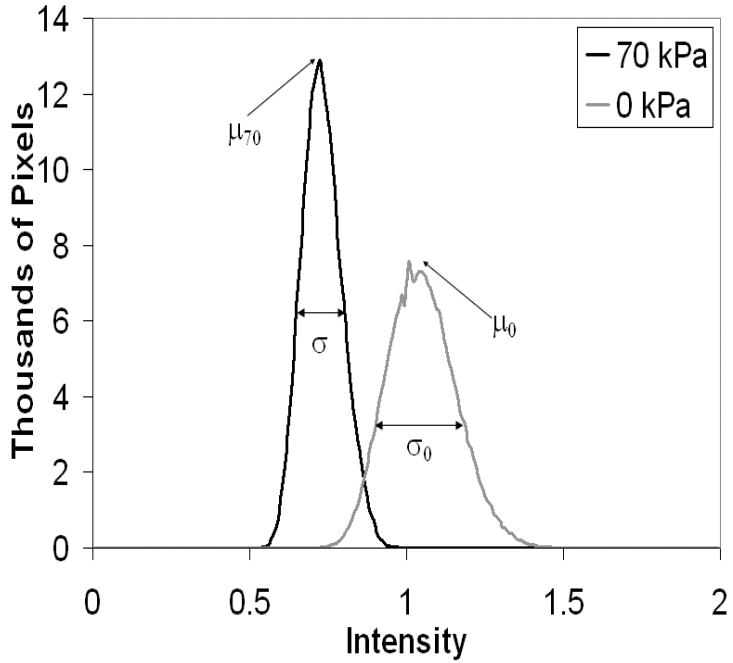
Grooves help to transport air pockets under the wafer features

Roughness


Outside Well
Inside Air Pocket
Under Well
Surface Roughness (um)
0
1
2
3
4
5
6
7
8
4
42
67
76
123
153
Image Number

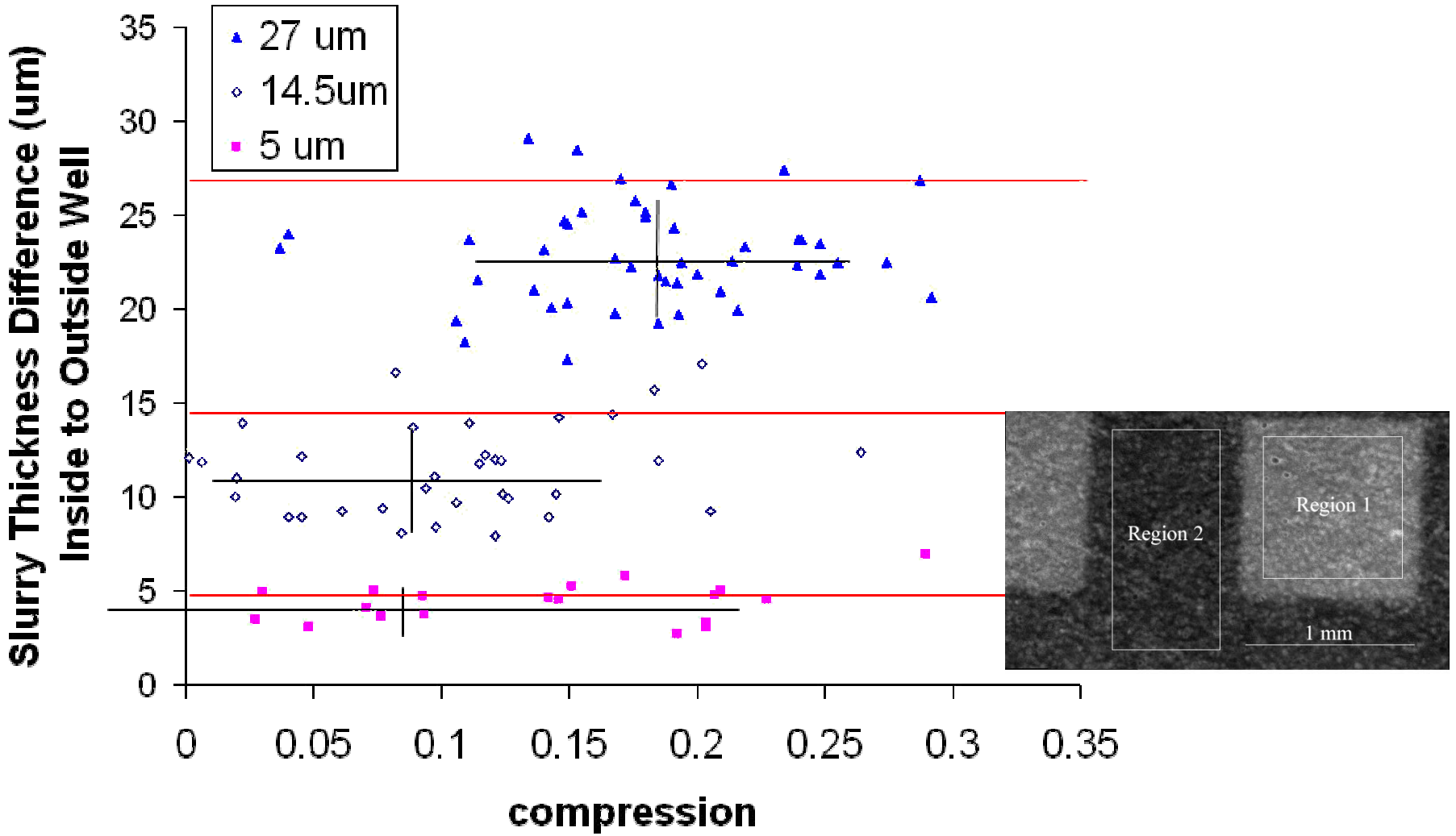
Roughness variation

- *asperity size distribution = fluid layer thickness distribution*
- *Standard deviation comparison → pad compression*
- *Peak location → fluid layer thickness.*
- *Compression factor: e*

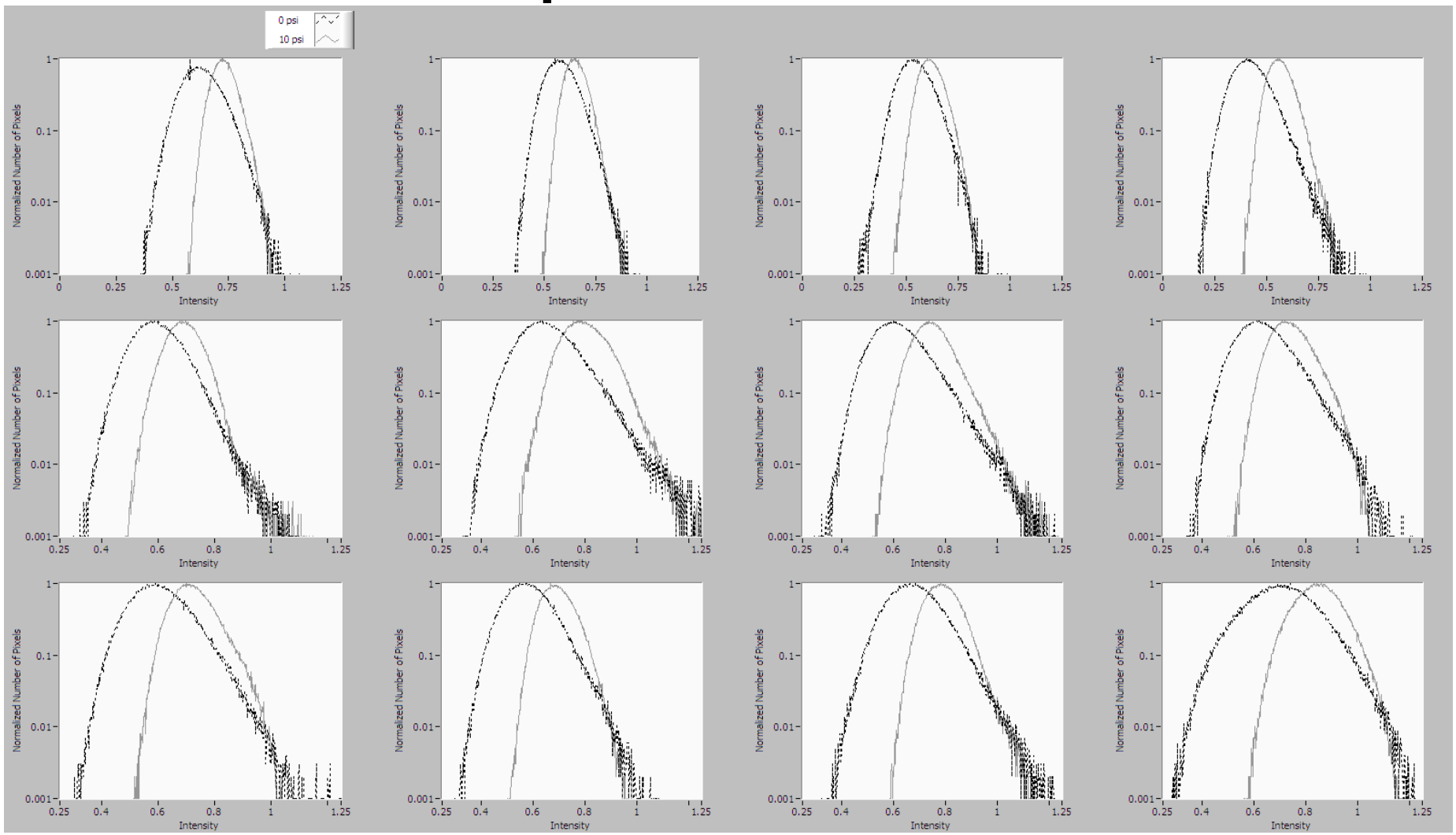


$$\varepsilon = \frac{\sigma - \sigma_0}{\sigma_0}$$

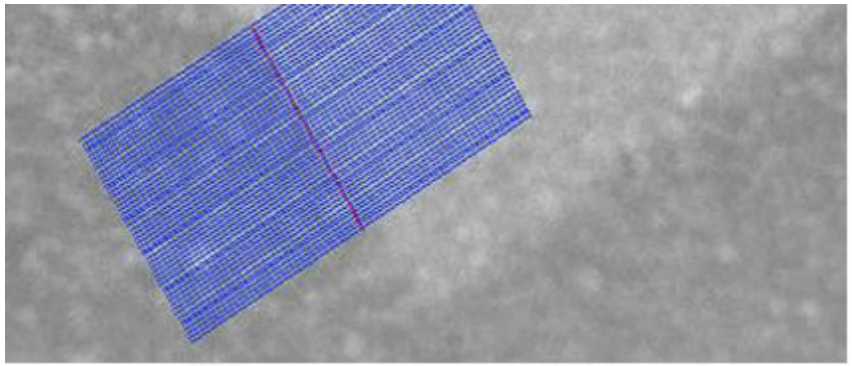
Pad Compression

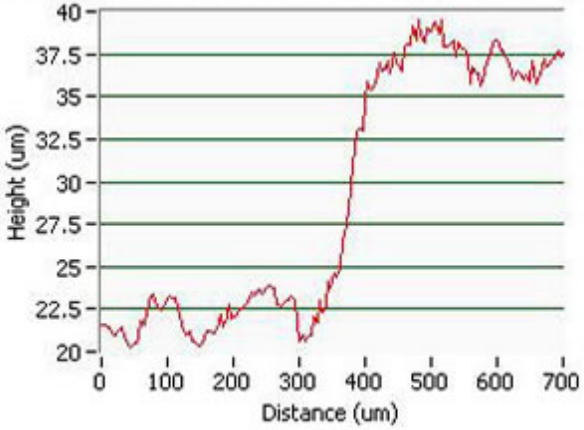


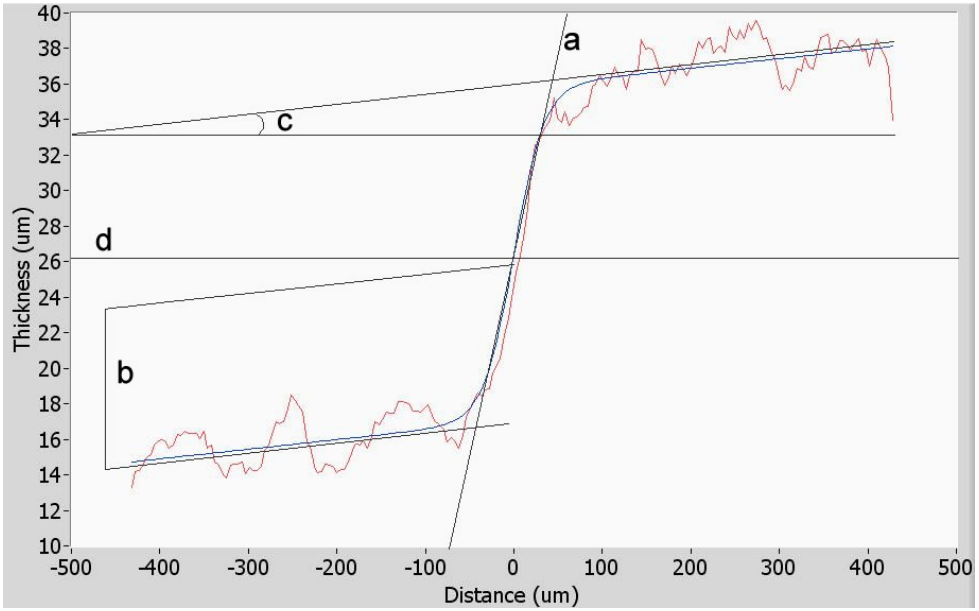
Sample Variations



Feature Effects







$$y = btanh(ax) + cx + d$$

Conclusions

- Can measure real-time, in-situ pad deformation
- Can we understand asperity behavior?
- Can we relate to polish?
- What is contact?
- Can we correlate friction (macro) with images (micro)?

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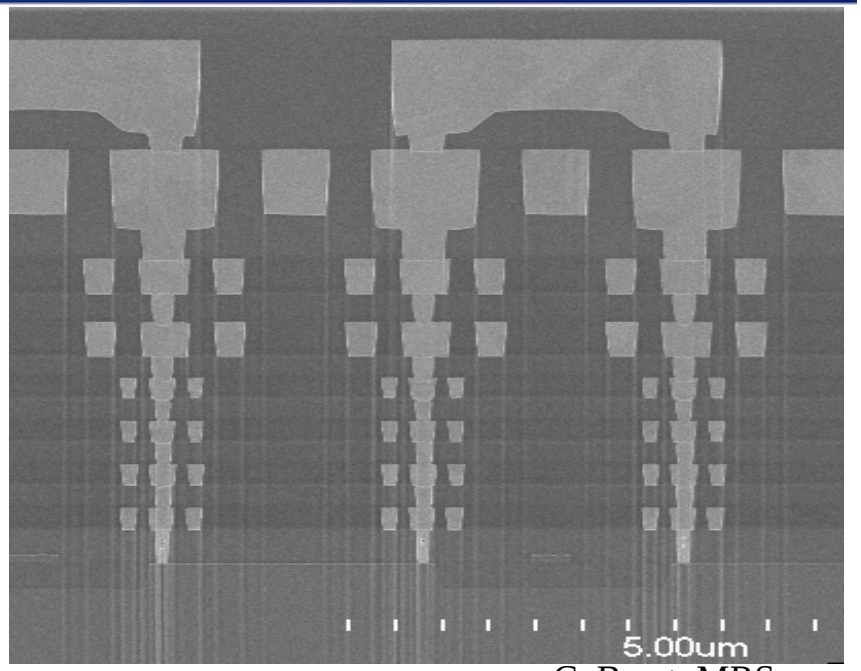
CMP: A Technical and Commercial Perspective

Cliff Spiro
VP Research and Development
Cabot Microelectronics
February 23, 2006

CMP Industry Demographics: Transition/Change

Growth Drivers

- More Wafer Starts
- More Layers
- More sub 250 nm Chips
- Strong Memory, Foundry Growth
- New Materials– Ru, GST, UlowK
- Complex Integration and Patterns
- 45,33,22 nm



C. Borst, MRS Proceedings

Growth Detractors

- More Global Competition
- Greater Customer Leverage
- Acute Customer Focus on Consumable Costs
- Greater Polishing Efficiency/300mm
- Disruptive Technology

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Cabot Microelectronics Approach

- Continue to Drive CMP Slurry Performance For All Materials and Nodes
- Invest Heavily in R&D $45 million/yr
- Develop Platforms With Built-In Tunability For Customization
- Globalize R&D to Get Closer to Our Customers
- Establish Joint Developments With Key Customers and Suppliers
- Expand Basic Research In House and at Universities
- Greater Emphasis on Cost and Quality and Supply Assurance
- Six Sigma and Design for Six Sigma
- Move Aggressively Into Technology Adjacencies
    - Pads
    - Engineering Surface Finish: CMP For Non- Microelectronics

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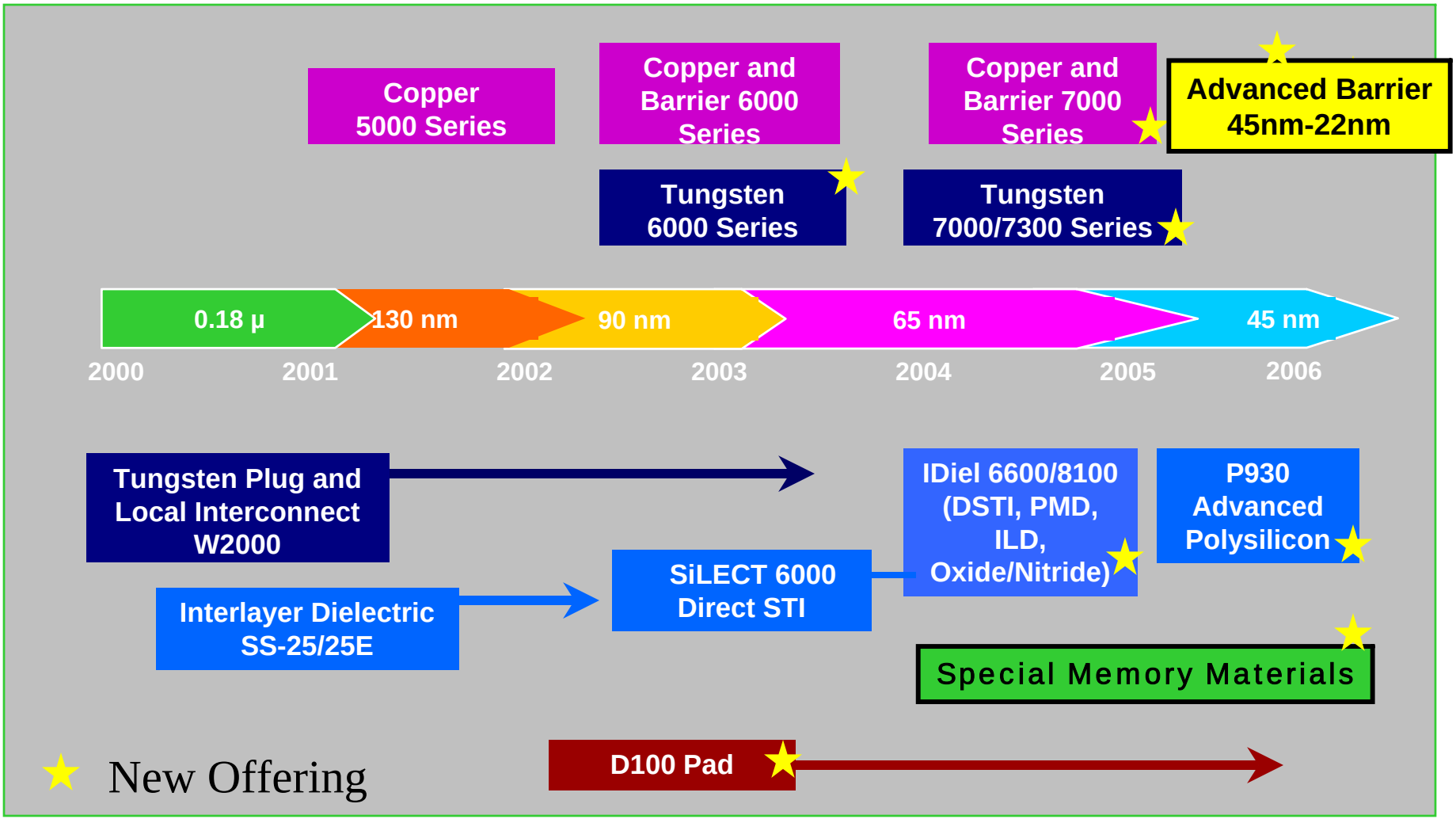
CMC Product Roadmap



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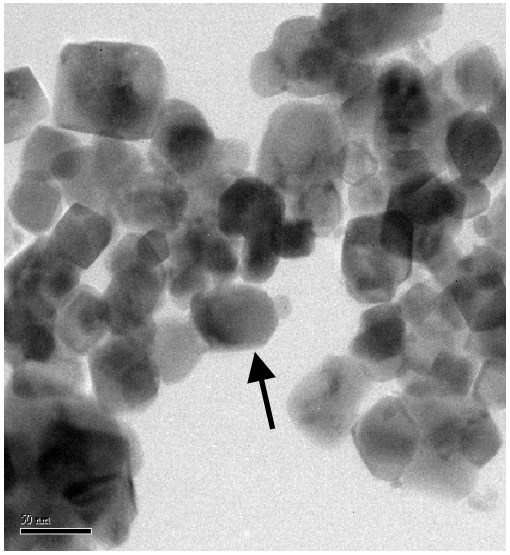
Nano-Ceria For Ultra-Low Defectivity

To Lower Defect Count

- Rounded Edge and Corner
- Narrow Particle Size Distribution

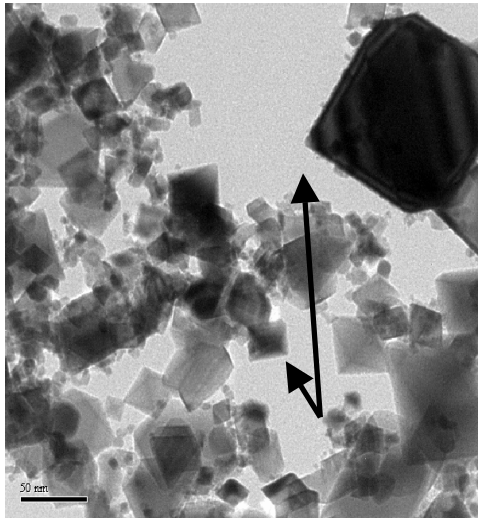
Ceria A



Scale = 50 nm

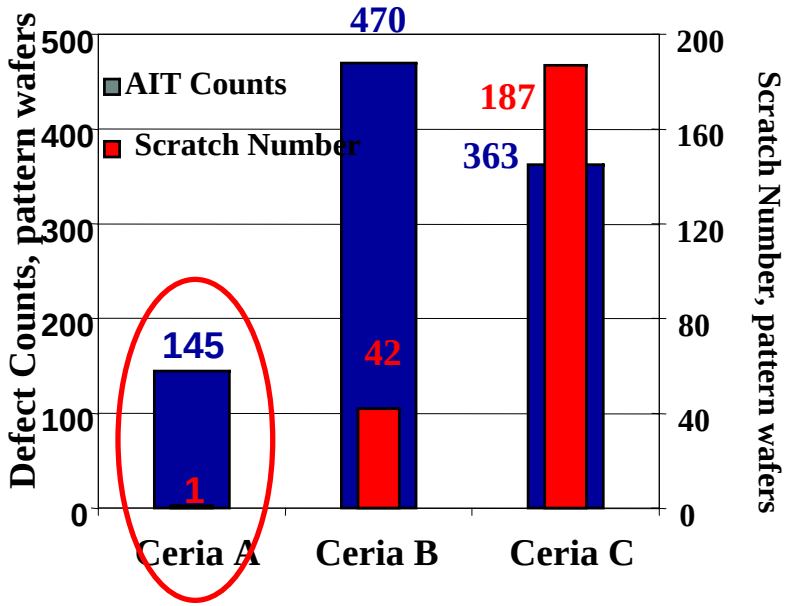
Small, uniform particles with rounded edges

Ceria B



Scale = 50 nm

Large, uncontrolled particles with sharp edges



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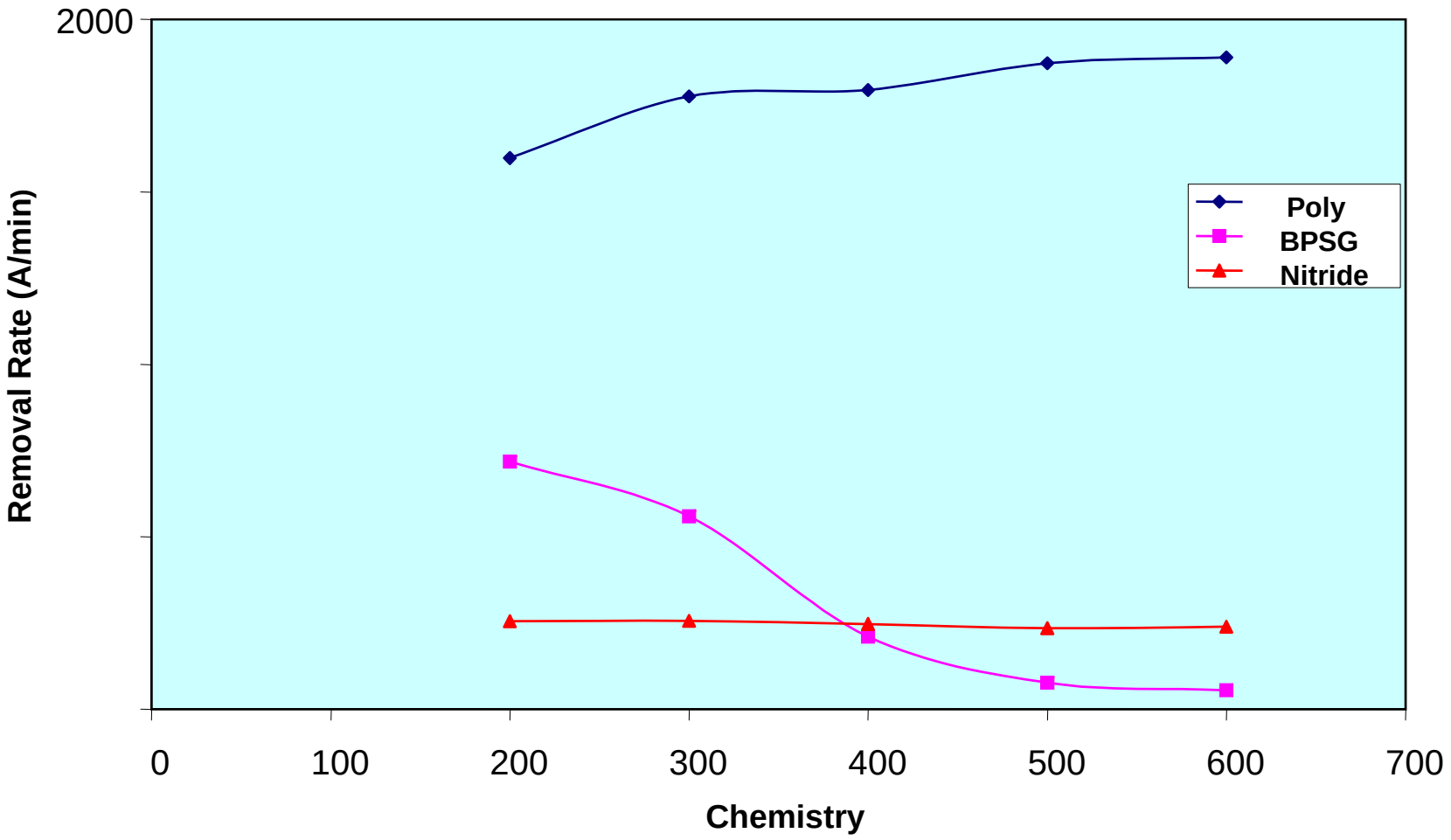
Selective Poly Slurry



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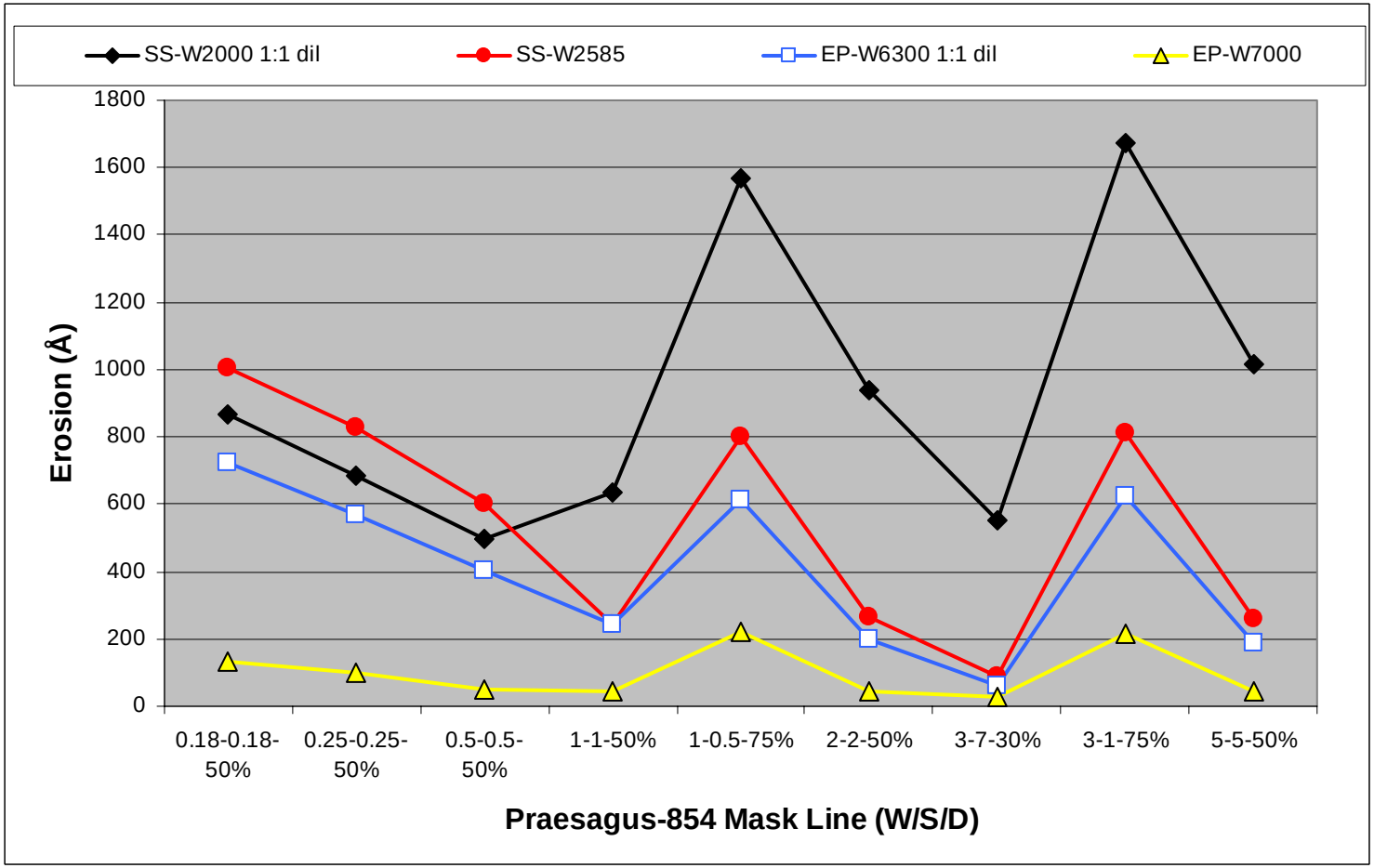
Significant Improvement in Tungsten Erosion



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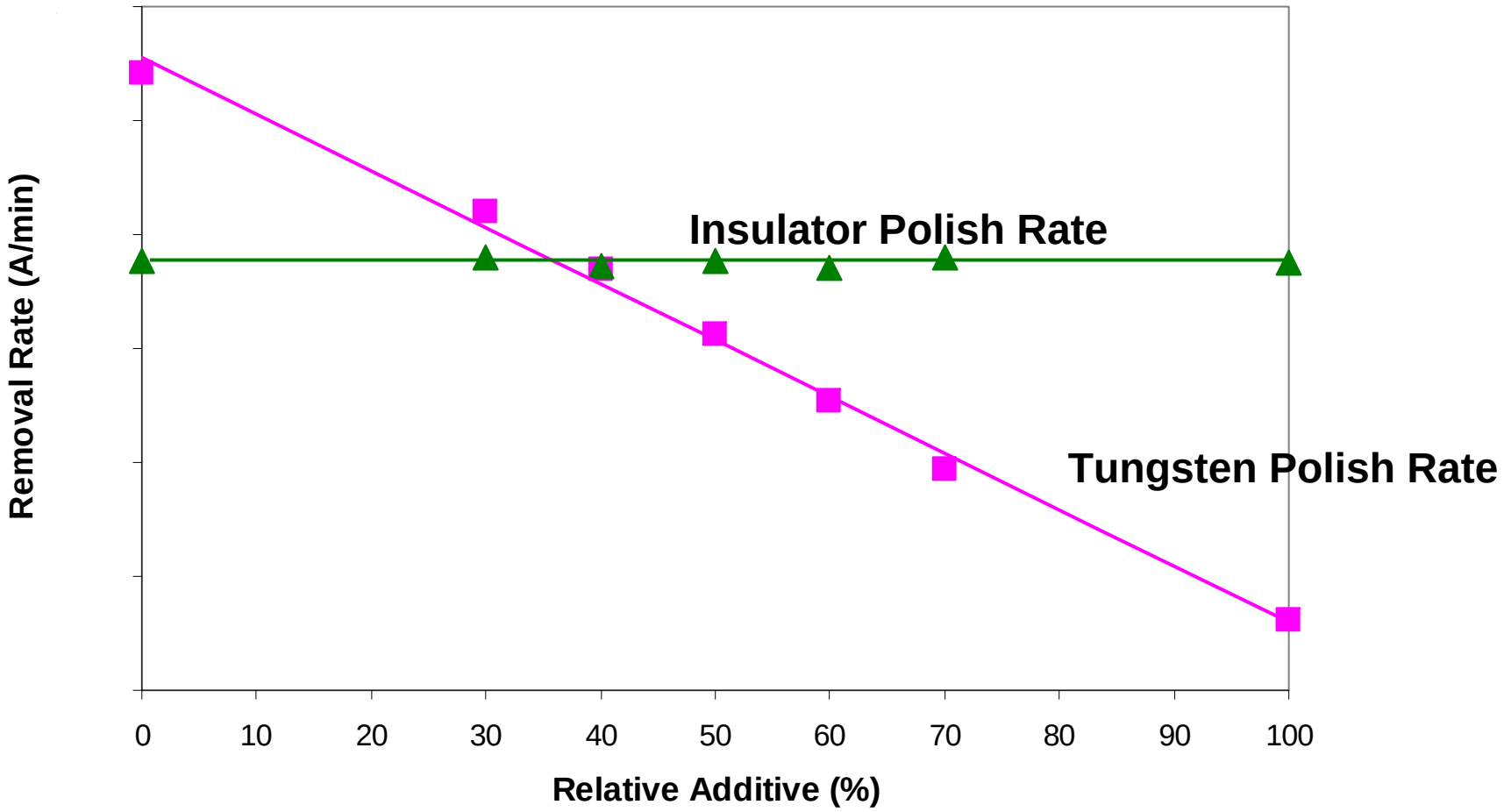
W7300: Tungsten / Oxide Tunability



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Cabot Microelectronics New Pad- D100

Low Cost
Long Life
High Performance

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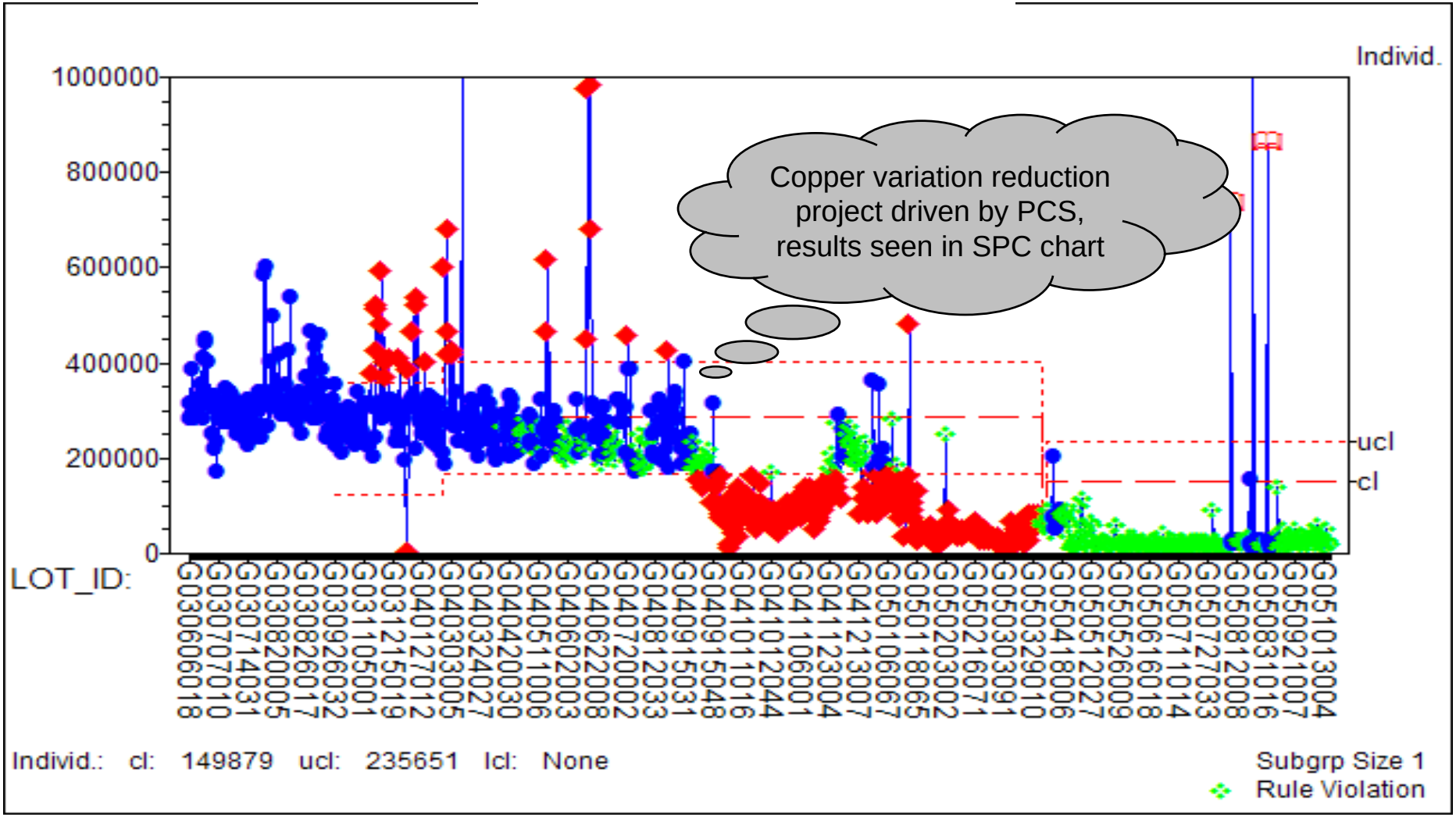
Six Sigma For Variation Reduction



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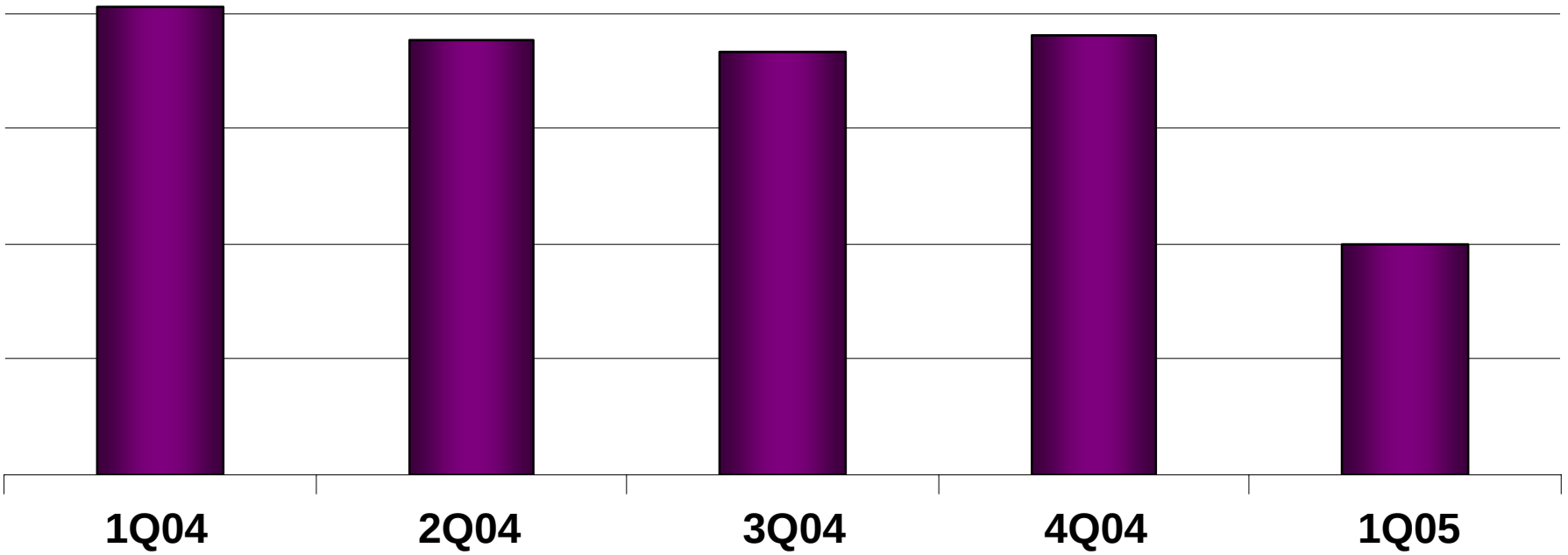
Six Sigma and Wafer Cost Reduction: Table Top Plus DOE Yield Savings and Efficiencies



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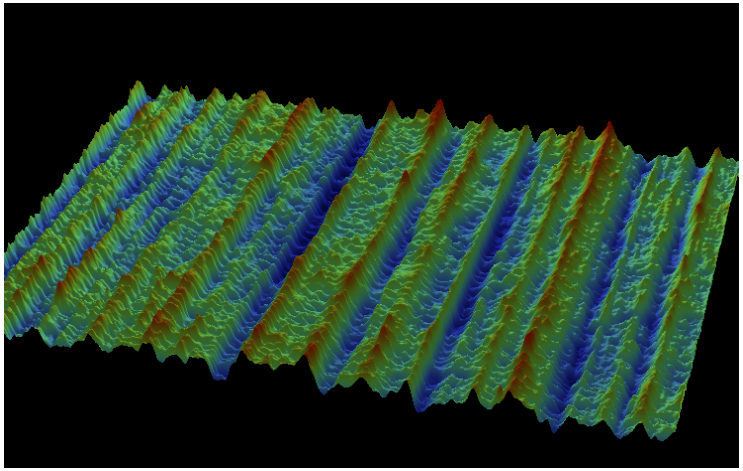
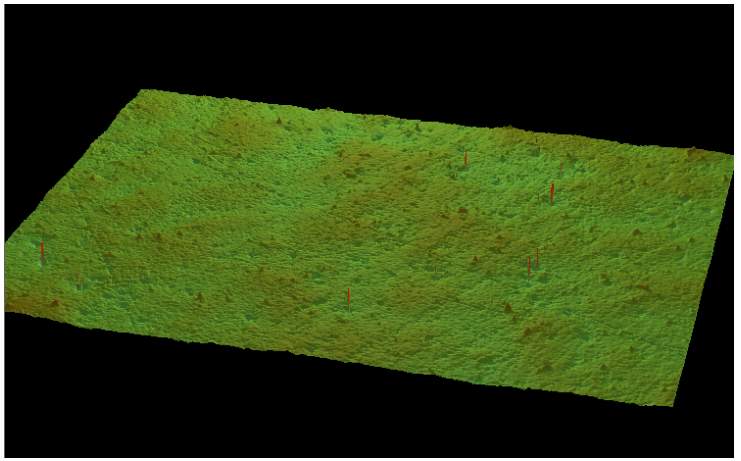
ESF Optics – Aluminum Mirrors

- ESF Added Value
  - Enable use of pure Al mirror (eliminate Ni plating)
    - Low weight
    - Thermal stability
    - Reduced cost
    - Consistent quality
  - CMC polishing reduces roughness from 30-80 Å down to < 10 Å
- Applications
  - X-ray telescopes
  - Cryogenic instruments
  - Interferometry
  - Medical imaging devices
- 3-Dimensional Polishing Capability





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Summary and Conclusions

- **Intensity of Technology Investment Increasing**
- **New Demands For Performance, Selectivity, Tunability**
- **Divergence of Integration, Patterns, Microstructures and Materials**
- **Greater Emphasis on Cost and Quality and Supply Assurance**
- **Adjacencies For Growth**

CMP For Microelectronics:
"A Lot of Hunt Left in This Dog"

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Thrust B: Front End Processes

Project 1: Surface Preparation

Anthony Muscat*, Chemical & Environmental Engineering, Arizona
Yoshio Nishi, Electrical Engineering, Stanford

Project 2: Deposition

Paul McIntyre, Materials Science and Engineering, Stanford
Stacey Bent, Chemical Engineering, Stanford
Charles Musgrave, Chemical Engineering, Stanford
Krishna Saraswat*, Electrical Engineering, Stanford

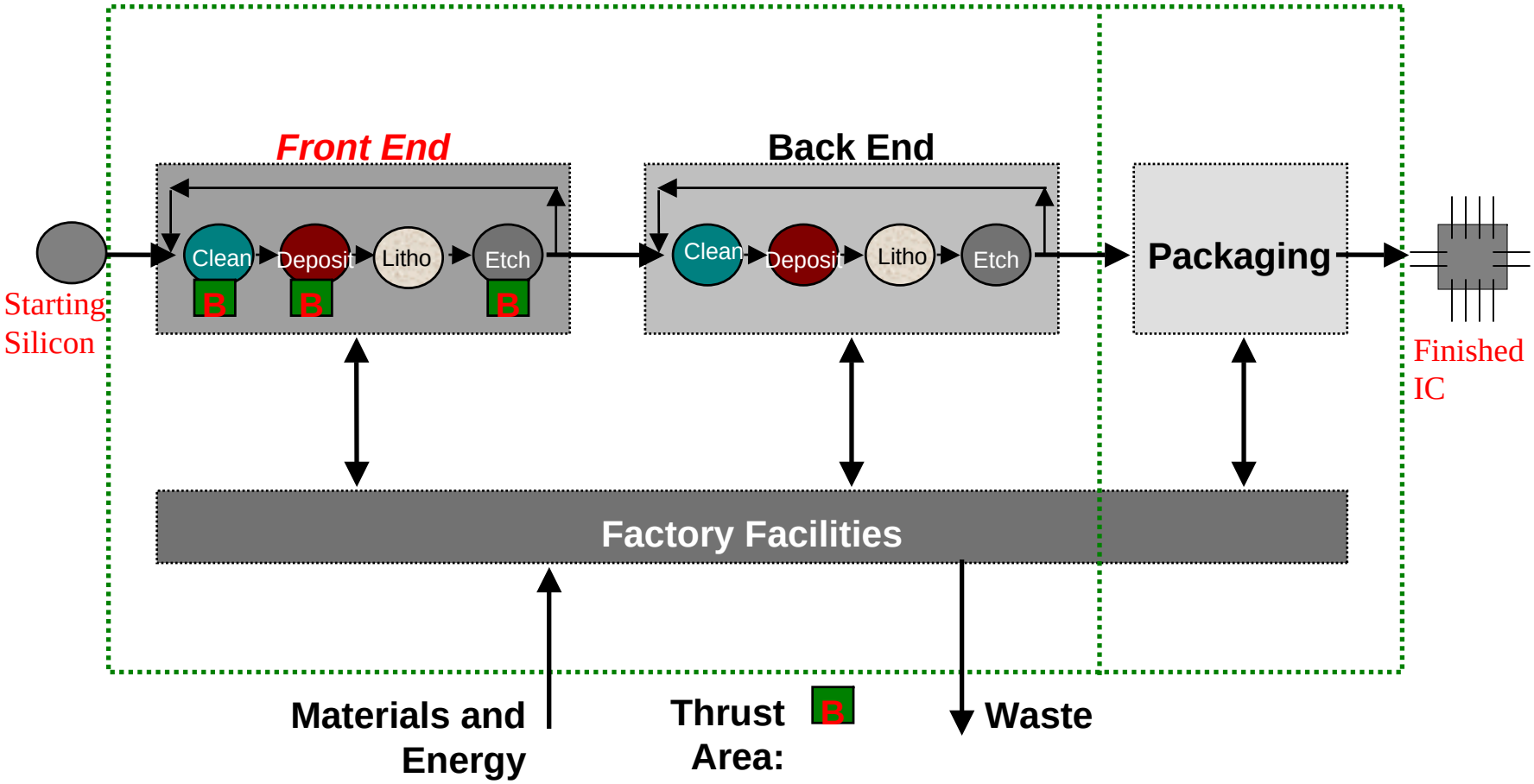
Project 3: Etching and Device Structures

David Graves, Chemical Engineering, U.C. Berkeley

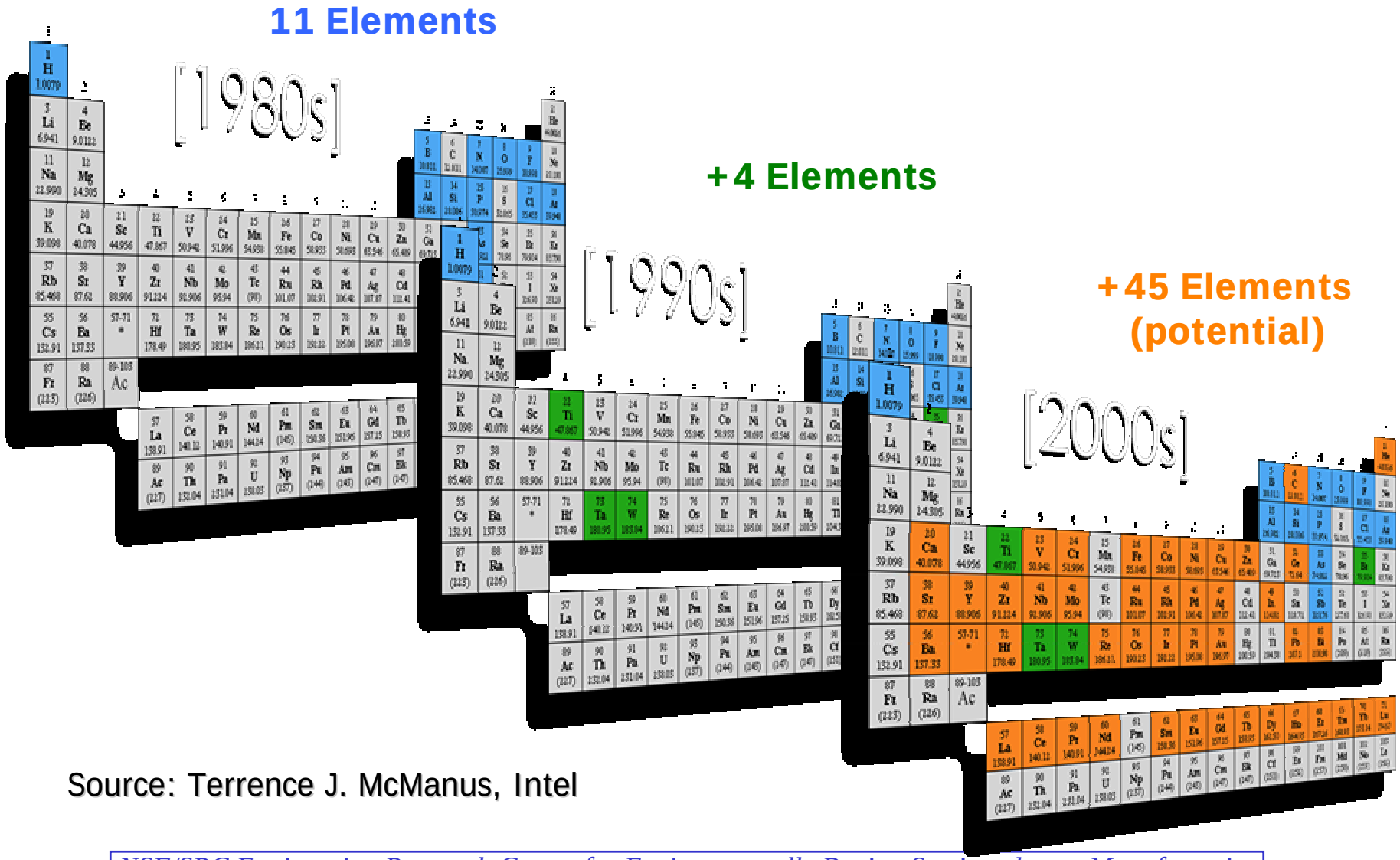
Annual Review, February 23-24, 2006

* Thrust Co-Leaders

Thrust B within ERC Research Framework



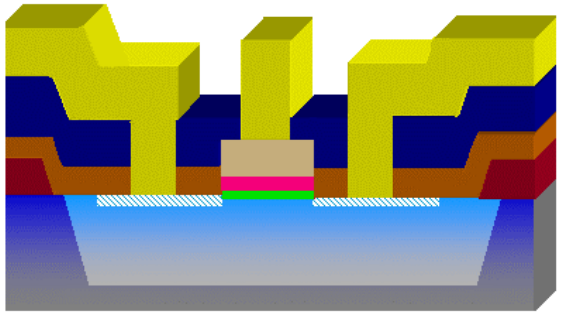
Moore's Law Relies on New Materials



Source: Terrence J. McManus, Intel

Thrust B Objectives

- **Device Modeling**
  - Saraswat (Stanford)
    - Identify promising gate stack structures and materials
- **Etching of High κ and Metal Gate Films**
  - Graves (Berkeley)
  - Saraswat (Stanford)
    - Precursor selection
    - Effluent generation
    - Profile simulations



- **Selective Surface Priming**
  - Bent (Stanford)
    - Deactivate SiO_2 by organic
  - Muscat (Arizona)
    - Activate Si by monolayer halogen
- **ALD of High κ Films**
  - McIntyre (Stanford)
    - Precursor selection
    - Effluent generation
    - Reaction chemistry modeling
- **Surface preparation of new materials**
  - Nishi (Stanford)
    - Ge cleaning process development
    - Surface characterization
  - Muscat (Arizona)
    - SiGe
- **Gas Phase Surface Preparation**
  - Muscat (Arizona)
    - Integrated HF/vapor + UV-Cl_2

Selected Accomplishments 1997-2005

- 5x reduction of UPW for some rinsing applications was demonstrated, including 50% reduction in cycle time (1997)
- Showed methoxy termination created oxide with superior interface properties (aq 2000, gas 2005)
- Developed Cost of Ownership model for implementing new surface passivation in fab (2001)
- Demonstrated promising electrical behavior of UV-ozone grown ZrO_2 films using patterned Pt MOSCAP structures (2001)
- Determined that anisotropic structure and plasma etching best trade-off between process issues, environmental issues, and device performance for three transistor structures (2002)
- Measured etch products in RuO_2 etching in O_2 plasma and applied wall deposition model (2003)

Selected Accomplishments 1997-2005, cont'd

- Developed first ICP abatement device for destroying PFCs downstream of a plasma etcher with destruction efficiencies >94%, results commercialized by Litmus (2004)
- Demonstrated chemical mechanisms and energetics of ALD blocking and selectivity as a function of organic SAM functionalization using quantum chemical simulations (2004)
- Utilized DI-O3 process on Ge to improve surface roughness to 0.12nm RMS (2005)
- Demonstrated selective deposition of single SiN layer on Si using UV-light (2005)
- Achieved a new chemically selective process to achieve high-resolution area selective atomic layer deposition of hafnium dioxide (2005)

Graduated Students

Tracey Burr (SPAWAR Systems)

Casey Finstad (Texas Instruments)

Hyoungsub Kim (SKK University, Korea)

Marci Liao (PDF Solutions)

Huihong Luo (Oracle)

Renee Mo (IBM)

Collin Mui (Novellus)

Charles Perkins (Intel)

Chris Wade (Agilent)

Thrust B Session

Introduction (5 min) Anthony Muscat, UA

Task B-1-1 (9 min) Adam Thorsness, UA
Surface Chemistry of High-k Barrier Layer Formation

Task B-1-2 (9 min) Jungyup Kim, Stanford
Surface Roughness and Passivation Studies of Ge surfaces

Task B-2 (8 min) Rong Chen, Stanford
Selective Surface Preparation and Templated Atomic Layer Film Deposition

Task B-2 (8 min) Raghav Sreenivasan, Stanford
Gate Stack Engineering by Atomic Layer Deposition

Task B-2 (8 min) Kang-Ill Seo, Stanford
Improvement of NBTI of High-k by Incorporation of Fluorine

Task B-3-1 (9 min) Jerry Hsu, UC Berkeley
Evaluating EHS Impacts of New Dielectric and Conductor Materials Etch Processes

Q&A (4 min)

Thrust B1:

Surface Chemistry of High-k Barrier Layer Formation

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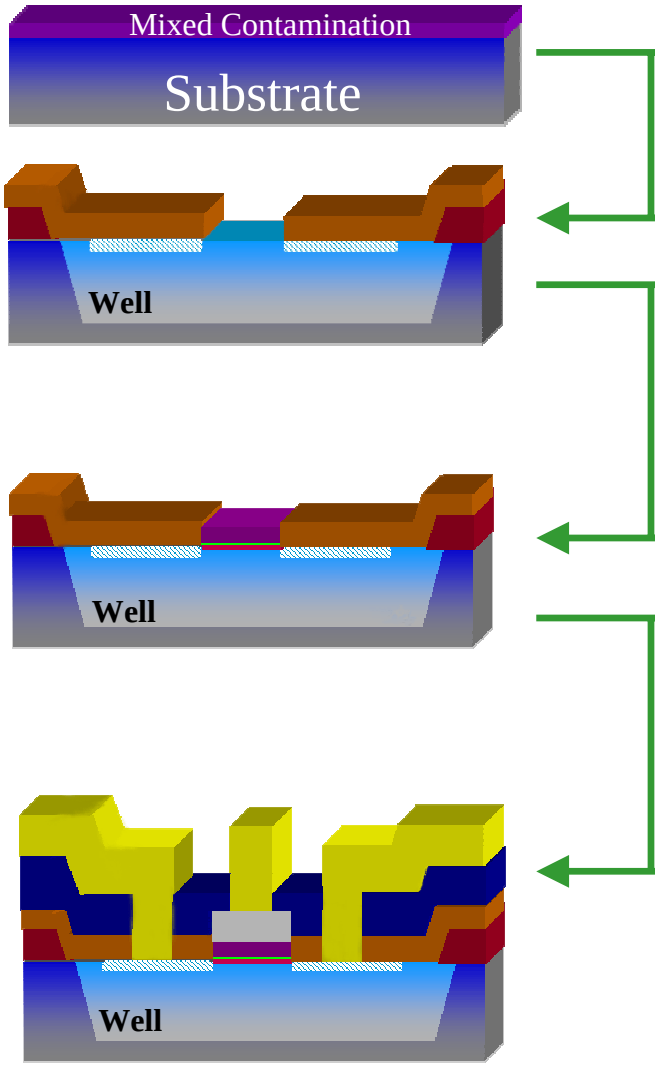
NSF/SRC ERC EBSM Annual Review

Feb. 2006

Outline

- Motivation and ESH Impact
- Research Cluster Apparatus and Process Flow
- UV-Cl_2 process to create a Cl-terminated Si(100) surface from SiH and SiH_2 terminated surfaces.
- Water reactivity with activated Cl-terminated Si(100) surface
- Detailed surface analysis of the silicon oxides resulting from $H_2O(g)$ + SiCl(a) reaction.

Gate-Last MOSFET Process with Additive Patterning



Clean, grow field oxide, pattern device area (Mask 1), ion implant (M2), deposit spacer oxide, pattern gate area (M3)

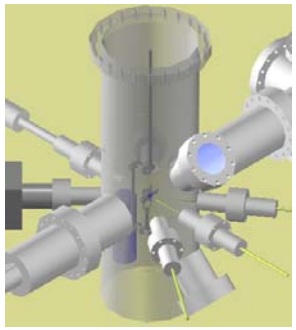
Selectively deposit barrier layer, high-k seed layer, and high-k dielectric layer

Deposit gate metal, pattern (M4), deposit metal isolation dielectric, pattern (M5), deposit metal 1 layer, pattern (M6)

ESH Impact

- Gas phase processing requires less chemical usage than liquid processes by several orders of magnitude.
- Integrate process into a single vacuum cluster tool.
- Low temperature method of forming a single silicon oxide layer means lower energy usage.

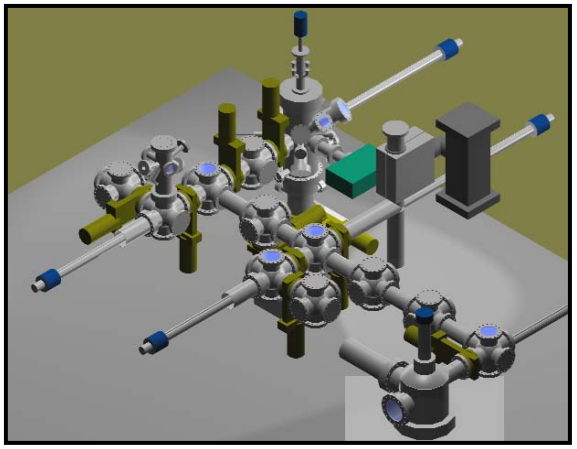
Research Cluster Apparatus



TPD Analysis/
ALD Chamber

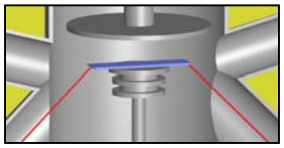
Photochemistry
Reactor

ALD
Reactor



Load
Lock

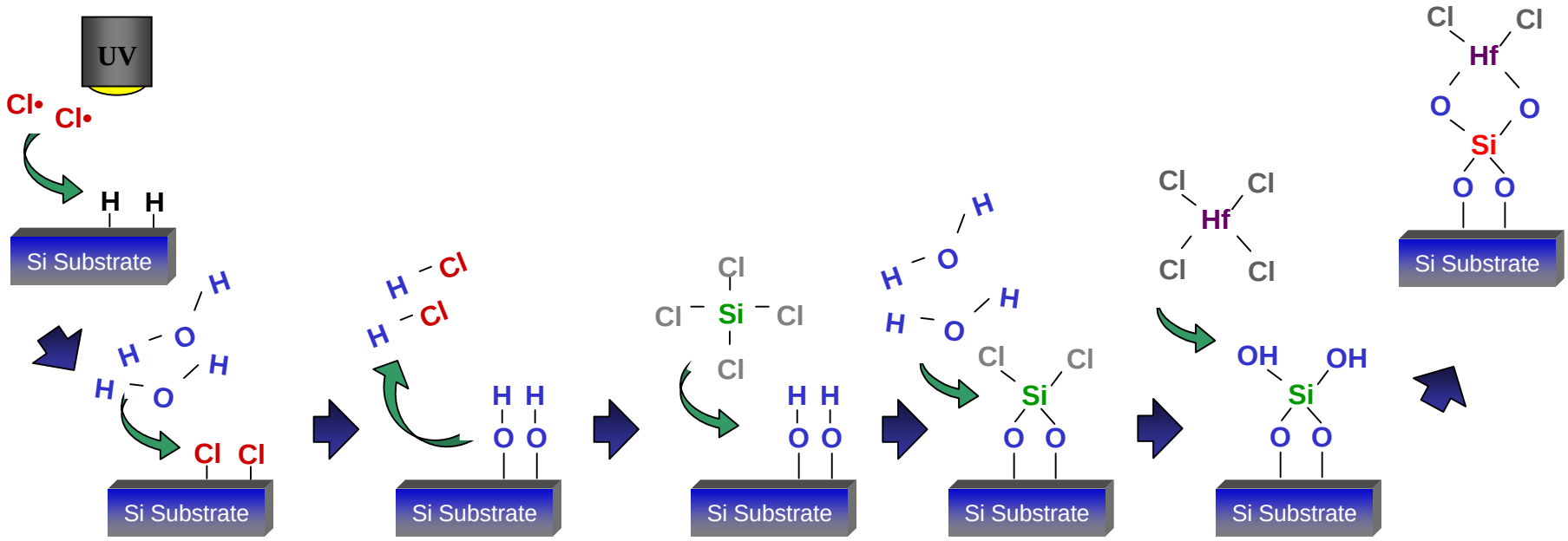
HF Reactor



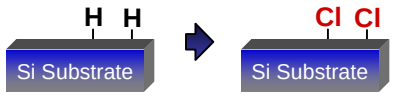
Surface Analysis
Chamber
(XPS, Auger)

Example of Controlled Starting Surface for ALD

- Focus of this presentation
  - UV/Cl_2 to create a Cl-terminated Si surface
  - H_2O exposure to create SiOH groups or a silicon oxide surface
- Advantages
  - Low temperature process
  - Self-limiting/Controllable formation a uniform oxide and OH-termination



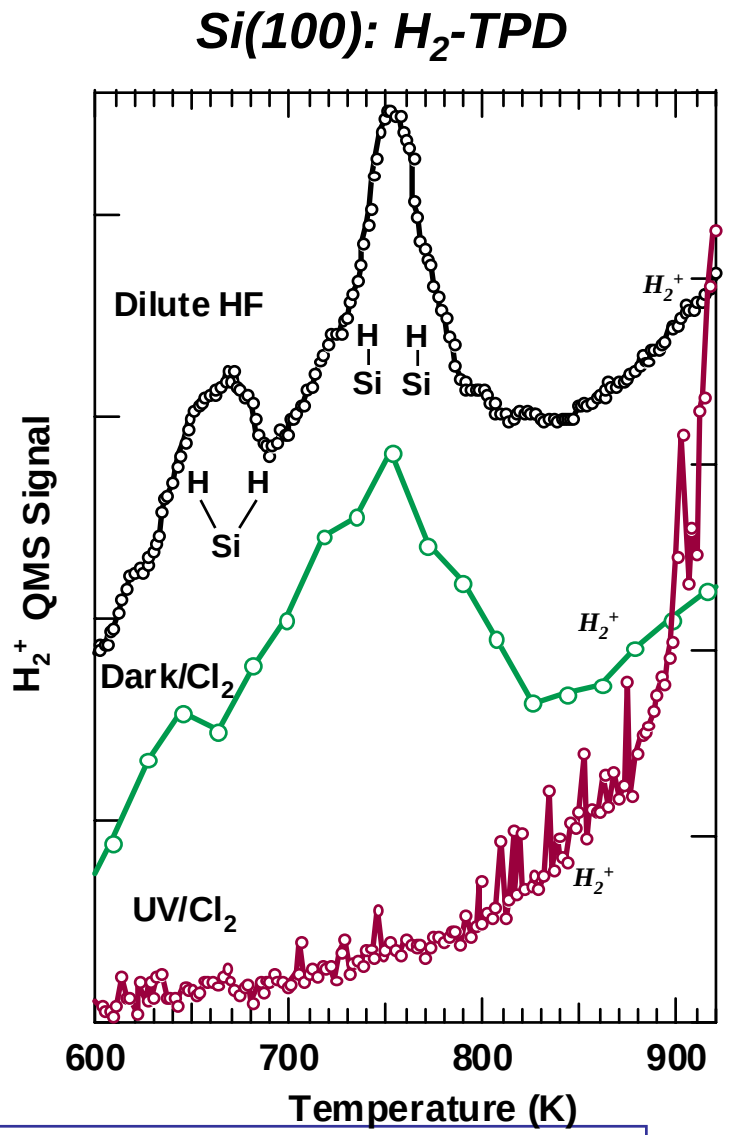
A UV/Cl_2 Process Replaced All Surface H With Cl Atoms



- H_2 desorbs from SiH and SiH_2 surface species after a **dilute HF clean** from an Si(100) surface

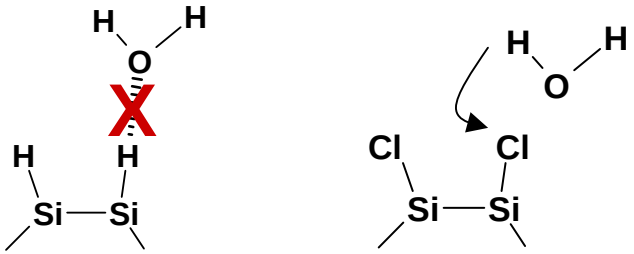
- H_2 desorbed from Si(100) surface exposed to **Dark/Cl_2 process**
  - *T = 300 K, 10% Cl_2 at 100 Torr, 5 min*

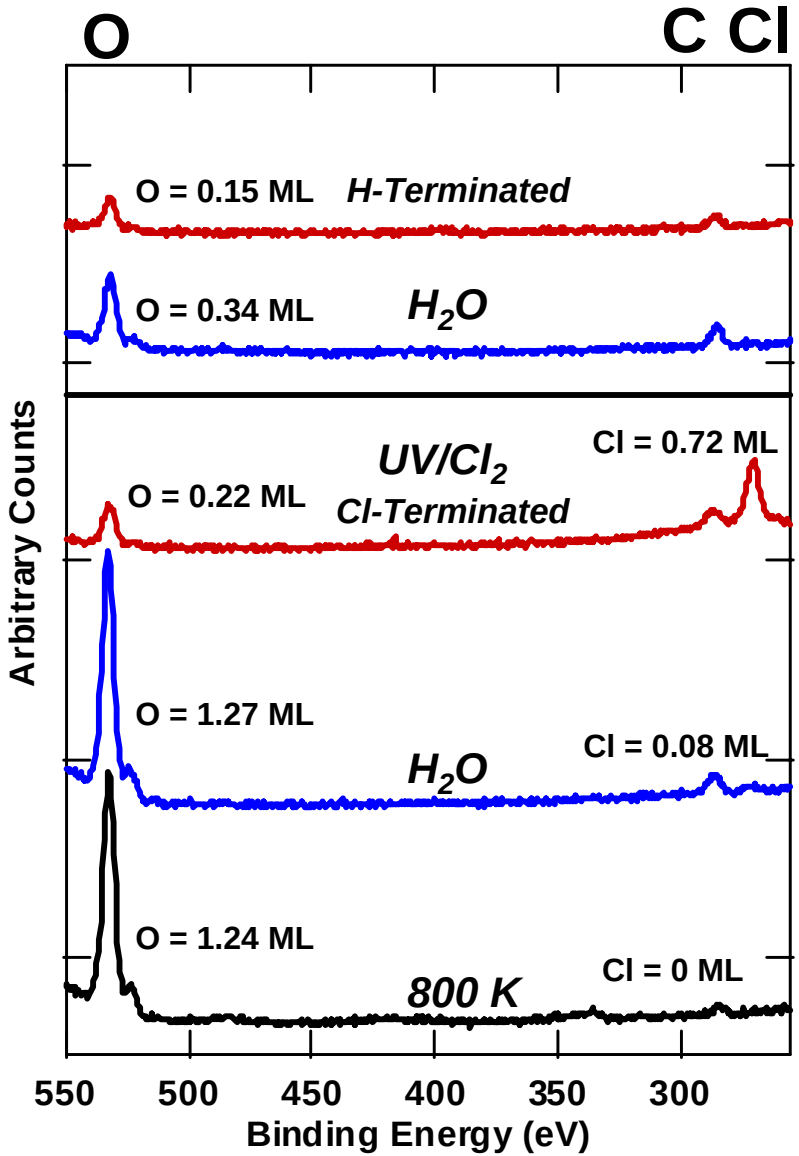
- No H_2 desorbed after **UV/Cl_2 process** indicating that all H atoms were replaced by Cl atoms.
  - *T = 300 K, 10% Cl_2 at 10 Torr,* 40 sec



Selectivity: More O on a Cl/Si(100) Activated Surface

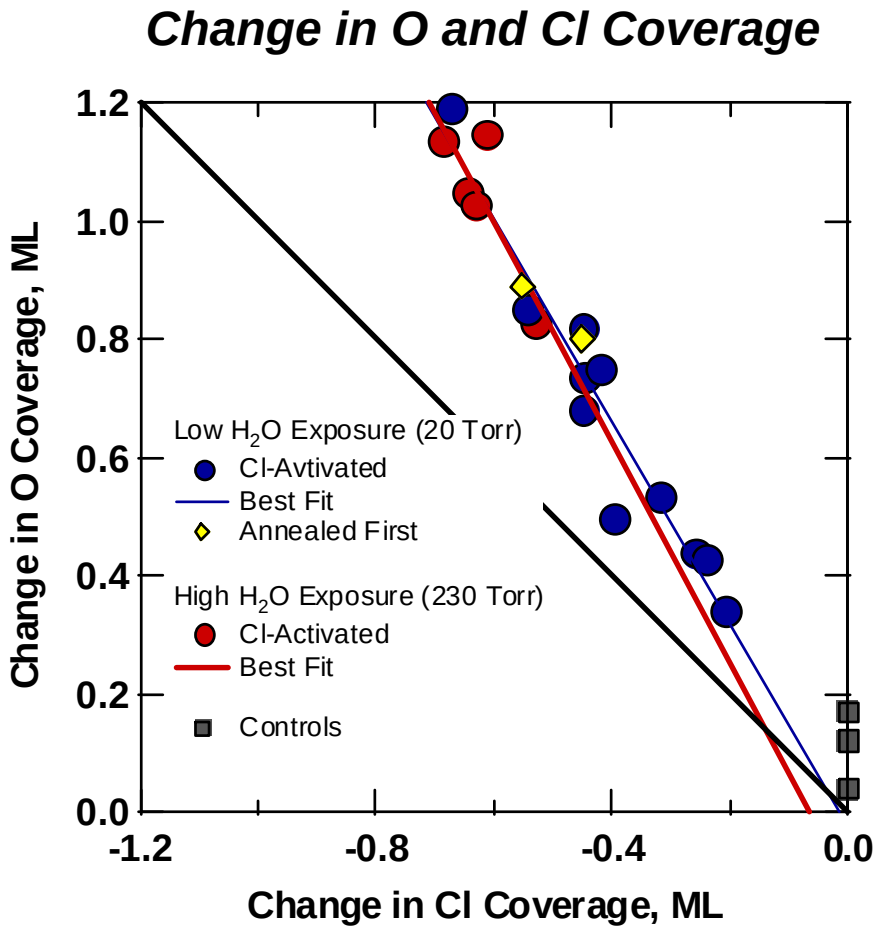
- H_2O exposure of non-activated surface results in only 0.2 ML O added.
- Cl activates surface for reaction with H_2O gas.
  - 0.83 ML – 1.2 ML added
- No increase in O after Cl is removed.



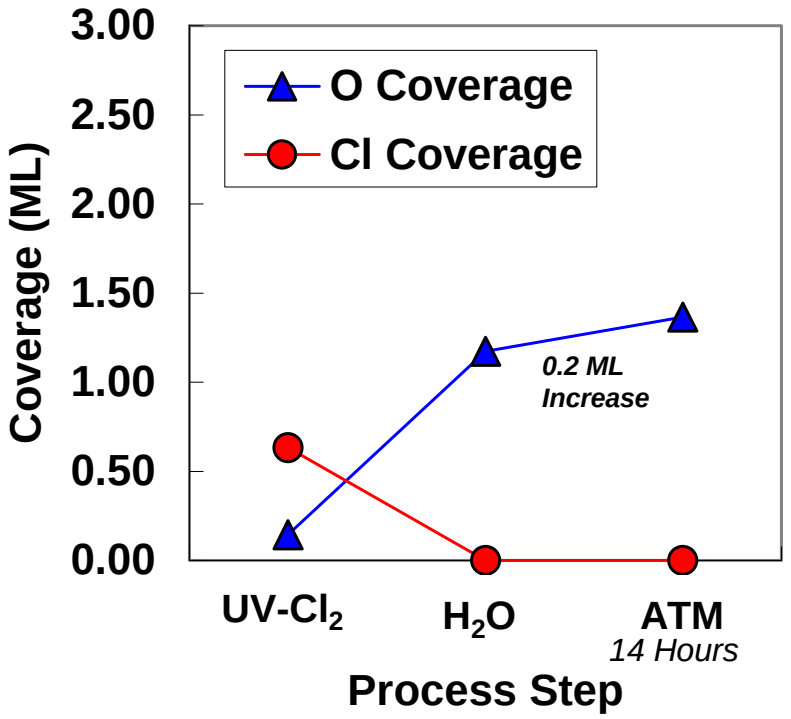


Addition of O and Removal of Cl

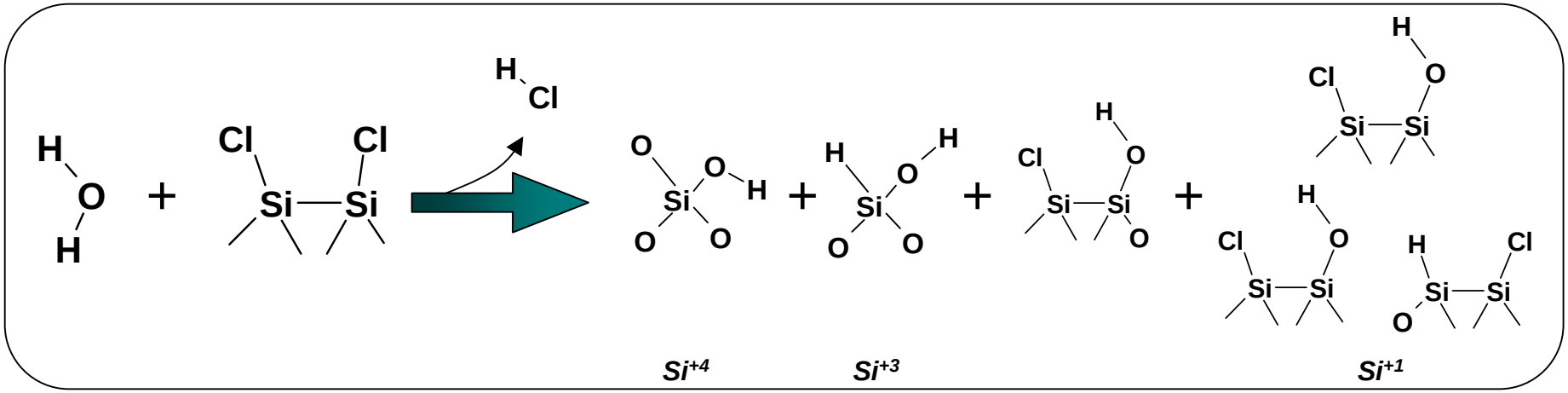
- 1.5 O added to 1 Cl removed

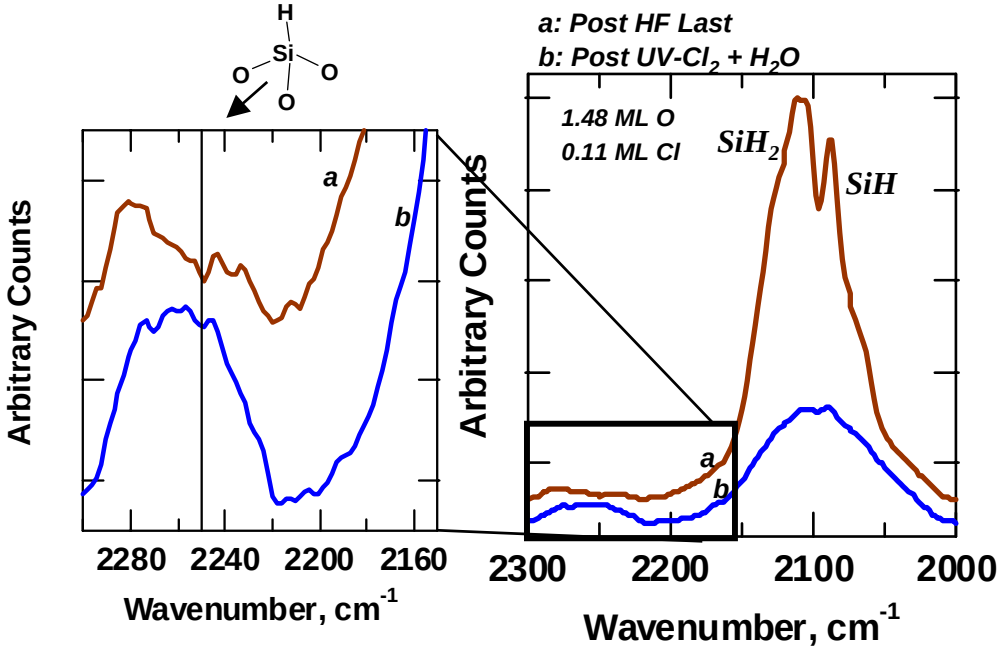


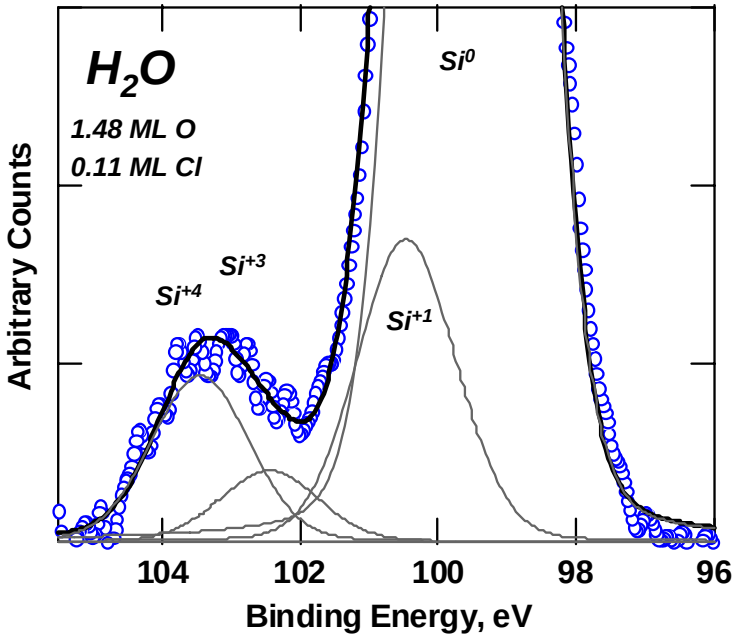
- Stable in atmosphere
  - Only a 0.2 ML increase in O after 14 hours.



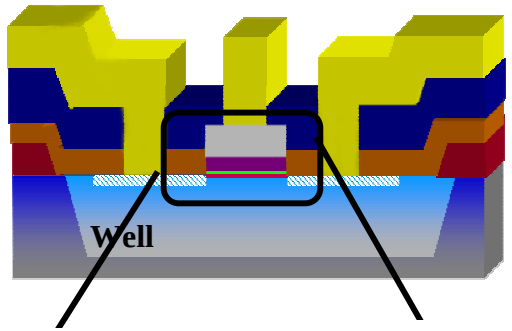
Oxygen in Si Backbonds and Different Suboxides Created



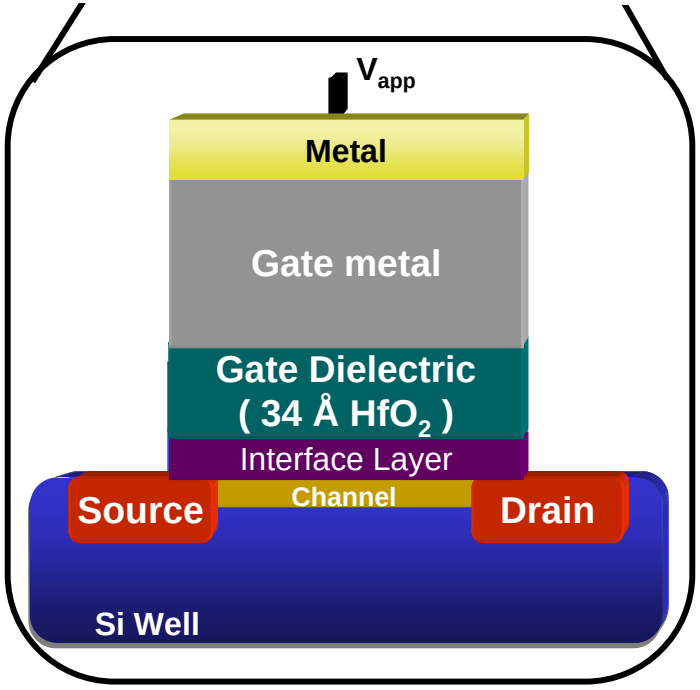


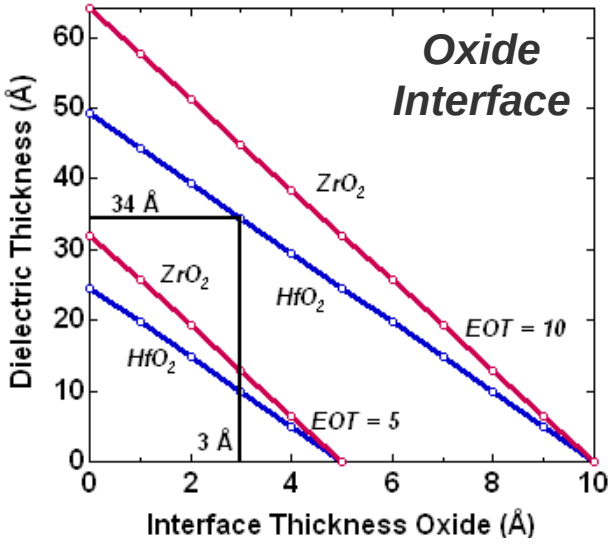


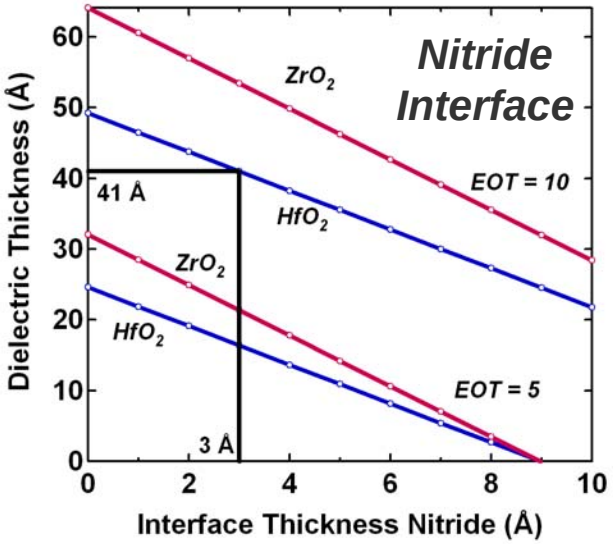
Interface Oxide Allows For Up to 34 Å of High-k



$$C_x = \frac{\kappa_x \varepsilon_0 A}{t_x} \qquad \frac{1}{C_{stack}} = \frac{1}{C_{HfO_2}} + \frac{1}{C_{SiO_2}}$$

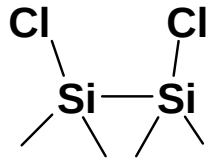


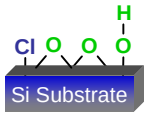




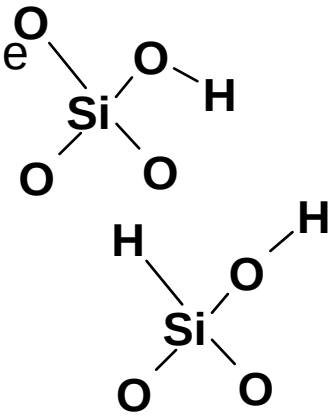
Summary/Conclusions

- Activated surface with halogen for low T interface growth
  - Obtained Cl-terminated Si surface from a UV-Cl_2 process
  - Cl interacted with all Si-H and SiH_2 on the Si(100) surface.
  - Only monochloride formed on the Si(100) surface during UV-Cl_2 process.
  - No H remaining on surface.



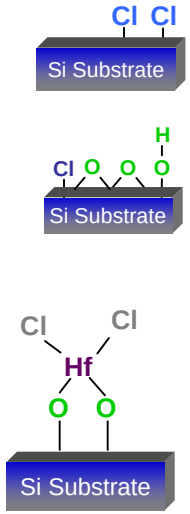


- Deposited single layer of silicon oxide
  - O atoms detected on the surface after water exposure stable up to 800 K. (no decrease in O coverage)
  - Ratio of 1.5 O atoms were added for every 1 Cl removed.
  - O in the Si backbonds
  - SiO_x where x = 1 – 4 exist after water exposure.



Future Plans

- Investigate parameters for manipulating Si^{+1} and SiO_2 (Si^{+4}) formation.
  - More ideal Cl-terminated surface combined with low H_2O partial pressures.
- Deposit high-*k* on thin oxide and perform electrical (CV) measurements on MIS capacitors.
- Activate high mobility substrates



Acknowledgments

- NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing Funding

Subtask B-1-2

Surface Roughness and Passivation Studies of Germanium Surface

Jungyup Kim
Jim McVittie
Toshiyuki Homma
Krishna Saraswat
Yoshio Nishi

STANFORD UNIVERSITY

Background

- Ge is gaining interest as a substrate for high mobility applications because of higher carrier mobility. (2X electron & 4X hole mobility of Si)

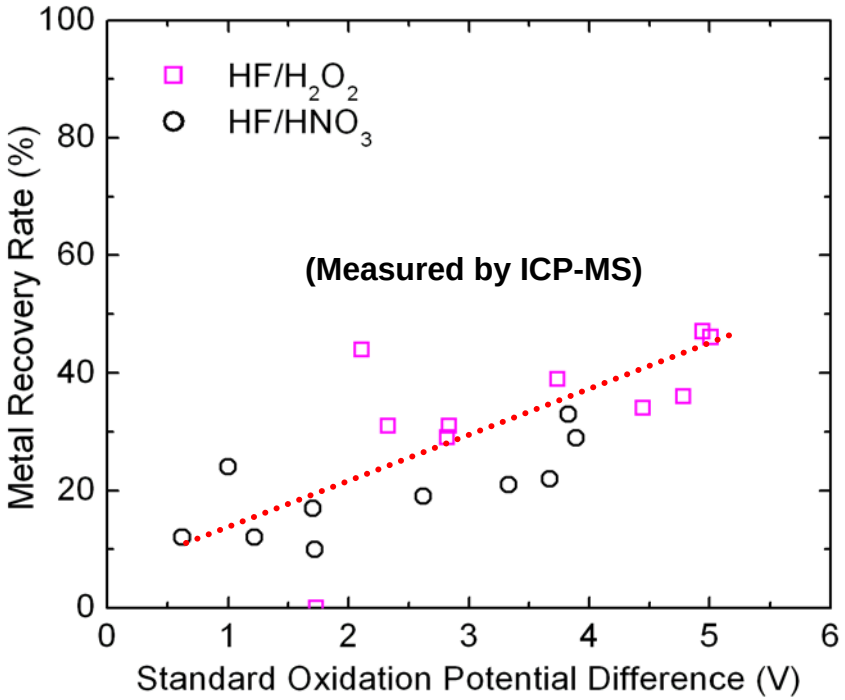
($cm^2V^{-1}s^{-1}$)	Si	Ge
Electron	1450	3900
Hole	505	1800

Schäffler et al, *Semiconductor Sci. Tech.* (1997)

- Therefore development of Ge surface preparation technique is required with particular characteristics ;

1. Efficient Removal of Metal Contamination
2. Minimal Consumption of the Substrate
3. Minimal Surface Roughness
4. Good Passivation Characteristics

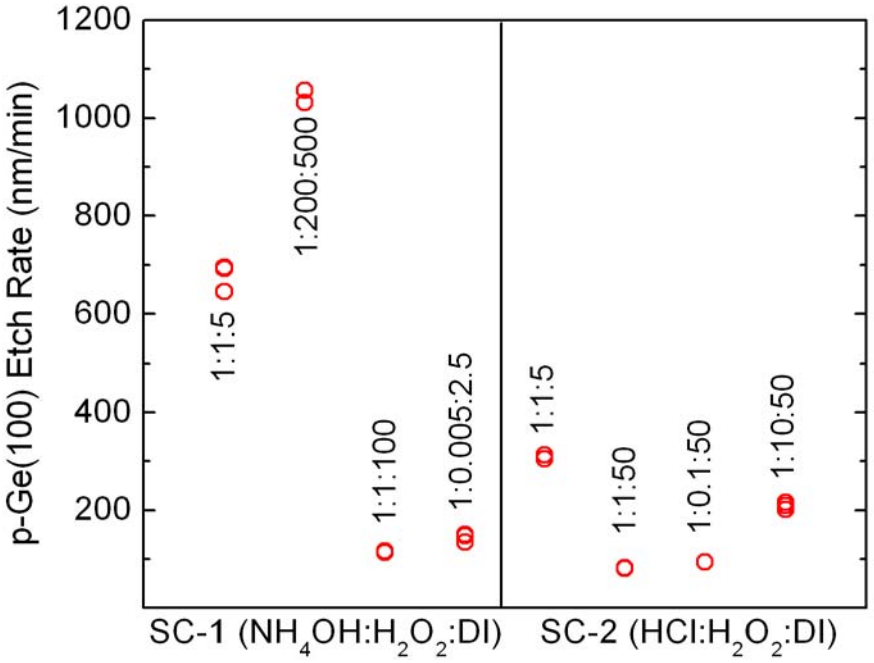
1. Efficient Removal of Metal Contamination

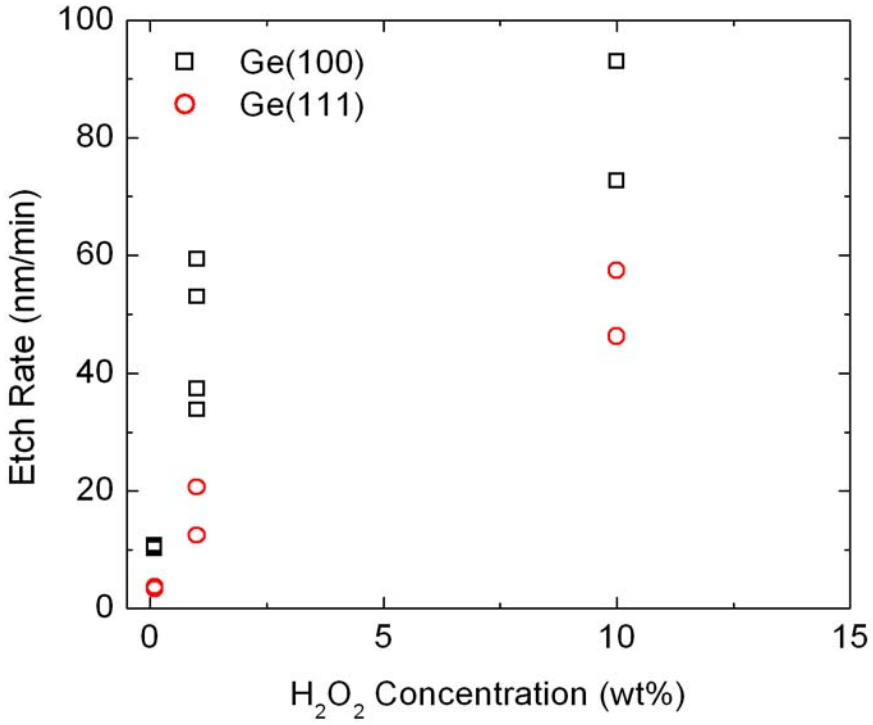


- Higher standard oxidation potential difference gives higher metal recovery rate → H_2O_2 and O_3 have the highest oxidation potential and need to be evaluated for cleaning properties.

	Redox Reaction	Standard Oxidation Potential
K	$K = K^+ + e^-$	2.931
Ca	$Ca = Ca^{2+} + 2e^-$	2.868
Na	$Na = Na^+ + e^-$	2.710
Mg	$Mg = Mg^{2+} + 2e^-$	2.372
Al	$Al = Al^{3+} + 3e^-$	1.662
Si	$Si + 2H_2O = SiO_2 + 4H^+ + 4e^-$	0.857
Zn	$Zn = Zn^{2+} + 2e^-$	0.762
Cr	$Cr = Cr^{3+} + 3e^-$	0.744
Ni	$Ni = Ni^{2+} + 2e^-$	0.257
Fe	$Fe = Fe^{3+} + 3e^-$	0.037
Ge	$Ge + 2H_2O = GeO_2 + 4H^+ + 4e^-$	0.019
NO_3^-	$NO + 2H_2O = NO_3^- + 4H^+ + 3e^-$	-0.96
Cu	$Cu = Cu^{2+} + 2e^-$	-0.342
Au	$Au = Au^{3+} + 3e^-$	-1.498
H_2O_2	$2H_2O = H_2O_2 + 2H^+ + 2e^-$	-1.776
O_3	$O_2 + 2H_2O = O_3 + 2H^+ + 2e^-$	-2.076

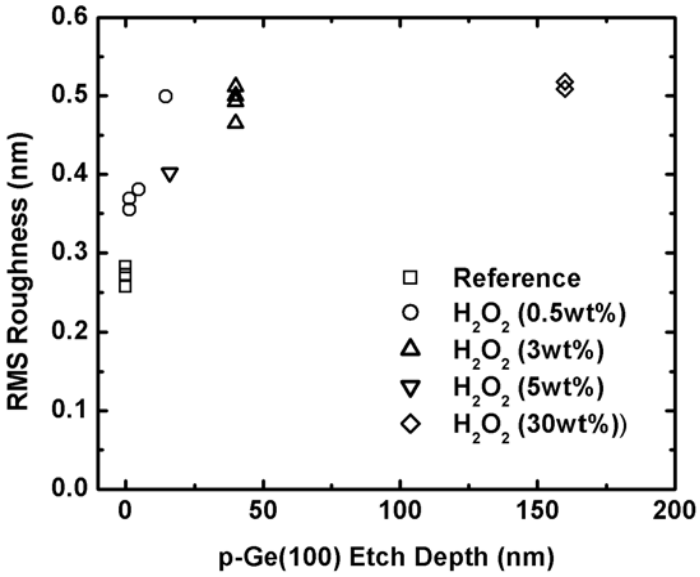
2. Minimal Consumption of Ge Substrate – Etch Rate Study

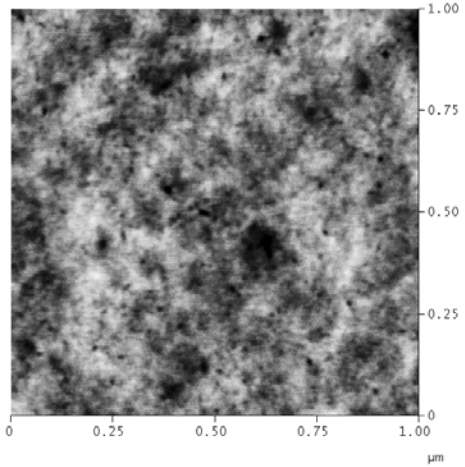




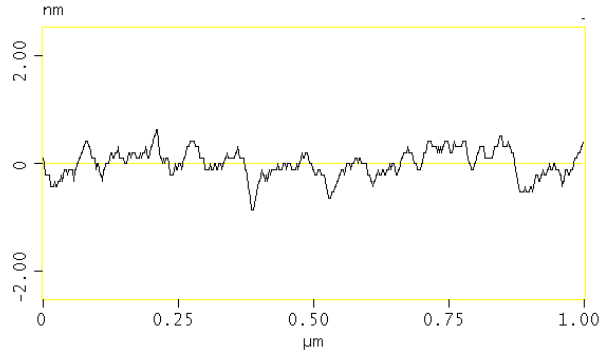
- H_2O_2 based aqueous solutions have high etch rates on Ge. O_3 has ~1/10 etch rate of H_2O_2.

3. Surface Roughness



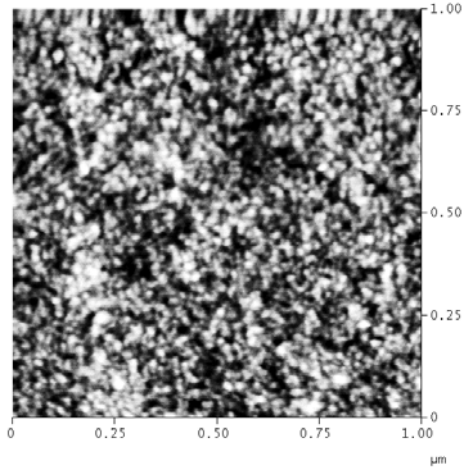


As received Ge

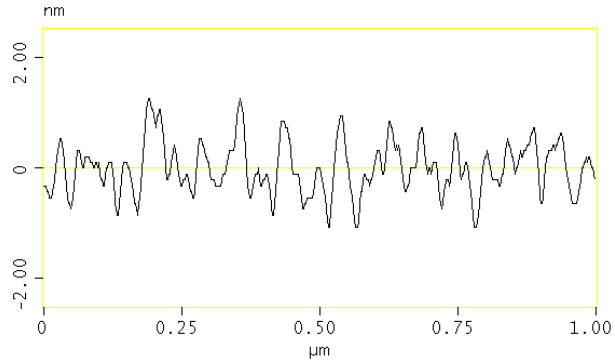


Cross-section

- Surface roughness increases with etch amount and saturates at a steady state value of 0.5nm.

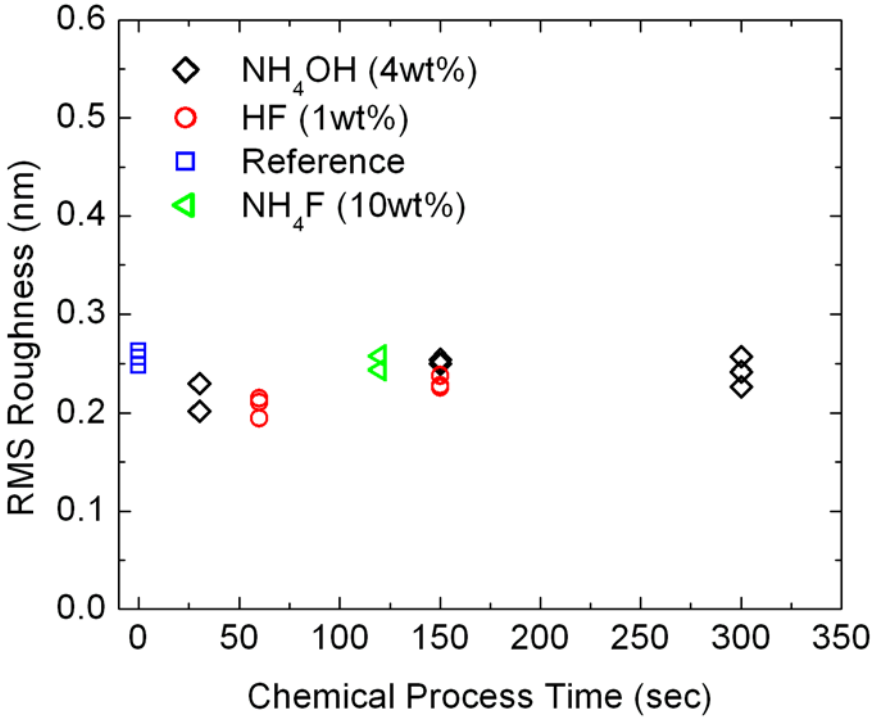


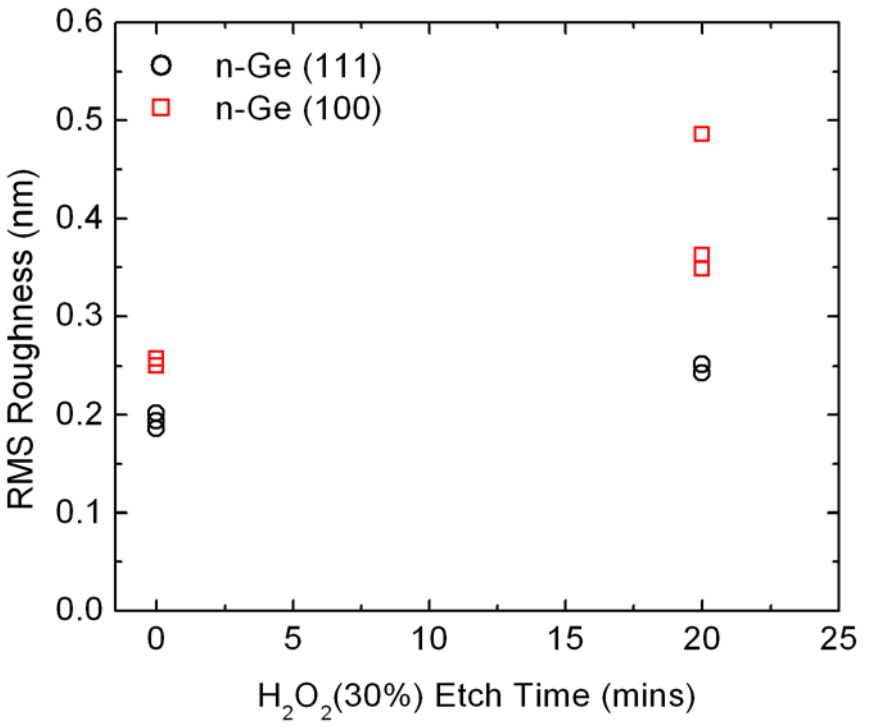
H_2O_2(3wt%) 10min



Cross-section

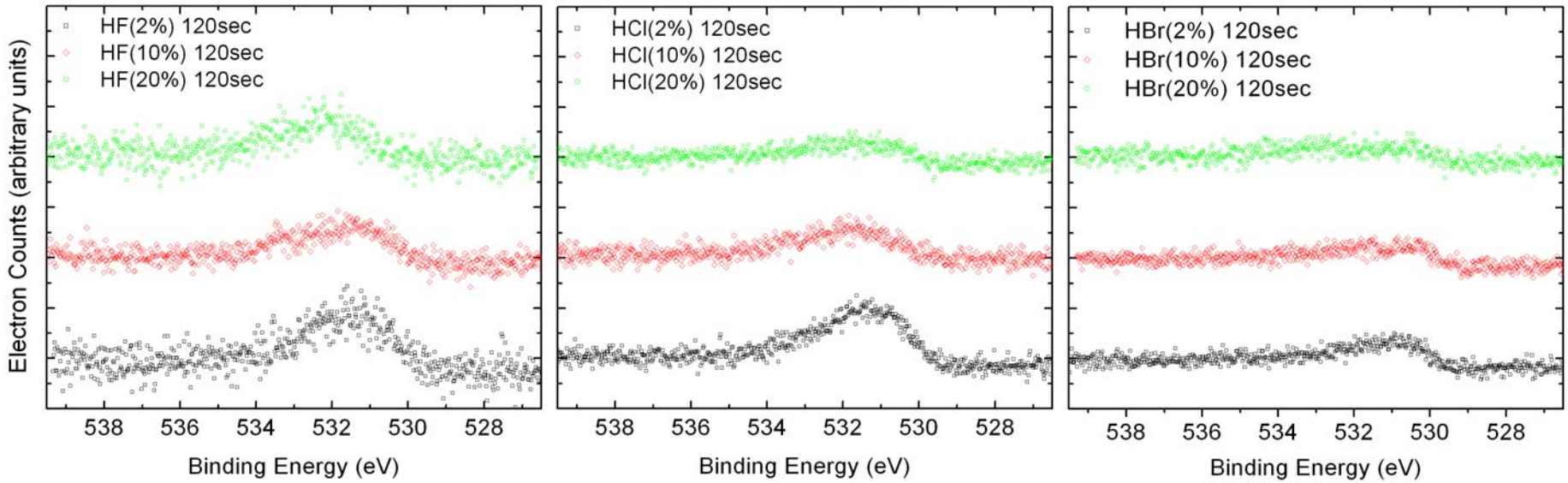
3. Surface Roughness – Correlation with Etch Amount

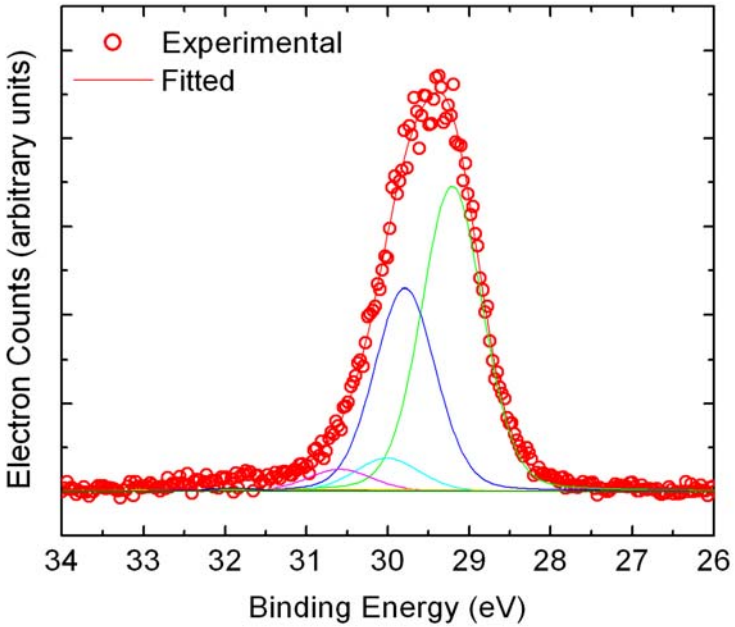




- Surface roughness does not increase in non-etching solutions (NH_4F, HF, NH_4OH and DI water). Surface roughness can be minimized by minimizing the etch amount.
- Surface roughness is direction dependent. Ge(111) has lower surface roughness than Ge(100)

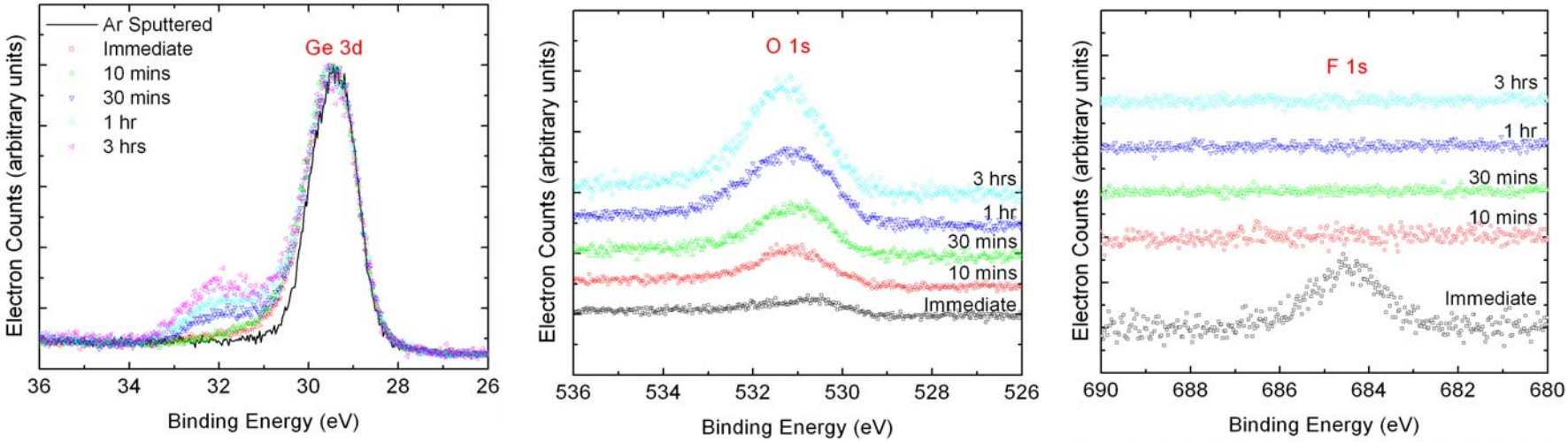
4. Surface Passivation - Ge Native Oxide Removal





- Higher concentration solutions removes more oxide from the surface.
- HF cannot completely remove oxygen species on Ge.

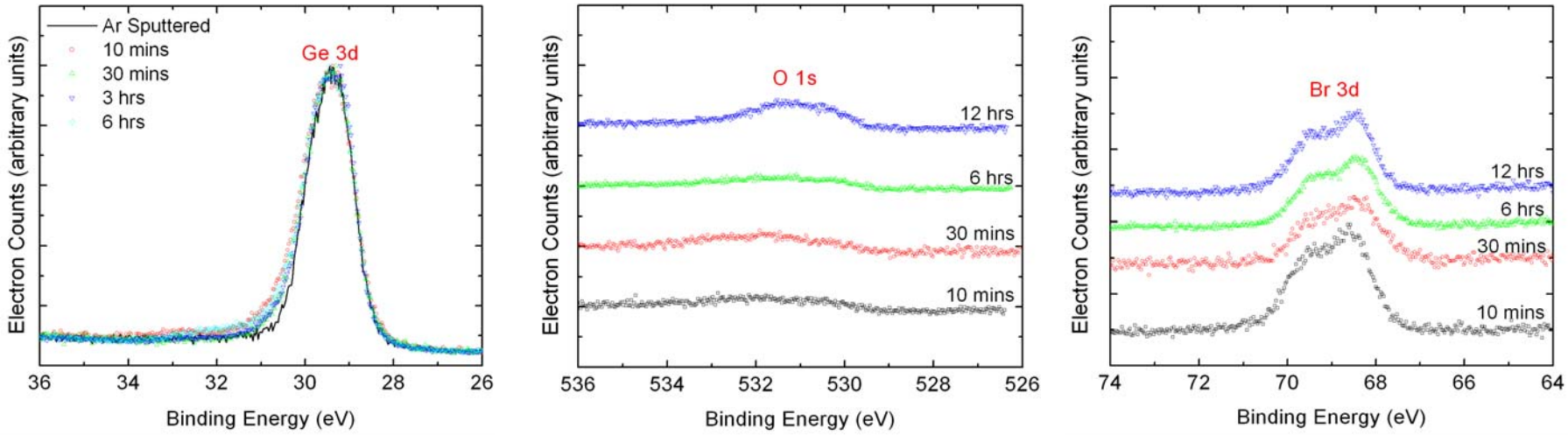
Ambient Stability of HF & HCl Passivated Ge(100) Surface



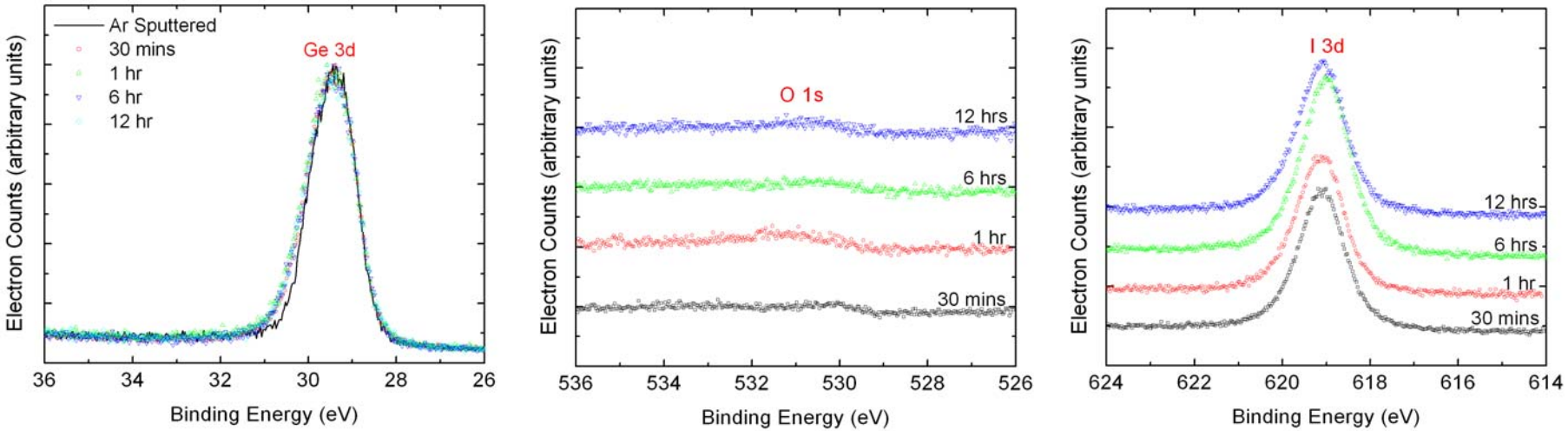
- HF treated surface re-oxidizes in 10 mins. (desorption of fluorine)

- HCl treated surface re-oxidizes in 10 mins. (desorption of chlorine)

Ambient Stability of HBr & HI Passivated Ge(100) Surface

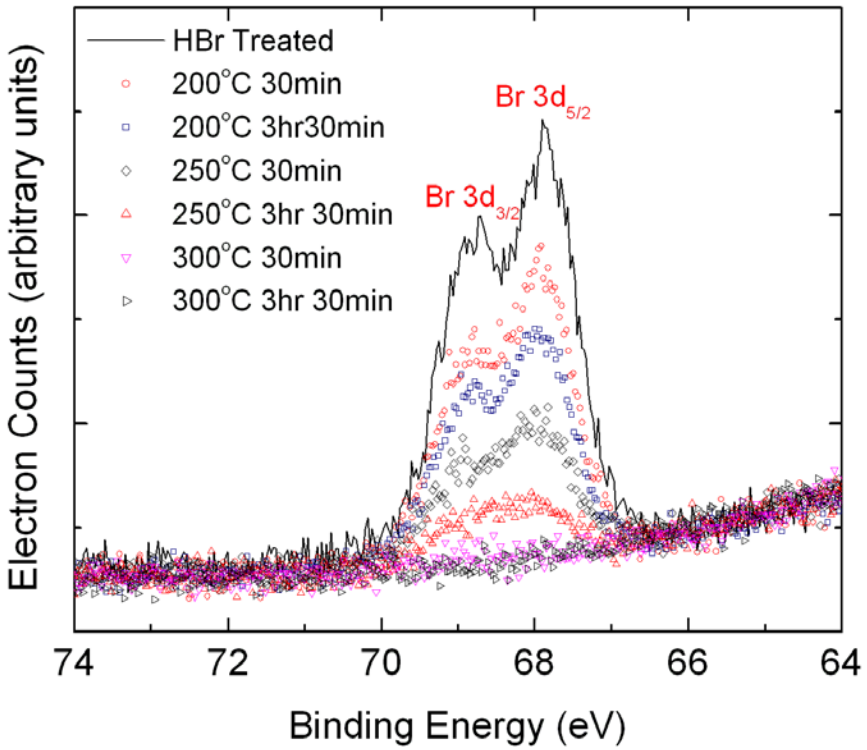


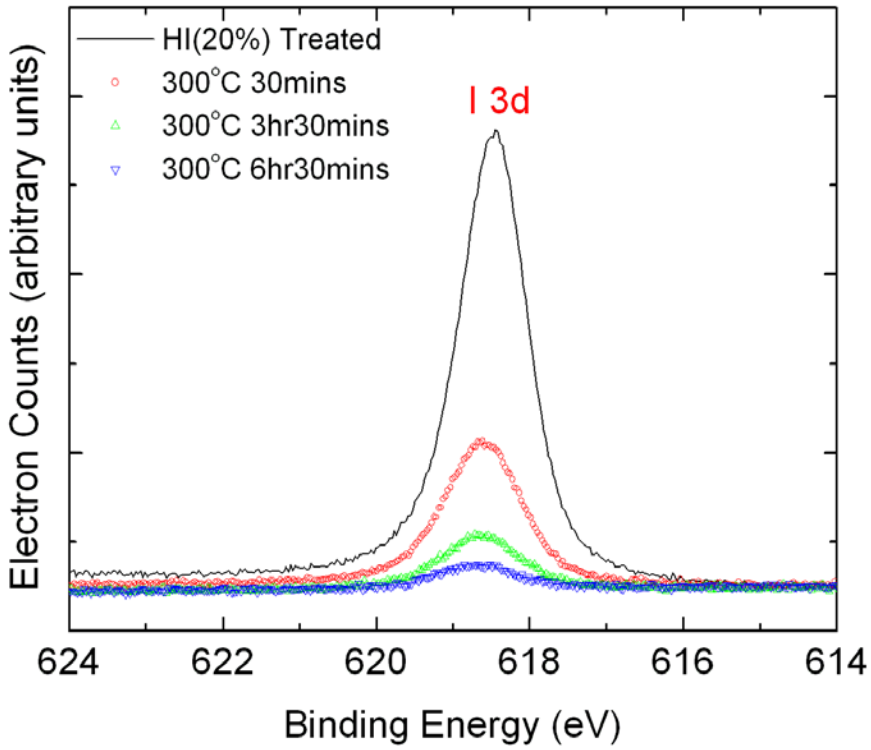
- HBr treated surface stays passivated for 6 hours.



- HI treated surface stays passivated for 12 hours.

Thermal Stability of HBr & HI Passivated Ge Surface





- HBr passivated surface is stable up to 250ºC.
  HI passivated surface is stable up to 300ºC

Conclusions

1. Redox potential table is a useful tool in choosing a material for metal removal.
2. High etch rates in oxidizing aqueous cleaning solutions (700 nm/min in 1:1:5 SC-1 @room temp) makes it difficult to apply Si cleaning solutions.
3. Ge has concentration dependent high etch rates in H_2O_2 solutions.
4. Surface roughness increases with etching amount and does not change in non-etching solutions. Surface roughness is less for (111) crystallographic direction.
5. Aqueous HBr & HI solutions passivates the Ge surface for >6 hours.
6. HBr and HI passivated surface is stable at 250ºC and 300ºC respectively.

Future Work

1. Characterization of Br and I passivation on Ge. (CV, ESR)

Thrust B: Front End Processing

Task B2: Selective Surface Preparation and Templated Atomic Layer Film Deposition

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Department of Materials Science and Engineering

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Department of Electrical Engineering

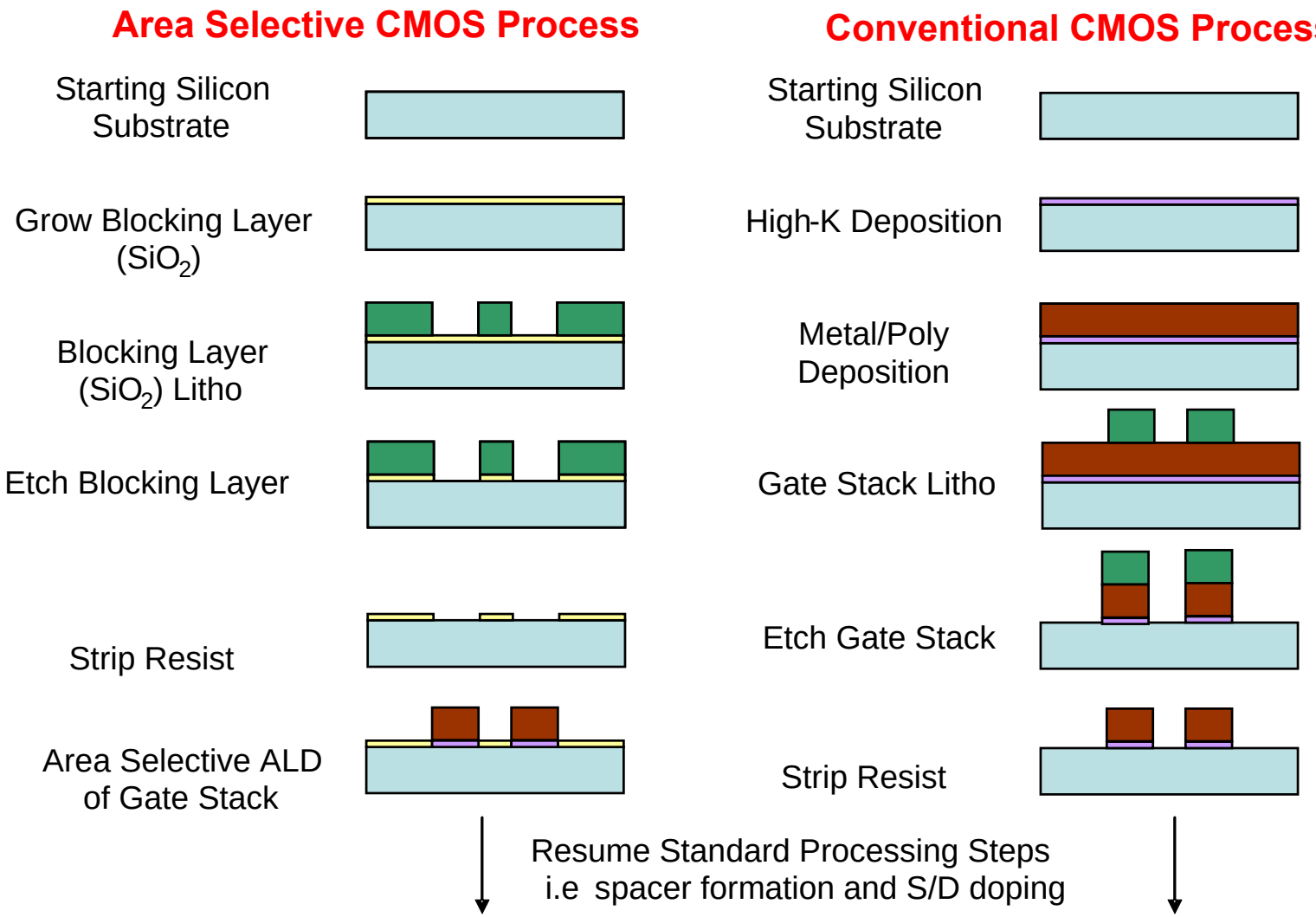
Stanford University

NSF/SRC EBSM ERC Review 2006-02-23

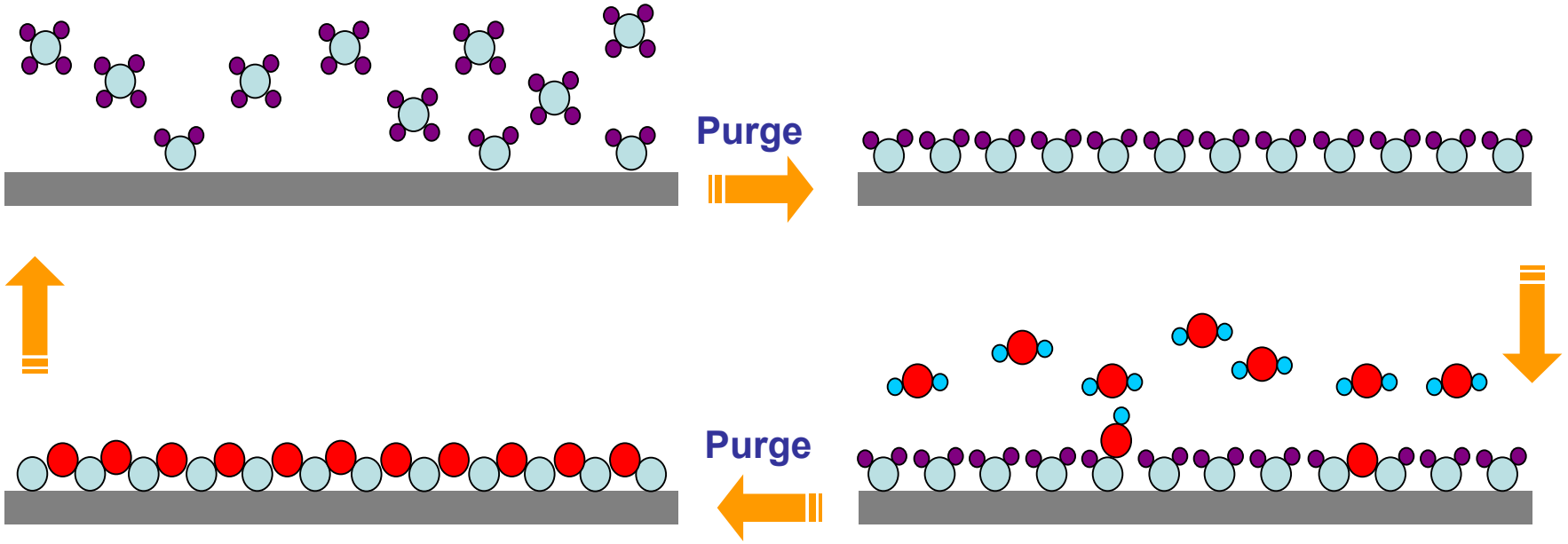
Area Selective ALD of Gate Stack

Goal:

- **Self-aligned deposition process for gate dielectrics and gate metal**
- **Avoid tuning etching for different high-κ gate dielectrics and gate metals**



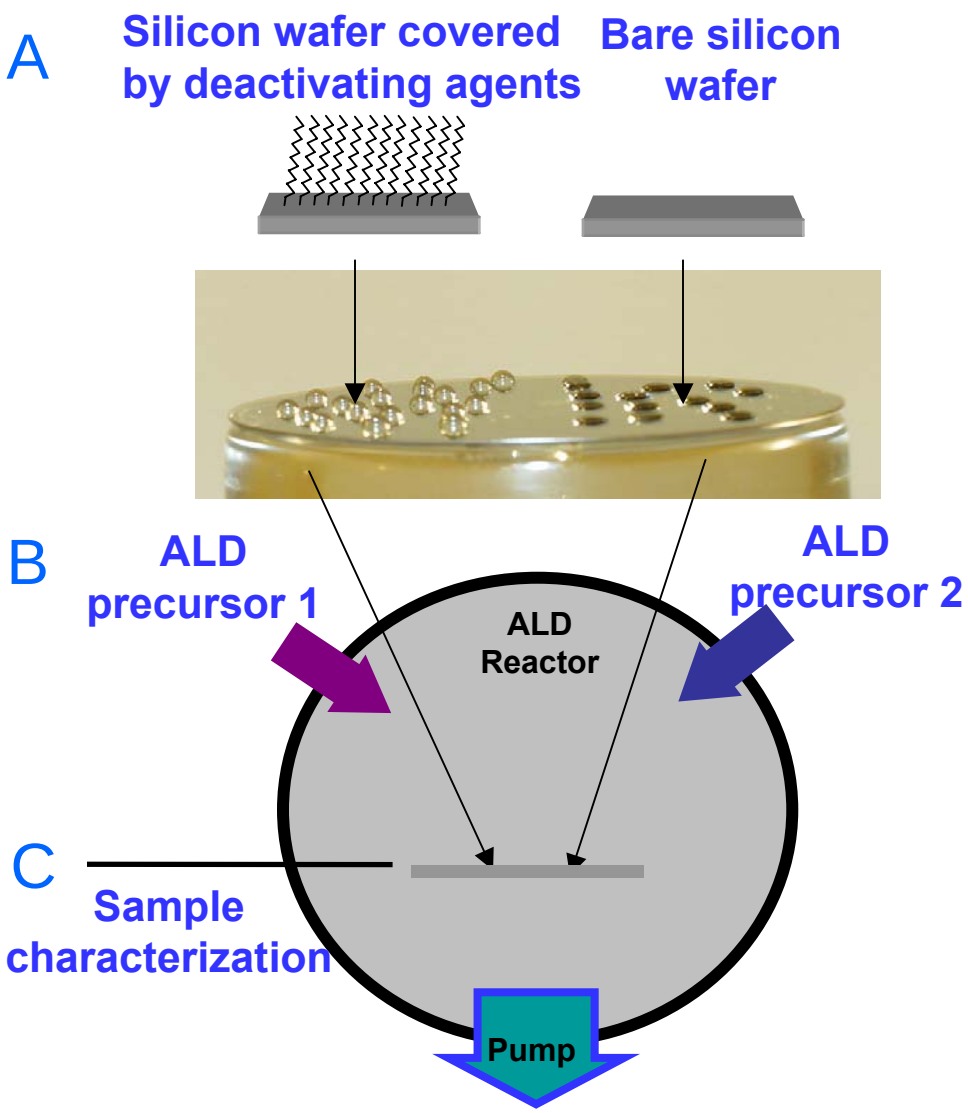
Atomic Layer Deposition



- Layer saturation reactions form conformal film and excellent step-coverage.
- ALD process is based upon chemical reactions between the precursors and the film surface.
- Surface saturation controls deposition.
- Reactions depend on the specific reactive functional groups present at the surface.

⇒ Manipulate surface groups before deposition to control the ALD process.

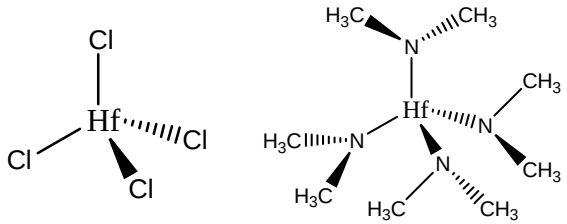
Experimental Setup



HfO_2 ALD Precursors:

- Hafnium chloride ($HfCl_4$) or hafnium alkylamido $Hf(NMe_2)_4$)
- Water

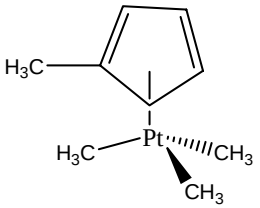
process temperature: 300°C for $HfCl_4$ and 250°C $Hf(NMe_2)_4$



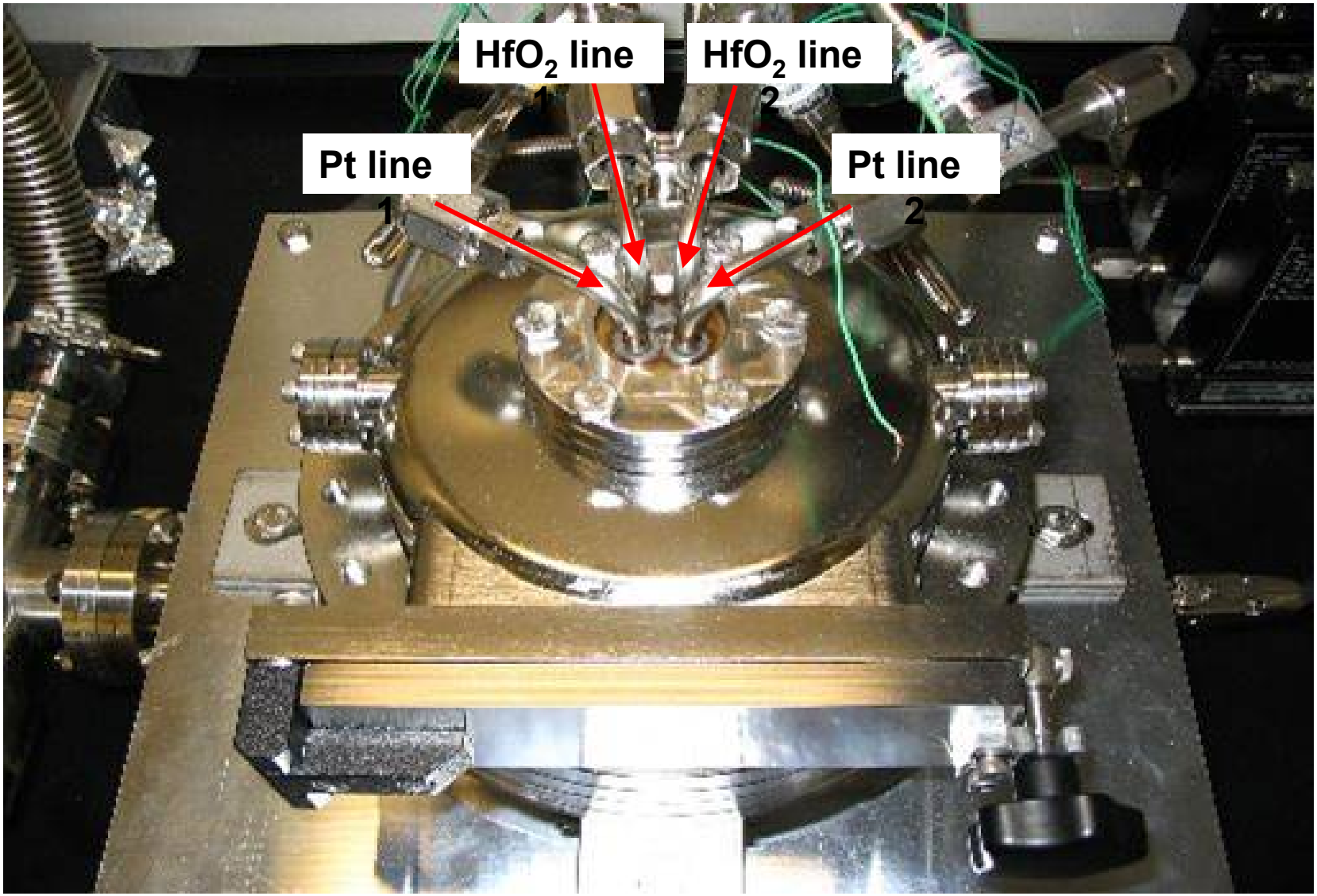
Pt ALD Precursors:

- (Methylcyclopentadienyl)trimethyl platinum ($MeCpPtMe_3$)
- Oxygen

process temperature: 325°C

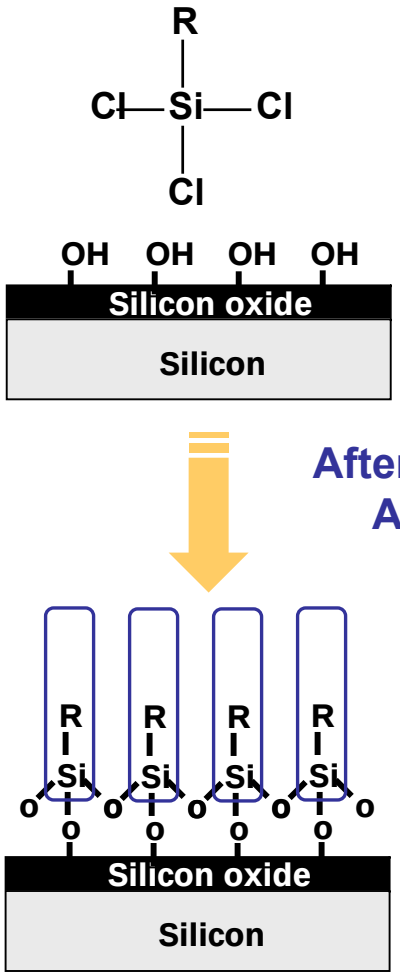


Top View of ALD Reactor

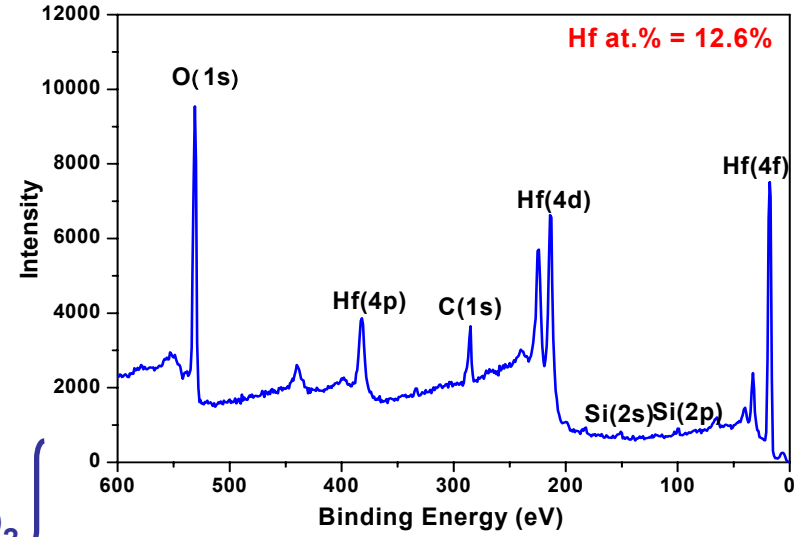


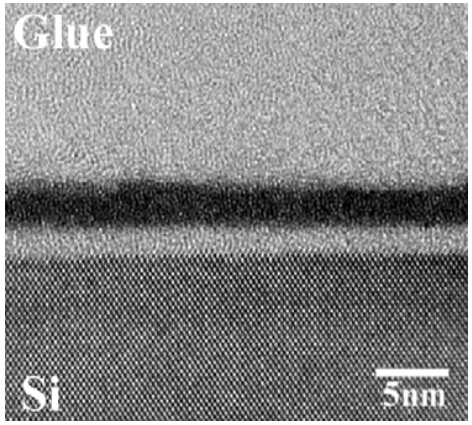
Deactivating Agents on Oxide Surface

silylating reactions

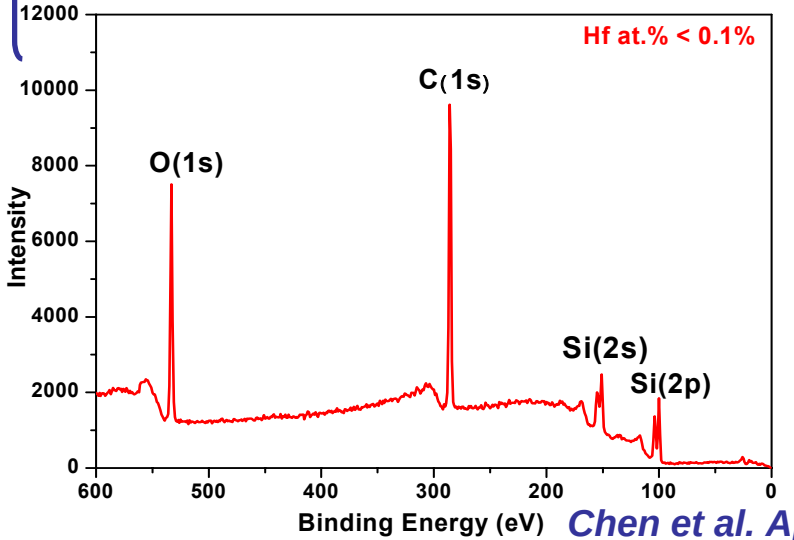


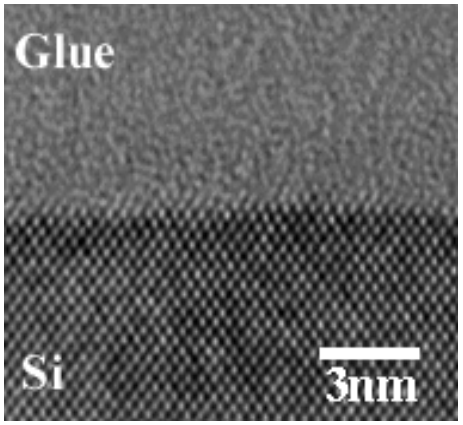
native silicon oxide surface





n-octadecyltrichlorosilane (ODTS) deactivated surface



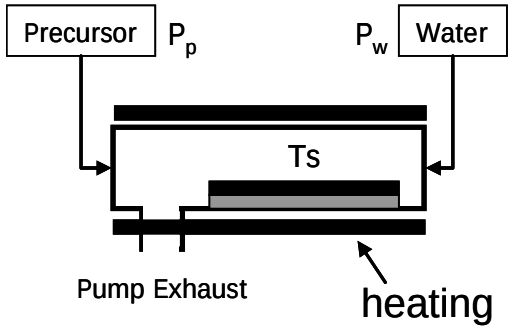


Chen et al. Appl. Phys. Lett. 2004, 84, 4017

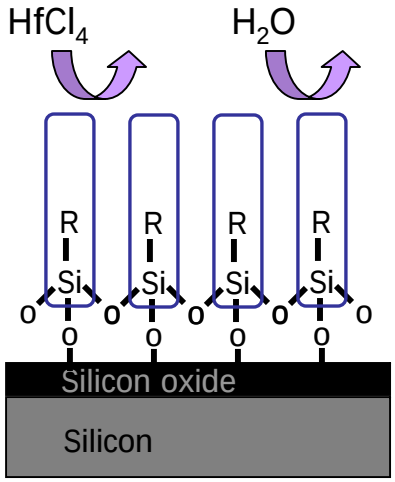
- **It is also effective for other high-k dielectrics (eg. ZrO_2) and metals (eg. Pt) ALD**

SAMs Formatiom through Vapor Phase Delivery

Preparation of SAMs by CVD



In ALD reactor



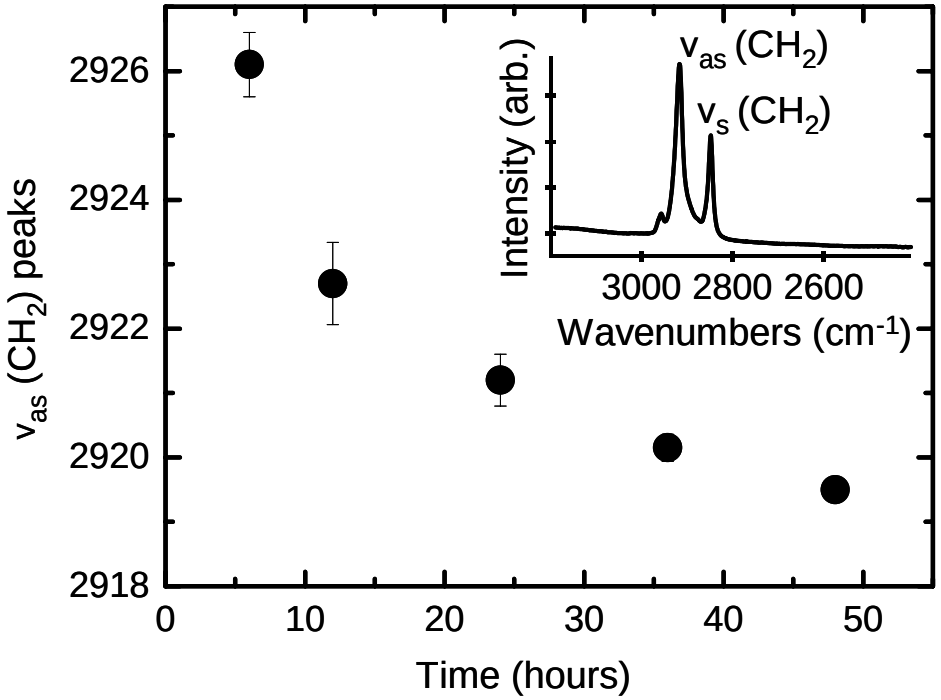
Experimental Condition:

Precursors (ODTS and water)

Ts=170^{o}C

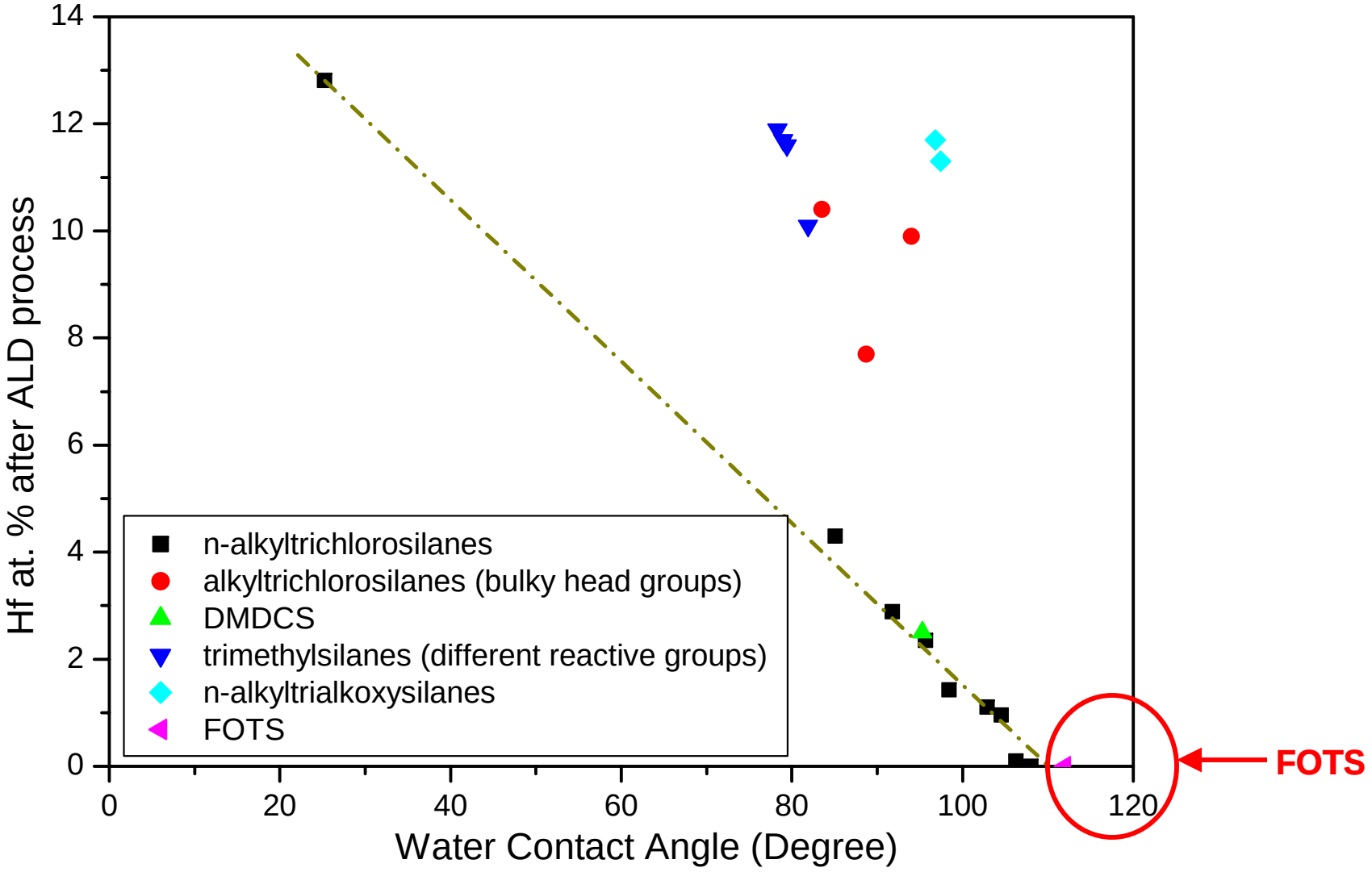
Goals:

- Avoid solvent usage – Environmental friendly
- Compatible to ALD process – Easy scale up to wafers used in IC industry (CVD, vacuum systems)



Long reaction time are necessary for SAMs crystallization and complete deactivation

Correlation between Deactivation & Hydrophobicity

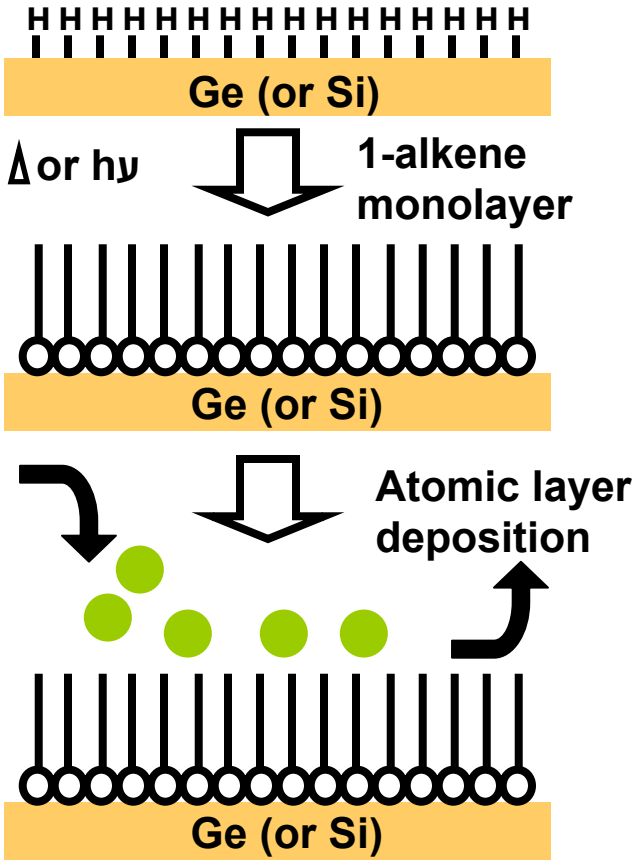


Chen et al. Chem. Mater. 2005, 17, 536

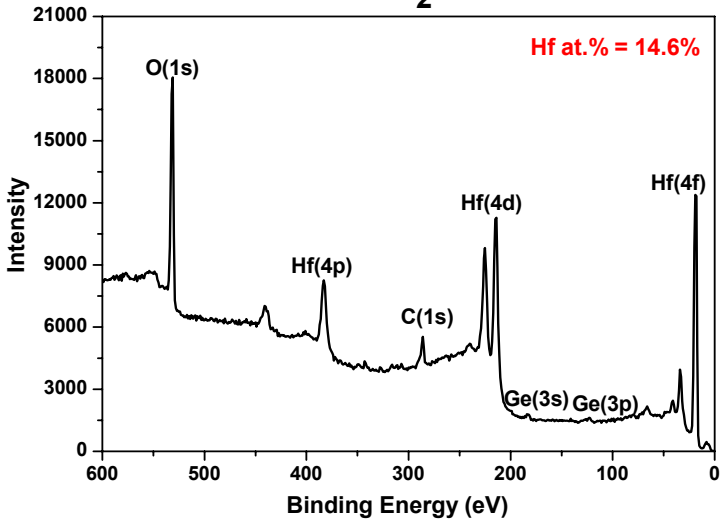
Deactivation of Ge and Si Semiconductors

Direct Attachment

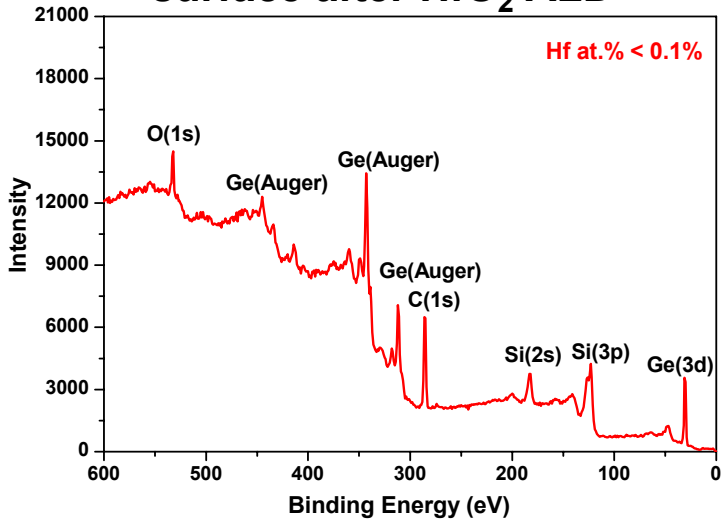
hydrogermylation
or hydrosilylation



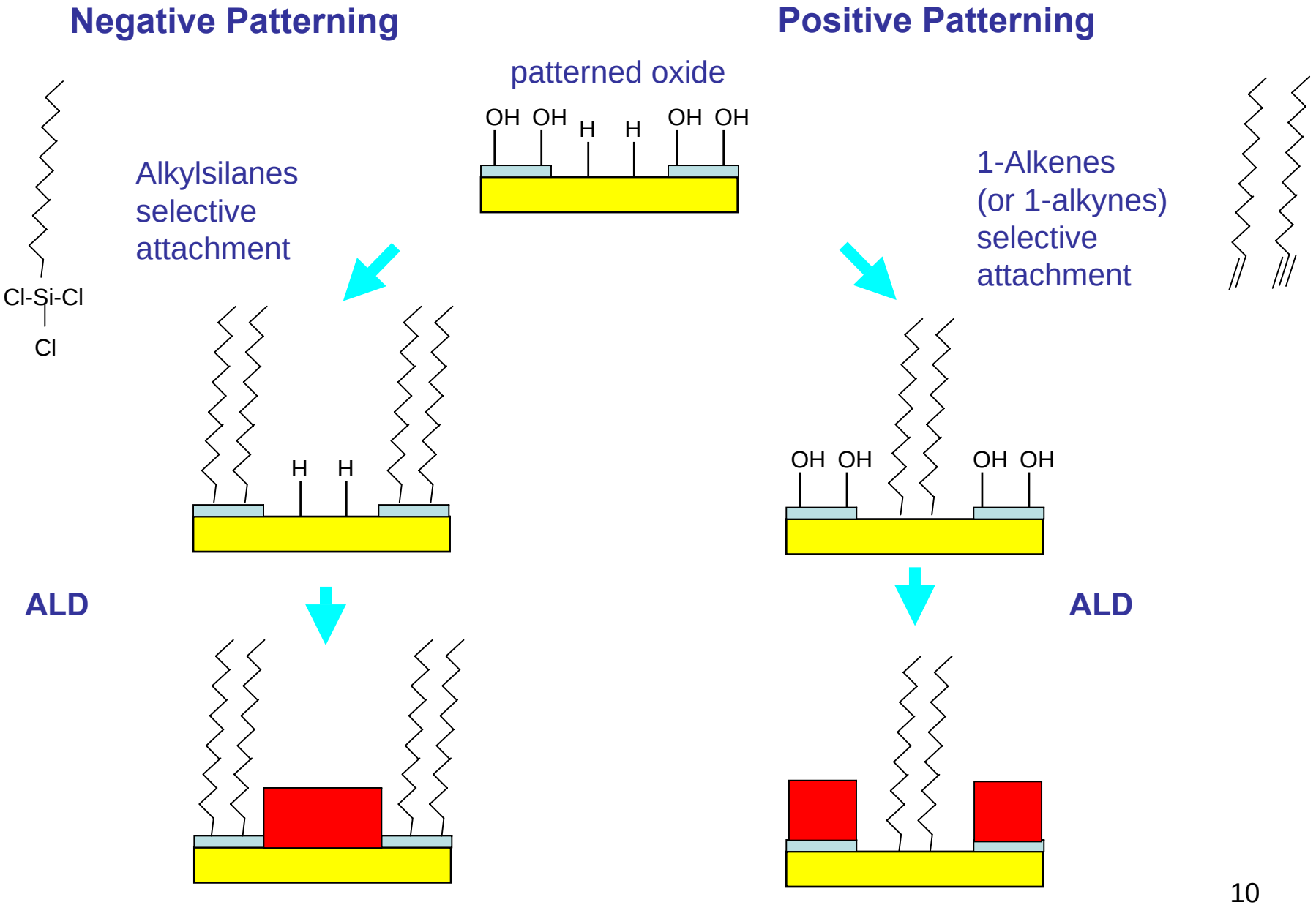
Fresh Ge(100)-H surface
after HfO_2 ALD



1-octadecene deactivated Ge(100)-H
surface after HfO_2 ALD



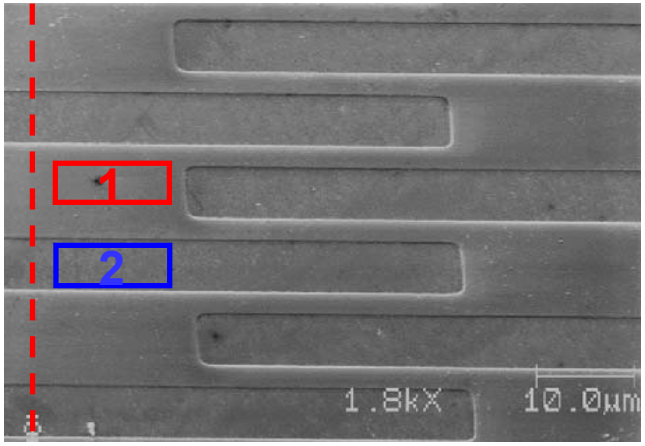
Positive and Negative Pattern Transfers



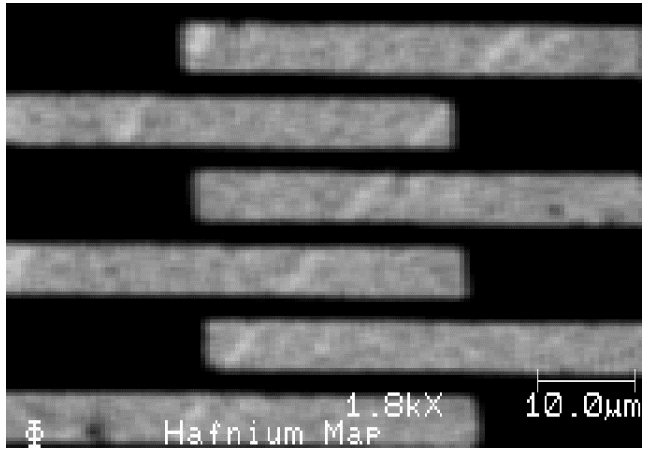
Area-Selective ALD of HfO_2 by Negative Patterning

Area #1, Octadecyltrichlorosilane deactivated oxide surface; Area #2, non-deactivated Si-H surface

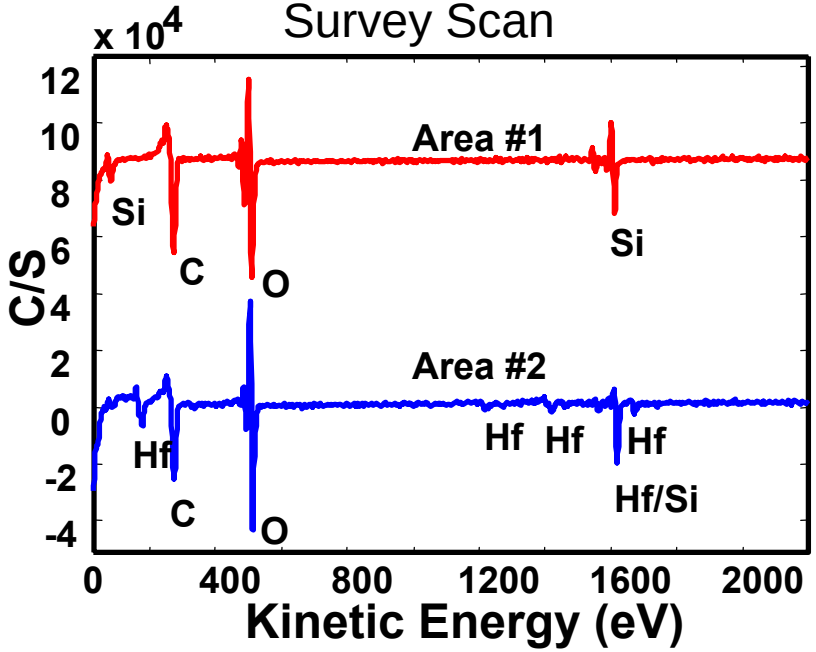
SEM Image



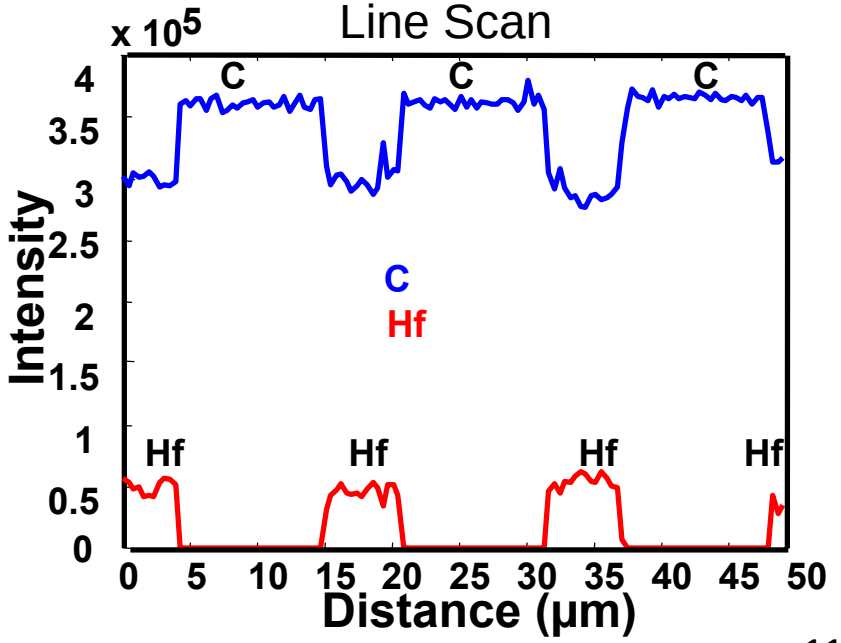
Hf Auger Mapping



Survey Scan



Line Scan

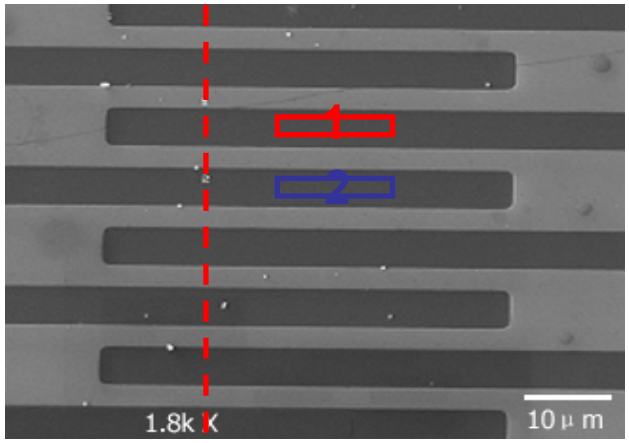


Chen et al. Appl. Phys. Lett. 2005, 86, 191910

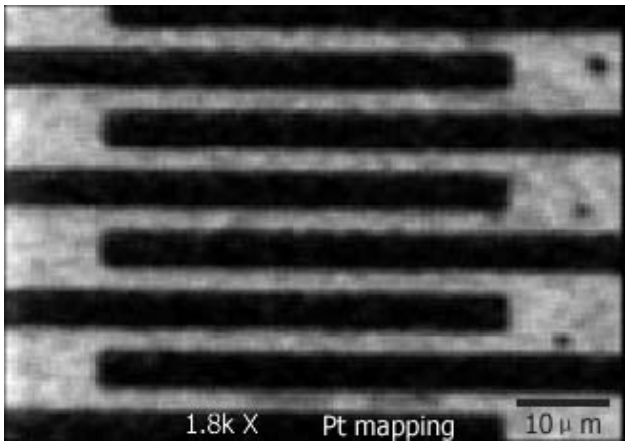
Area-Selective ALD of Pt by Positive Patterning

Area #1, non-deactivated oxide surface; Area #2, 1-octadecene deactivated hydride surface

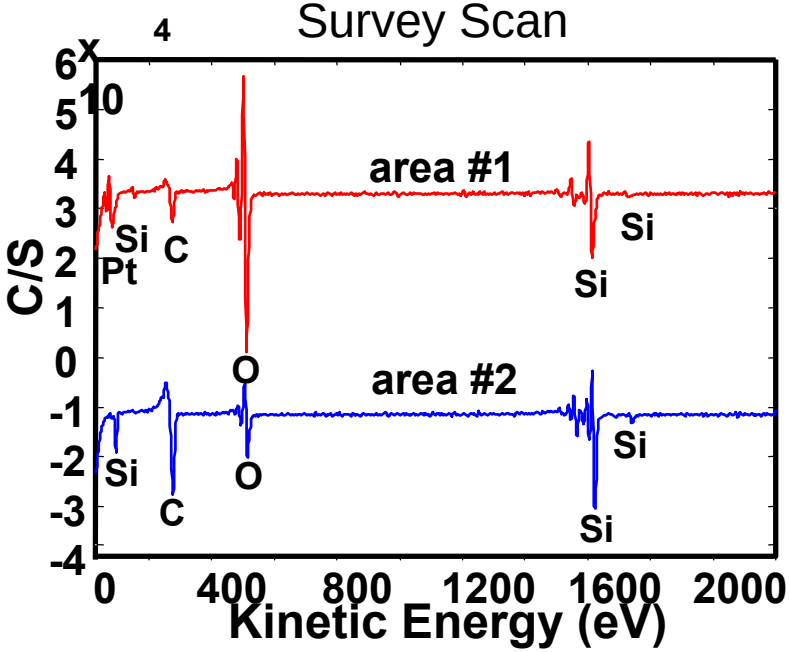
SEM Image



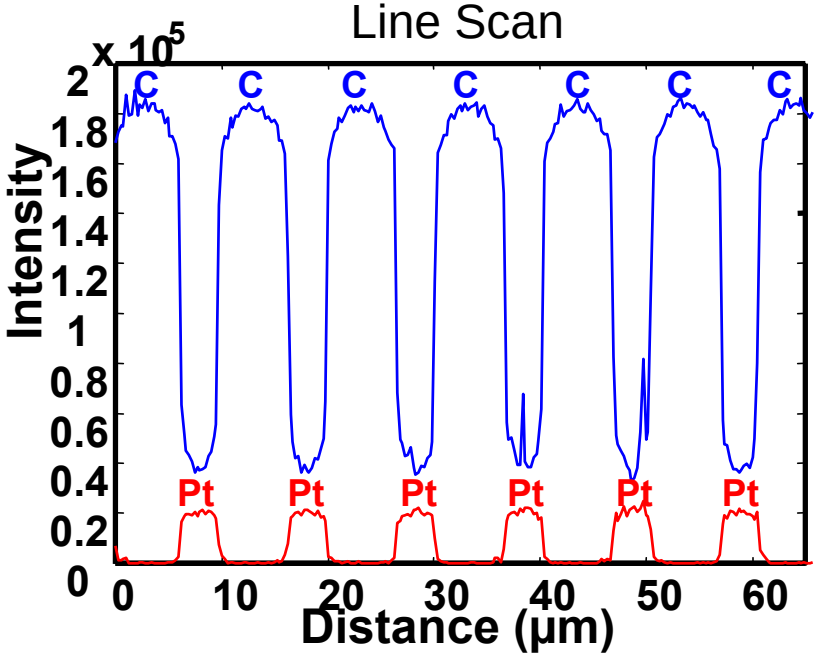
Pt Auger Mapping



Survey Scan



Line Scan



Chen et al. to be published in Adv. Mater. 2006

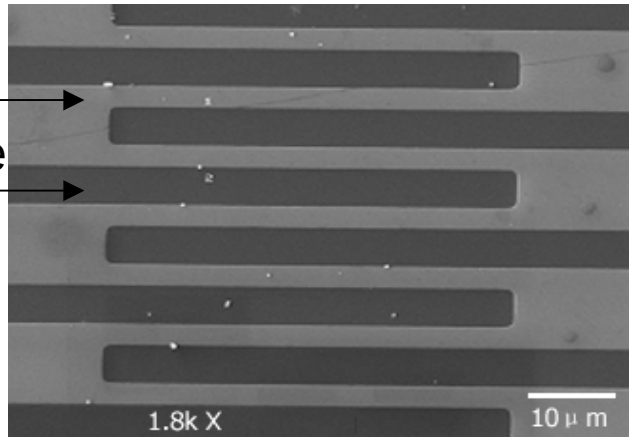
Selective Deactivation on Patterned SiO_2/Si

SEM image of representative structure

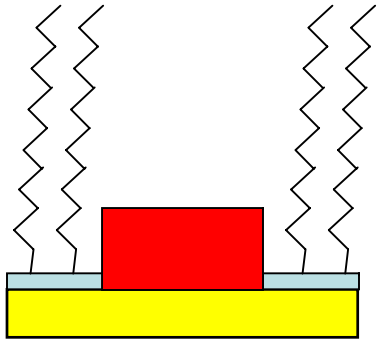
alkylsilanes

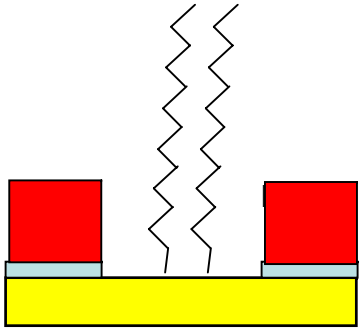
oxide

hydride

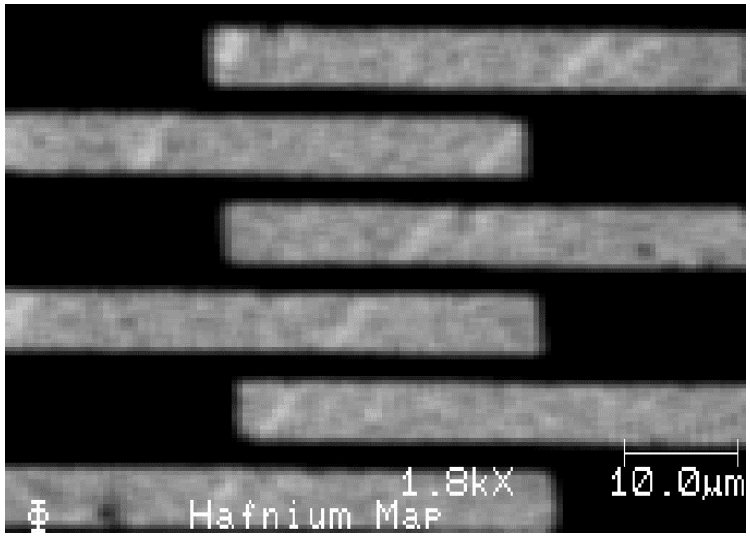


1-alkenes or 1-alkynes

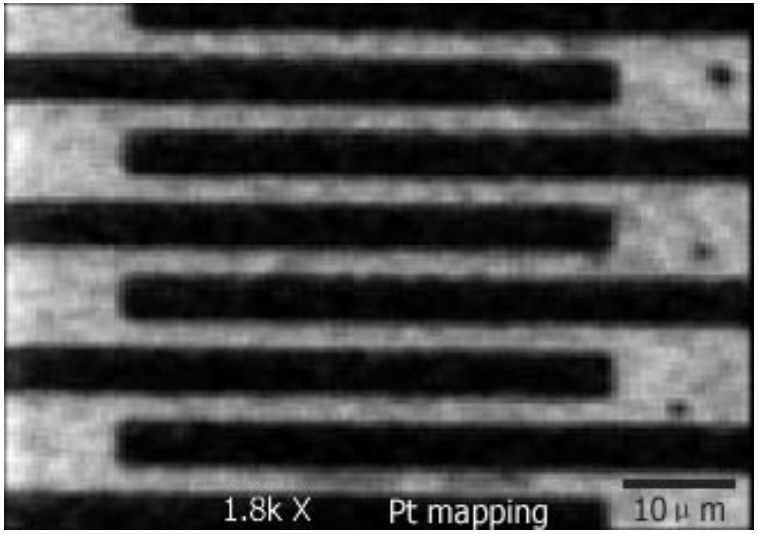




HfO_2 elemental mapping—negative



Pt elemental mapping—positive



Summary

- Deactivation study on SiO_2 by siloxane-based SAMs
- Deactivation study on Ge-H and Si-H by 1-alkenes/1-alkynes and alkanethiols
- Vapor phase SAMs formation and deactivation mechanism study
- Pattern transfer investigation by selective attachment and soft lithography
- Area selective ALD on other dielectrics/semiconductor, e.g. medium-k Si_3N_4/Si and high-k HfO_2/Si
- Electrical characterization on Capacitors fabricated by area-selective ALD

Acknowledgements

People:

Bent group members
Prof. Michael A. Kelly
Dr. Peter B. Griffin
Prof. Krishna Saraswat
Prof. Chris E. D. Chidsey
Prof. Charles B. Musgrave

Funding:

- **NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing**
- **Initiative for Nanoscale Materials and Processes (INMP)**
- **Stanford Center for Integrated Systems (CIS)**
- **Honda**
- **Texas Instruments Graduate Fellowship**

Facilities:

Gate Stack Engineering by Atomic Layer Deposition

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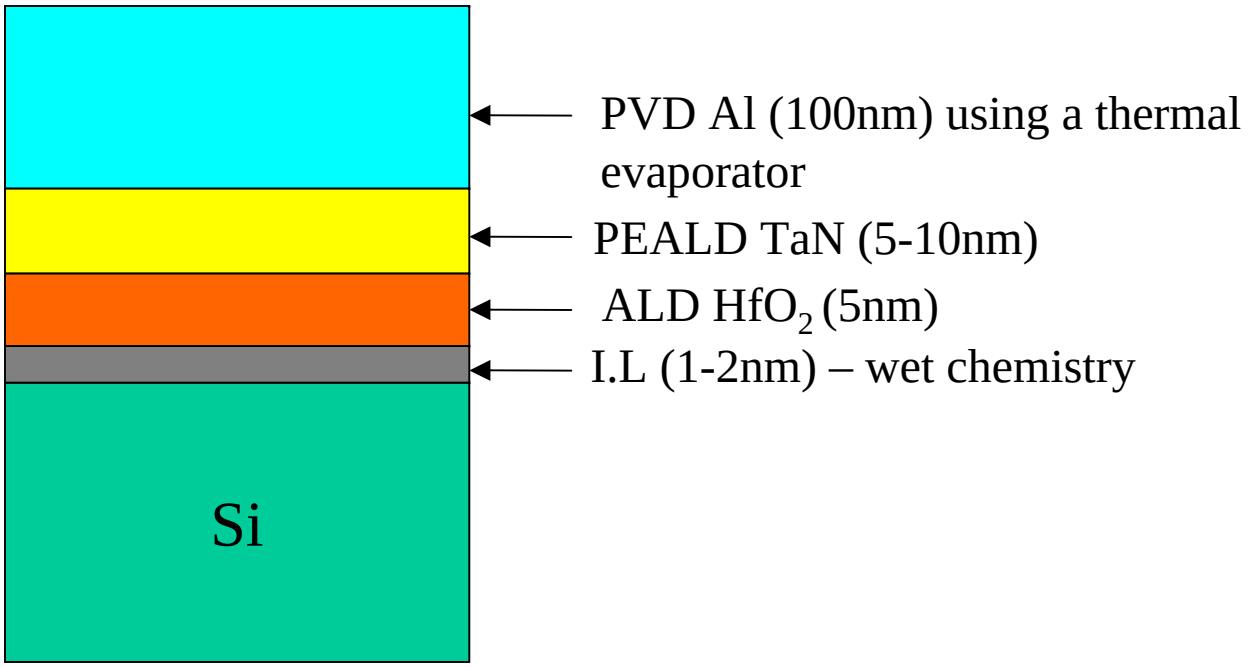
Thrust B, Project 2

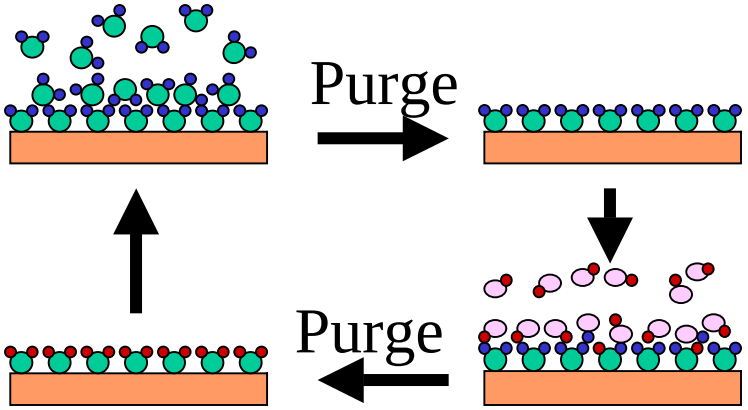
NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

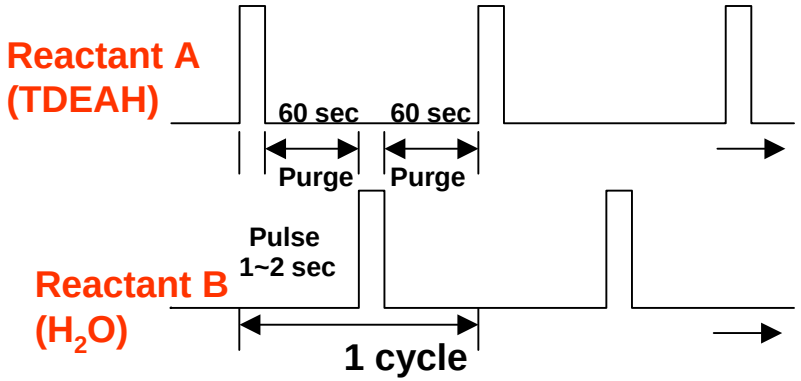
Ultimate Goal



Our goal is to be able to fabricate the entire gate stack without exposure to the ambient. This process has the promise of preventing I.L growth during post processing.

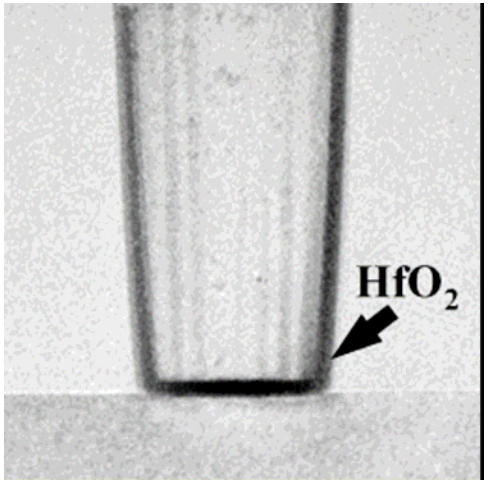
Atomic Layer Deposition





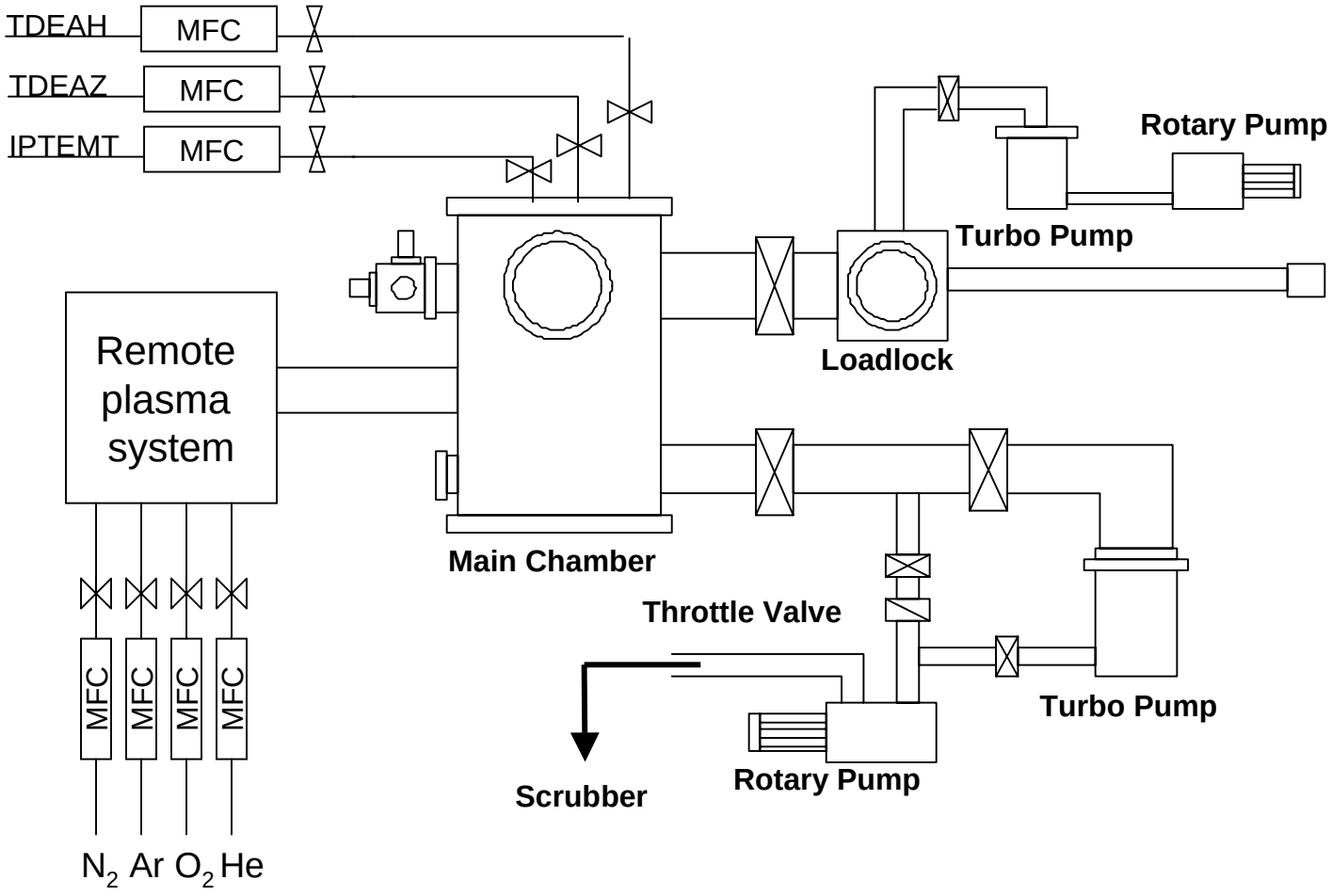
Schematic of the ALD process

- Self-limiting growth
- Highly conformal, low defect thin films
- Very good step coverage
- Low temperature deposition
- Excellent control over film thickness
- Uniform thickness over large areas
- Good control of stoichiometry
- Abrupt interface to the substrate



(courtesy Hyoungsub Kim)

ALD Chamber Layout

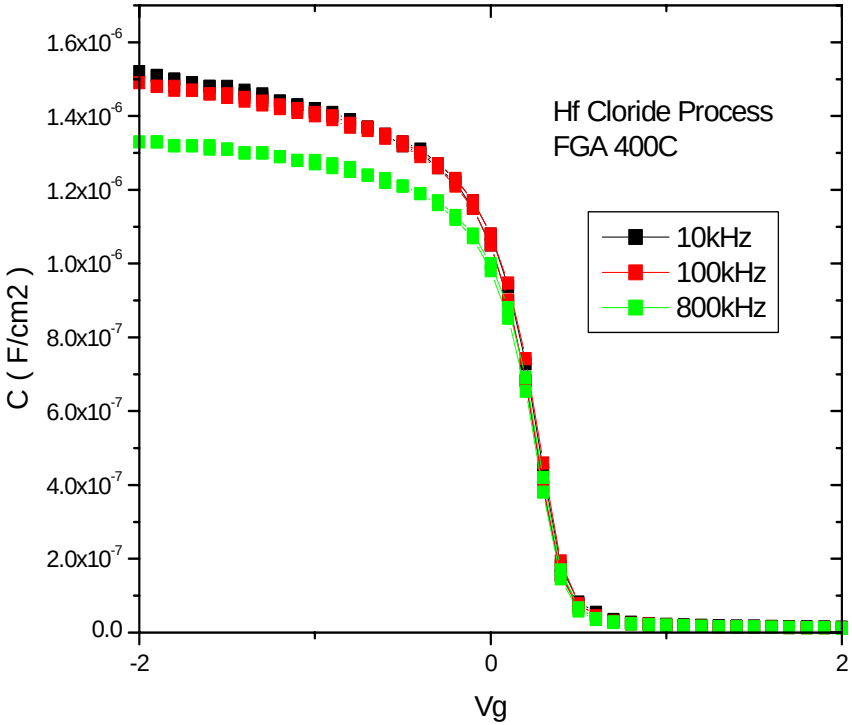


ALD Process Parameters

	$HfCl_4$	TDEAH
Substrate temp	300 °C	**140°C**
Bubbler temp	150 °C	**65°C**
Pulsing	1-60-1-60	1-50-1-50
Dep rate	0.5Å/cycle	**0.75Å/cycle**
Chamber wall	R.T	**75°C**
Oxidizer	H_2O	H_2O
N_2(carrier gas)	20 sccm	2.5 sccm
Process Pr	0.5 Torr	0.5 Torr

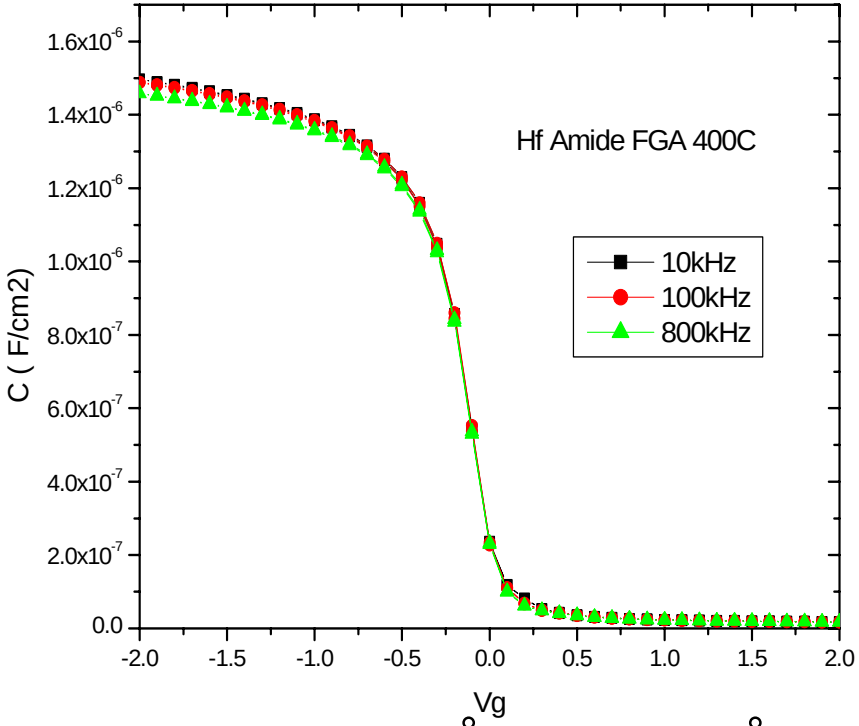
C-V Hysteresis

Chloride



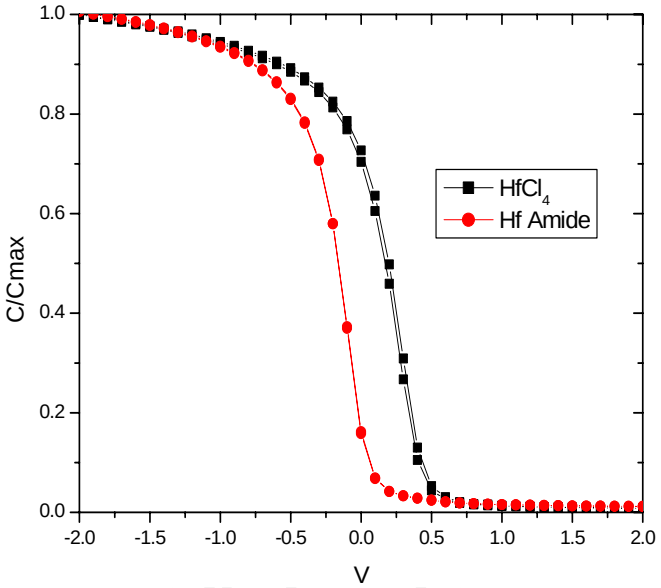
t_{HfO2} = 45Å, I.L = 15Å
Cap derived EOT = 23.1Å
Hysteresis ~ 20 mV

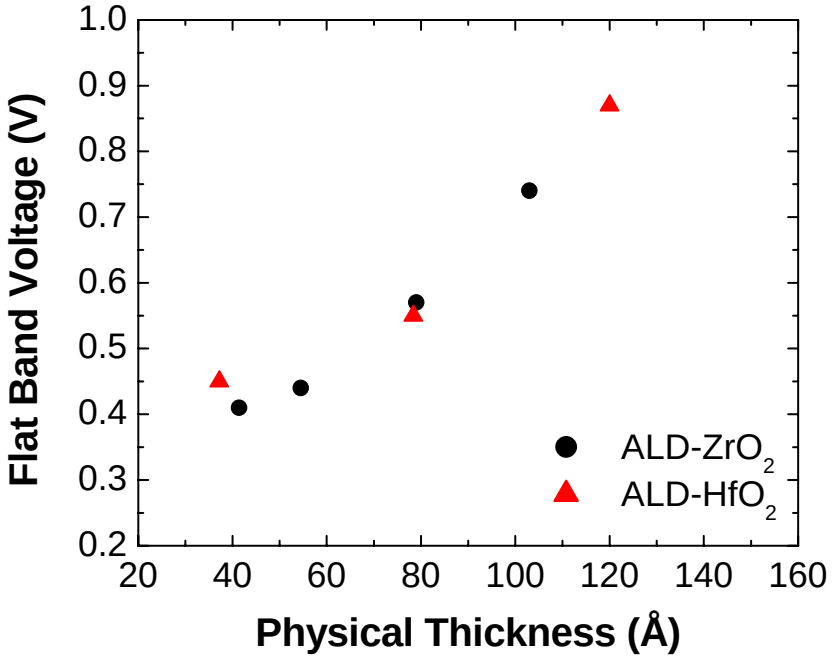
Alkylamide



t_{HfO2} = 50Å, I.L = 15Å
Cap derived EOT = 23.2Å
Hysteresis ~ 5 mV

Precursor Effect on V_{FB}





V_{FB} (alkylamide) = 0.09V

V_{FB} (chloride) = 0.49V

ϕ_{Pt} = 5.25 eV on HfO_2

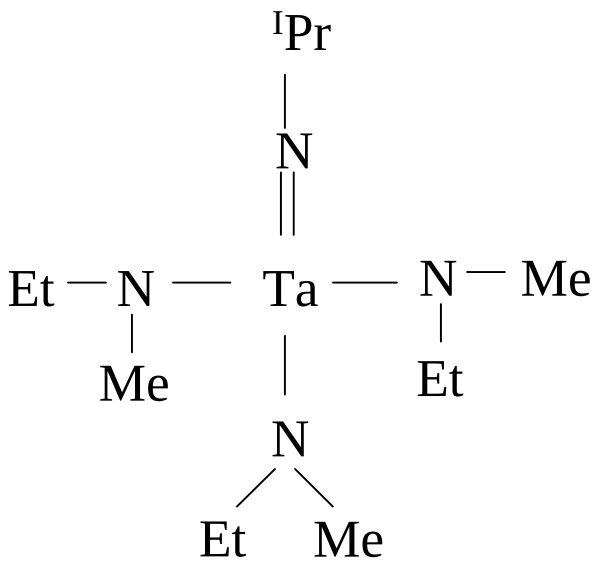
"Ideal" V_{FB} = 0.35V

Q_F (alkylamide) = + 2.4E12

Q_F (chloride) = -1.29E12

Small curvature of V_{FB} vs. thickness suggests fixed charge located mainly at high-*k*/SiO_2 interface with a small "bulk" contribution as well

Plasma Enhanced ALD of TaN



Isopropylimido tris(ethylmethylamino) tantalum (IPTEMT)

Plasma Gas Mixture:
Ar(1000sccm) /N_2 (80sccm)/ H_2(5sccm)

Plasma RF Power: 780W

Process Pr: 1.5Torr

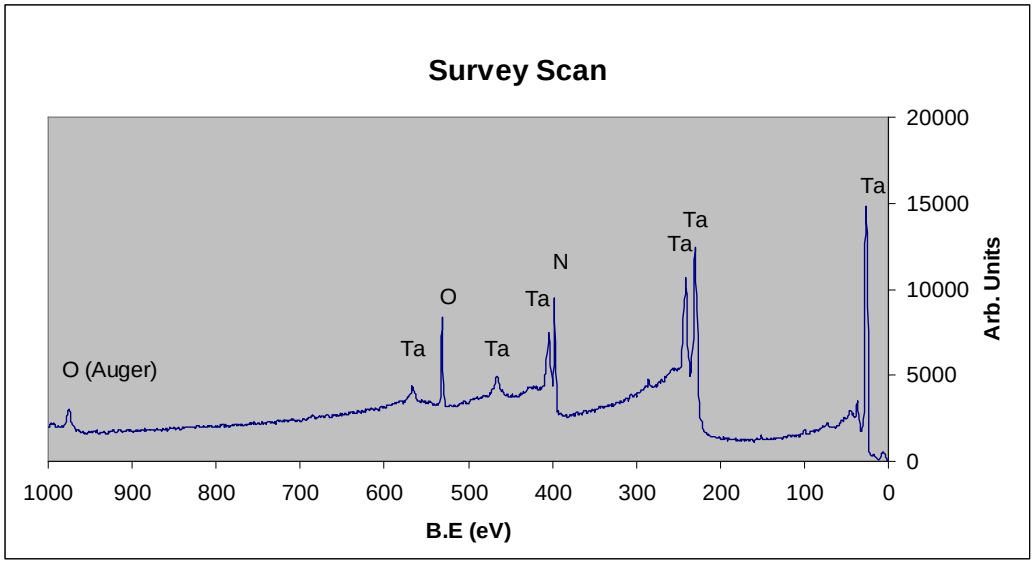
Substrate Temp: 250 - 400°C

Ta precursor: IPTEMT (liq at R.T)

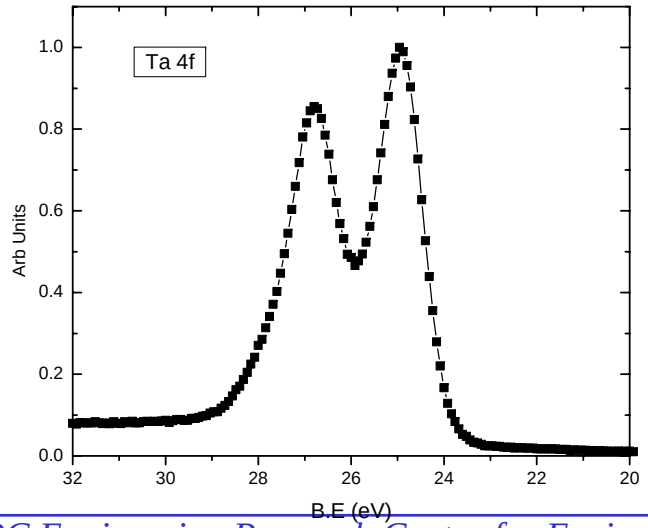
Pulse Times: 10-50-2-50 sec

Growth Rate: 0.45Å/cyl

XPS Spectra

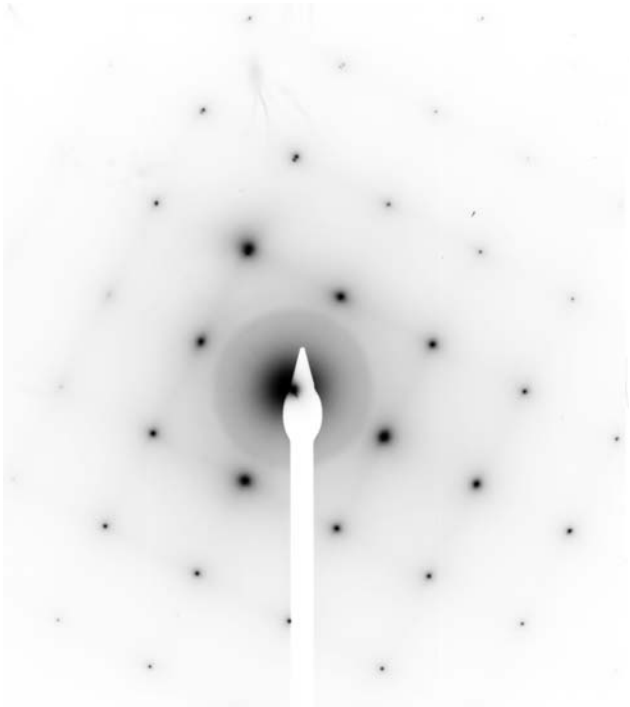


TaxNy deposited @ 400°C showed 35% [N] and 25% [O] in the as-deposited sample. Carbon impurities in the bulk of the film were below the detection limits of the XPS.

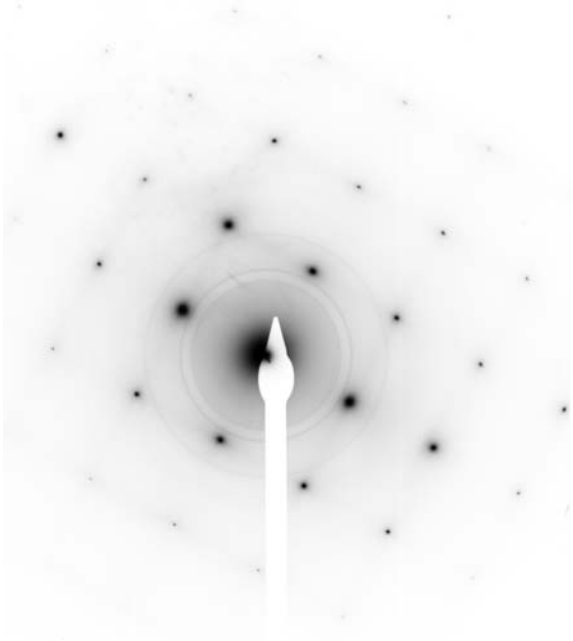


The Ta $4f_{5/2}$ and $4f_{7/2}$ located at 26.7 eV and 24.8 eV resp indicates the as-deposited film to be stoichiometric Ta_3N_5.

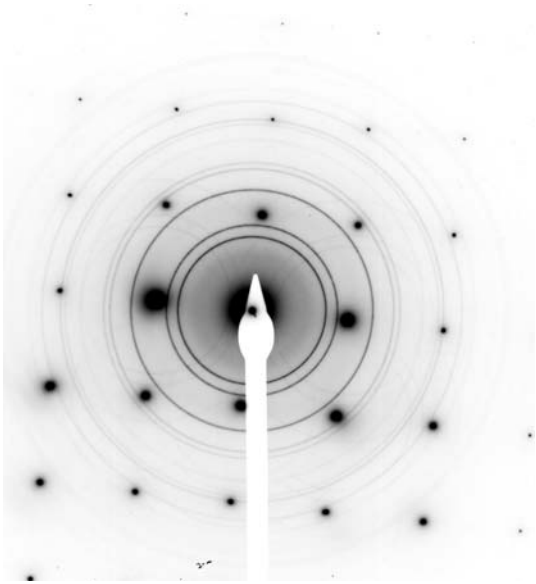
In-situ TEM Annealing



700°C



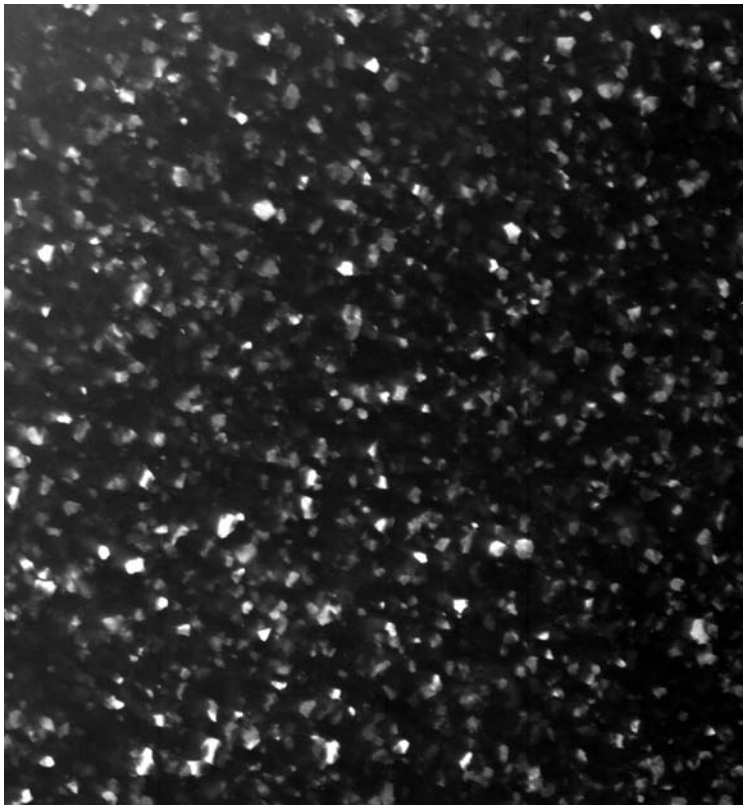
800°C



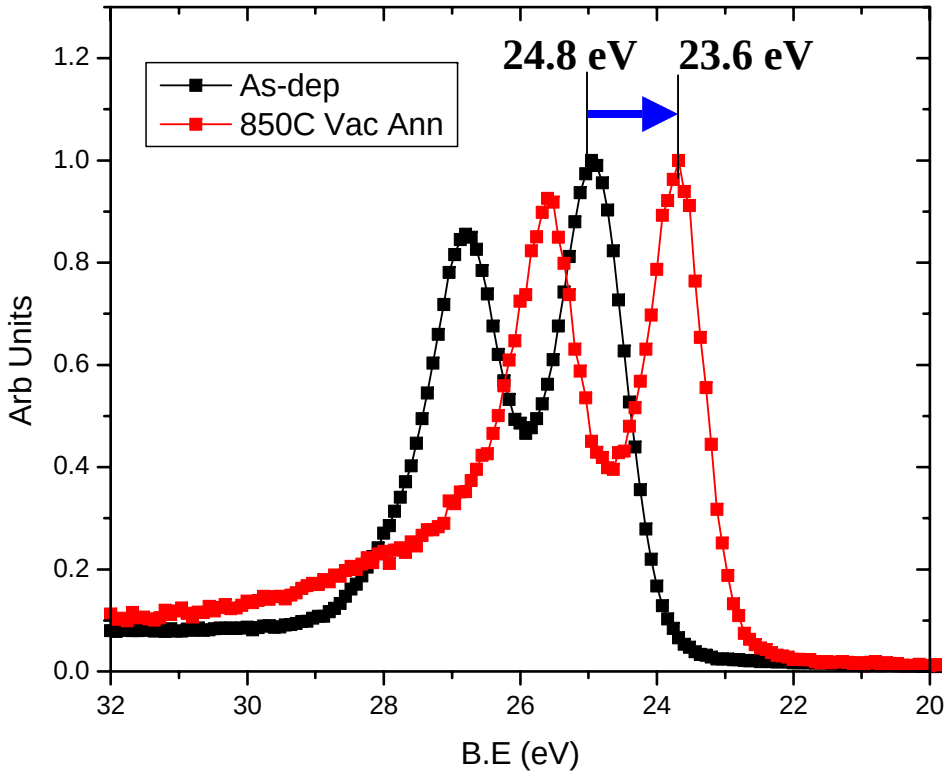
850°C

The Ta_xN_y film deposited on Si/SiO_2 surface crystallized completely at 850°C to form cubic TaN. The observed spot pattern is that of (100) Si substrate.

Stoichiometric TaN



DF image showing TaN crystals after 850°C vacuum anneal



Ta 4f peak shift consistent with the phase change from Ta_3N_5 to cubic TaN

Summary and Future Work

- We have successfully grown high quality HfO_2 thin films on silicon substrates using the ALD process. The electrical characteristics of the HfO_2 films grown using TDEAH are far superior to those obtained using the chlorides.

- We have also optimized a plasma enhanced ALD process to deposit Ta_xN_y at 400 °C which crystallized into stoichiometric cubic TaN when annealed in vacuum at 850°C.

- We are currently working on integrating the two different processes to fabricate capacitors with HfO2 dielectric and TaN metal gate.

- The ESH implications of the Hafnium and the Tantalum precursors have been analyzed.

Improvement of NBTI of High-*k* by Incorporation of Fluorine

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Task B-2

Selective Surface Preparation and Templated Atomic Layer Film Deposition: Novel Processes for Environmentally Benign Transistor Gate Stack Manufacturing

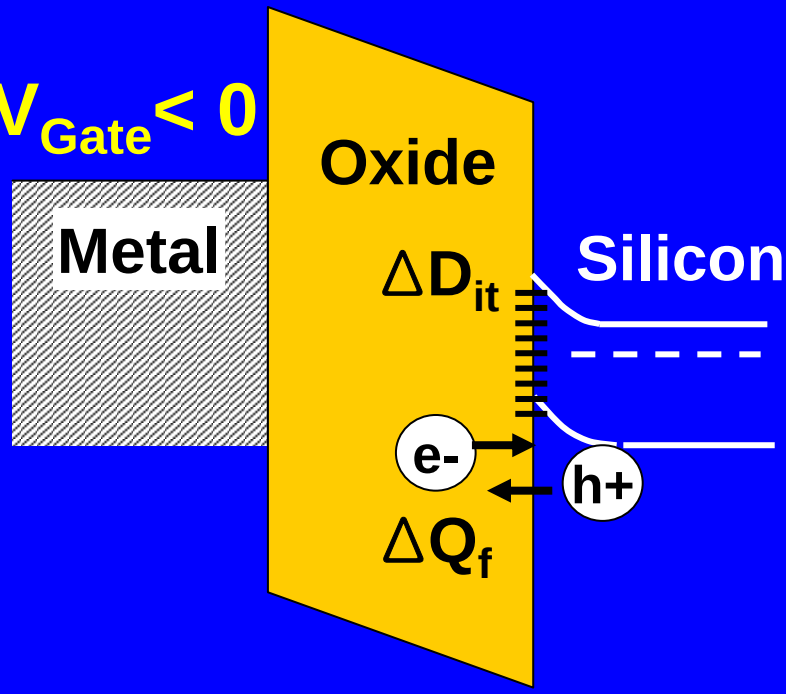
NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

NBTI in MOS devices

- What is Negative Bias Temperature Instability (NBTI) ?

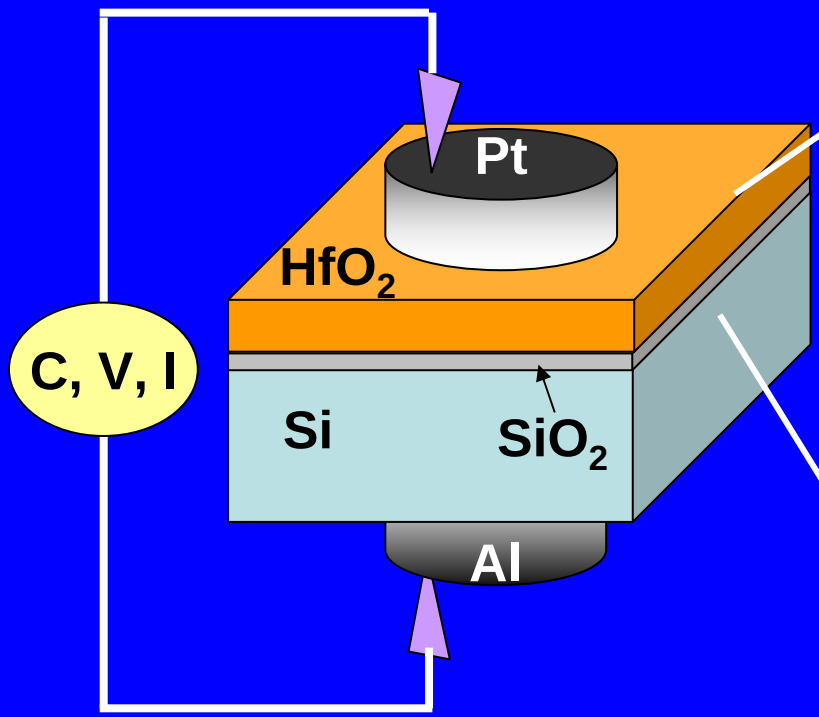
➔ Generation of interface traps (ΔD_{it}) and positive charges (ΔQ_f) under negative gate bias especially in elevated temperature.

➔ $V_T \uparrow$, $I_{off} \uparrow$, $I_{Dsat} \downarrow$, $g_m \downarrow$ with time in p-channel MOS

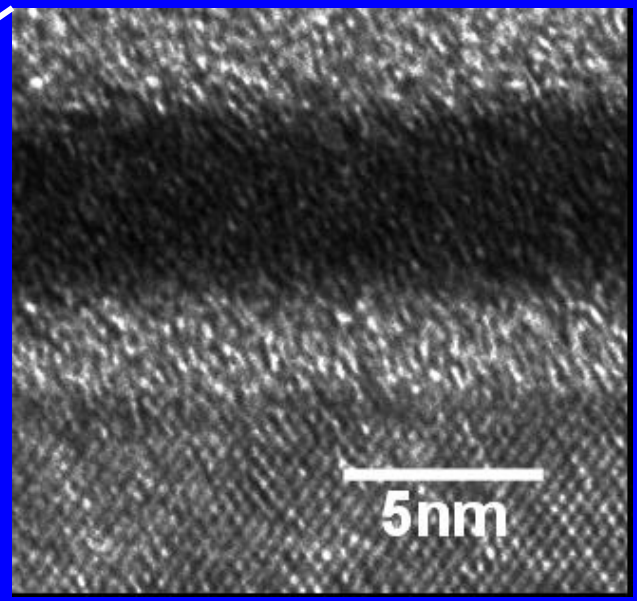


$$\Delta V_T = q\,(\Delta Q_{it} + \Delta Q_f)\,/\,C_{ox}$$

MOSCAP structure & TEM



- Cross sectional TEM



Glue

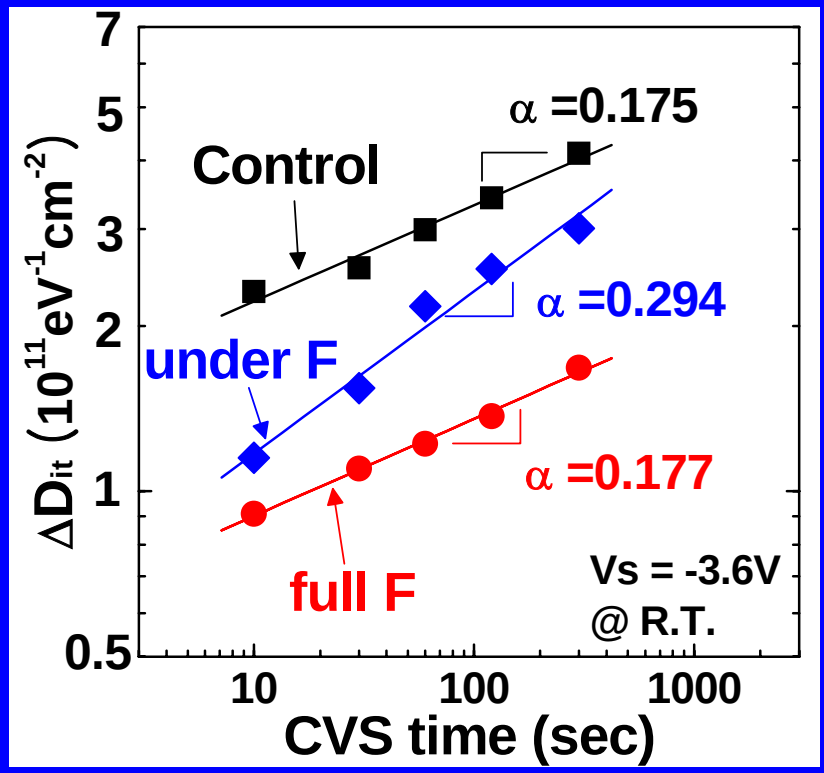
ALD-HfO_2 = ~5nm

SiO_2 = ~2nm

Si (001)

➔ Amorphous HfO_2 with smooth interfaces

“F” effect on ΔD_{it}



- Based on R-D model,

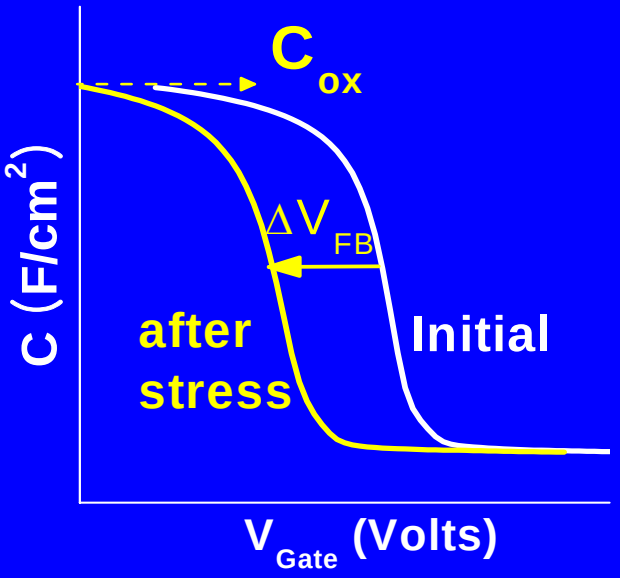
$*\Delta D_{it} = CE_{ox}{}^{s}\exp(-E_A/k_BT)\, t^{\alpha}$

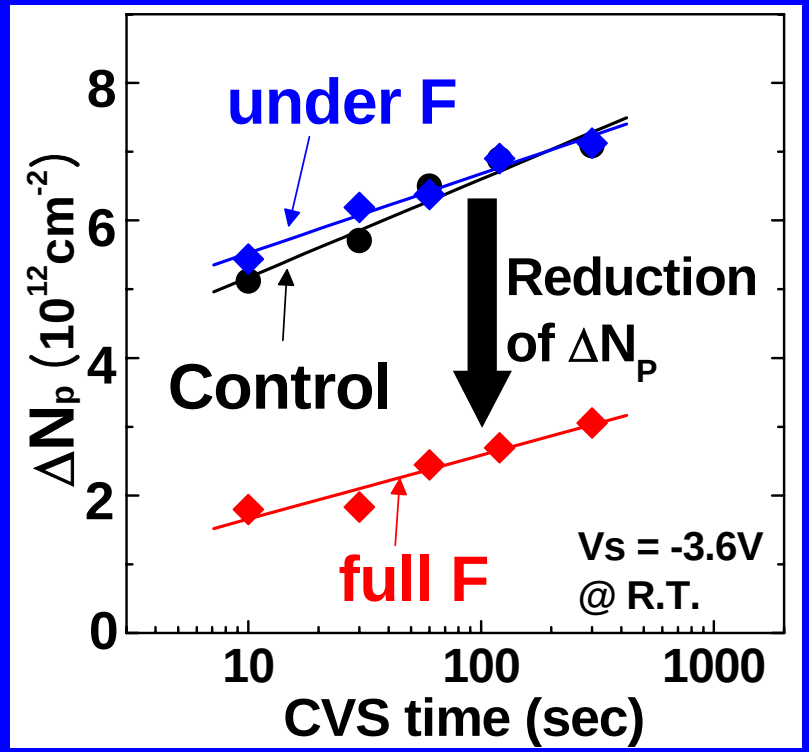
* Shigeo Ogawa and Noboru Shiono, *Physical Review B*, vol. 51 p 4218, 1995

➔ ΔD_{it}(full F) < ΔD_{it}(under F) suggests gentle introduction of F at SiO_2/Si interface by F diffusion through HfO_2 is desirable.

“F” effect on ΔN_p

- $\Delta N_p = -C_{ox}\Delta V_{FB}/q$

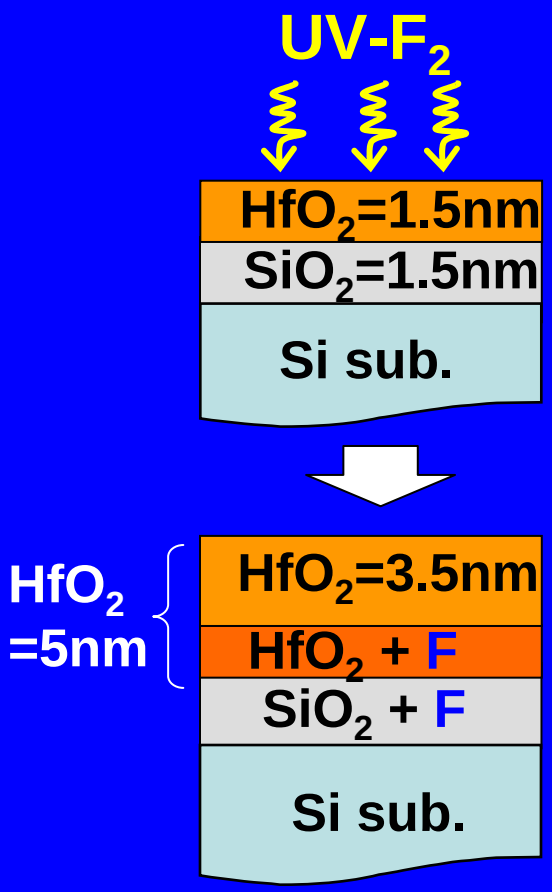


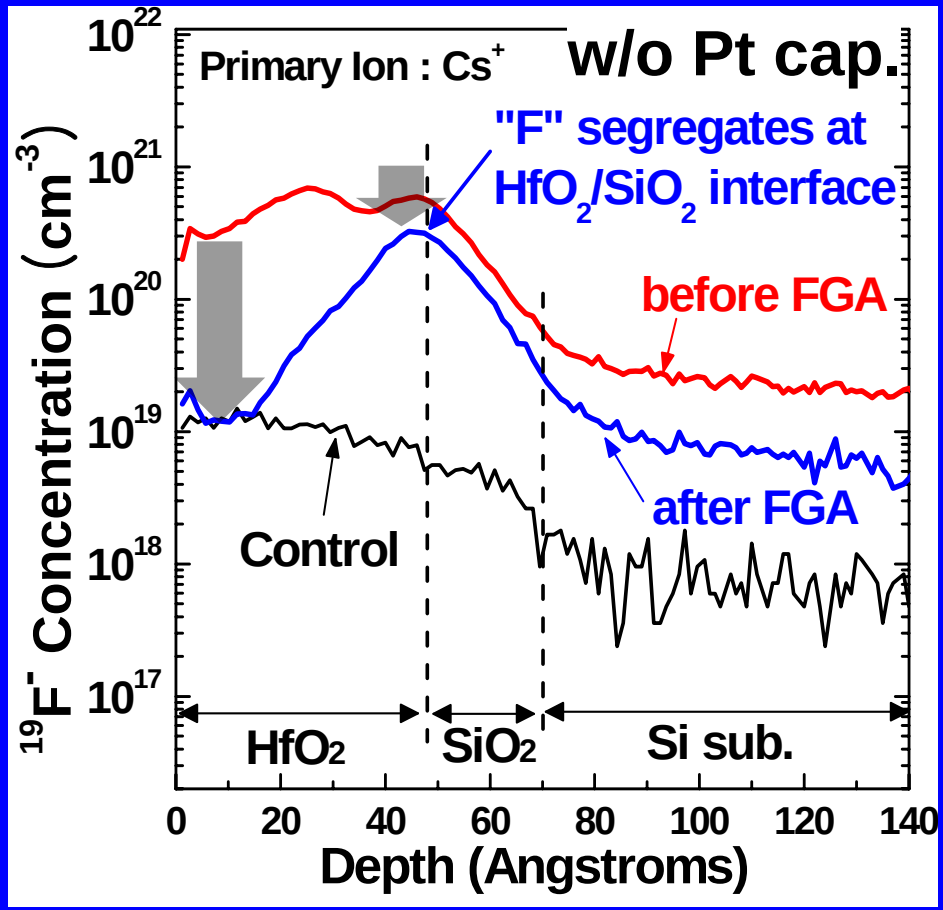


➔ ΔN_P(full F) < ΔN_p(control) ≈ ΔN_p(under F) indicates that F passivates hole trapping sites in HfO_2 bulk or HfO_2/SiO_2 interface.

“F” SIMS profile of “local F”

- Local F

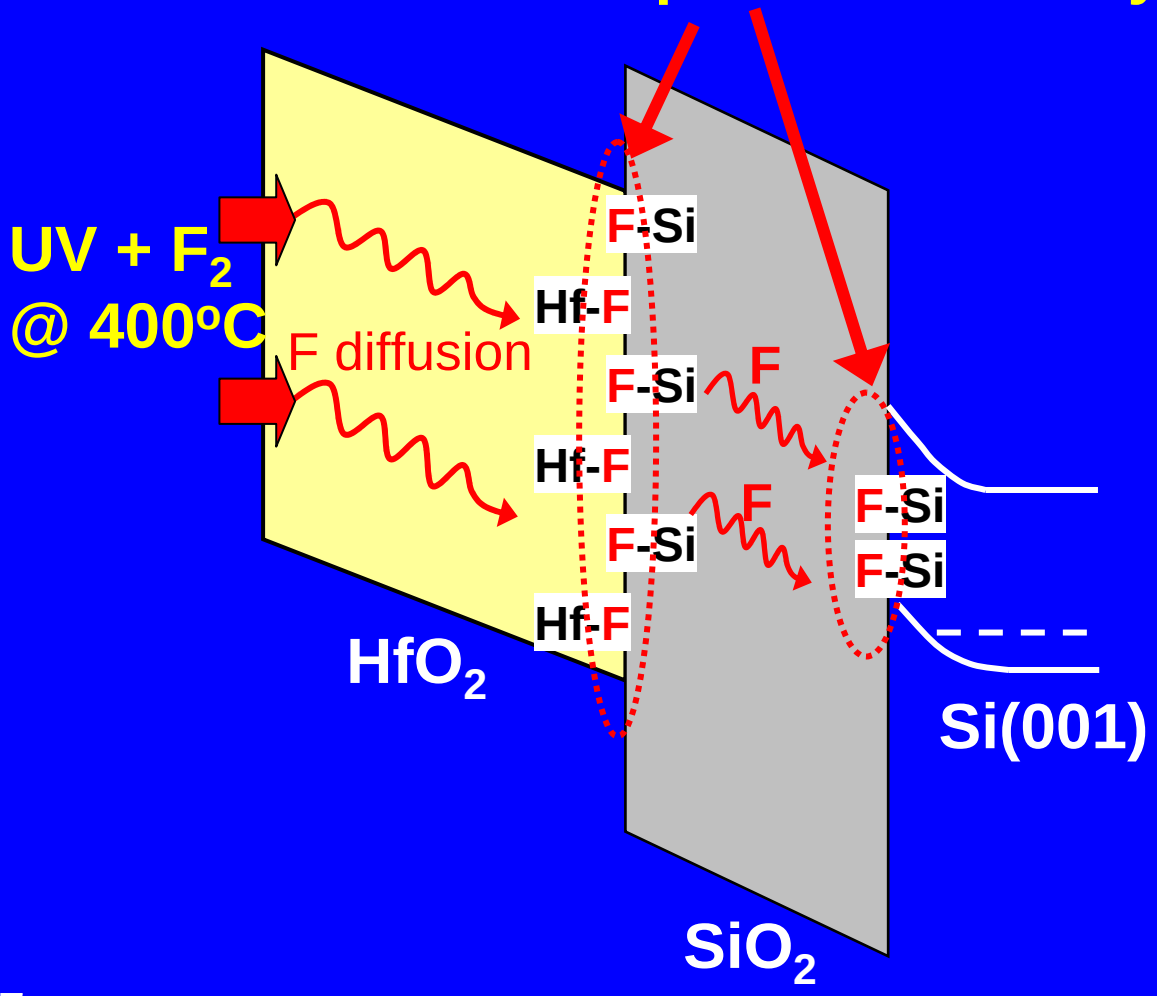




➔ “F” at HfO_2/SiO_2 forms more stable bonds than “F” in bulk HfO_2.

Mechanism of “F” effects

Strong Hf-F, Si-F bonds at interfaces improves reliability



*Bond Enthalpy (KJ/mole)

Si-H	299
Si-O	800
Si-F	553
Hf-H	?
Hf-O	802
Hf-F	650
Ti-H	205
Ti-O	672
Ti-F	569

*www.webelements.com; J. A. Kerr, “CRC Handbook of chemistry and physics 1999-2000”

Conclusion

- **Demonstrate that "F" incorporation reduces NBTI significantly in "high-*k*(HfO_2) / metal gate" system (<50%) ; $\Delta D_{it} \downarrow$, $\Delta N_P \downarrow$, and $\Delta V_{hys} \downarrow$.**
- **Demonstrate engineering of "F" profile to segregate at HfO_2/SiO_2 and SiO_2/Si interfaces is effective in reducing NBTI without deteriorating leakage current.**

Acknowledgements

- **Prof. Yoshio Nishi and Prof. Baylor B. Triplett for helpful discussions on electrical data. Prof. Mike Kelly for helping XPS analysis.**
- **Funding: NSF/SRC Center for Environmentally Benign Semiconductor Manufacturing, MARCO Center for Materials Structures and Devices, INMP program (Stanford)**

Task B-3: Evaluating EHS Impacts of New Dielectric and Conductor Materials Etch Processes

Modeling of Inductively Coupled Plasmas

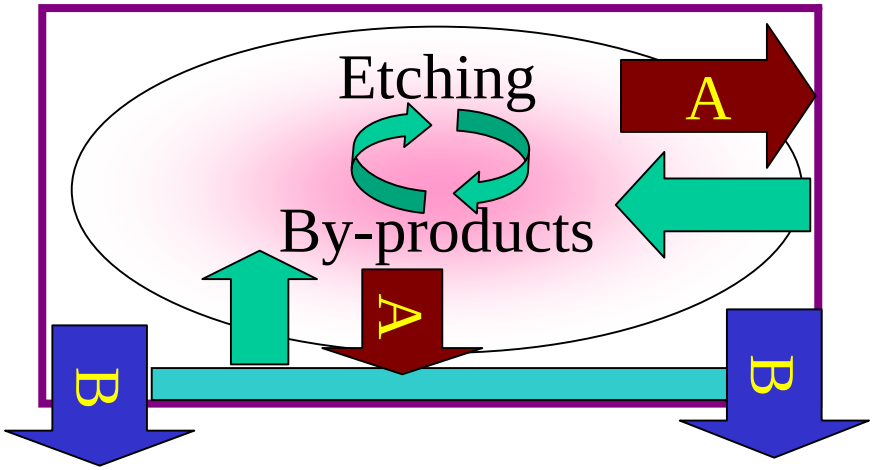
Cheng-Che Hsu, Dr. Mark A. Nierode and
Prof. David B. Graves
Department of Chemical Engineering
University of California, Berkeley

Feb. 23-24, 2006
ERC Review
Tucson, Arizona

ESH Impact of Etching Processes

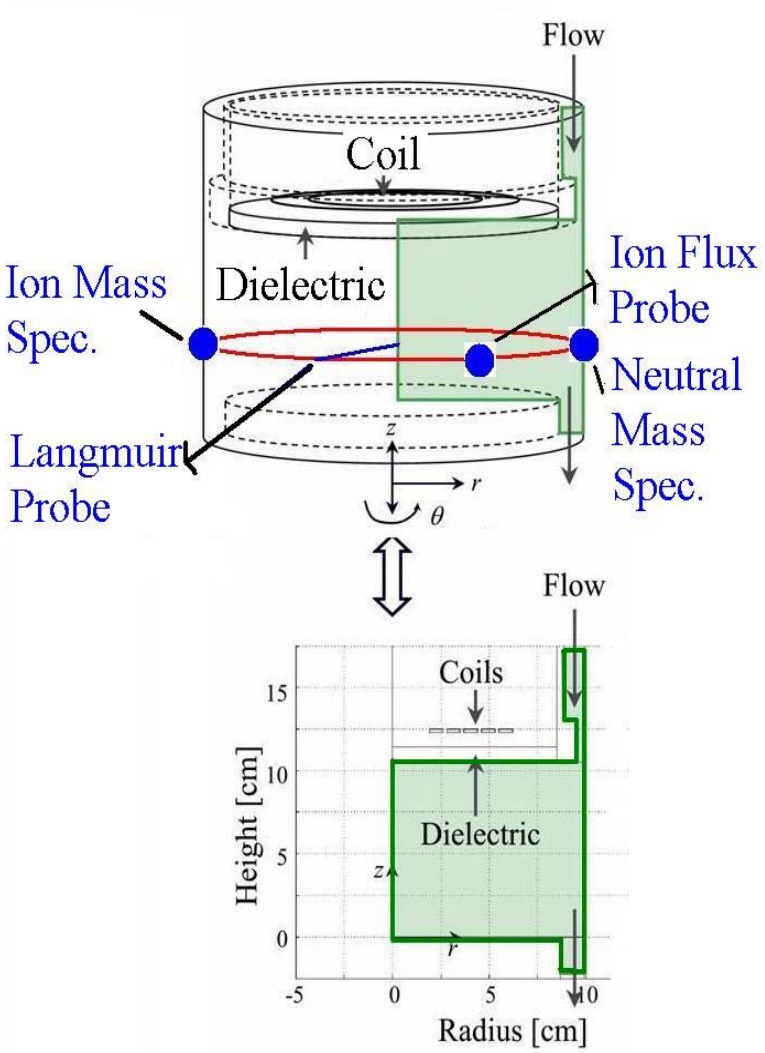
By-products formation and transport have both process and **ESH significance**.

- **Etching processes**
  - **Large set of chemistries**
  - **Potential toxic by-products.**
  - **Process is complicated, (through gas phase or surface reactions) but very little is known.**
- **ESH significance of by-products:**
  - **A: Wall re-deposition: potential threaten the worker.**
  - **B: Effluent: ESH Impact**
- **Goal**
  - **Understand mechanism**
  - **Identify/Predict the condition with minimum emission**



- **Methodology**
  - **Predictive model development**
    - **Validation: Exp. Testbed at UCB (Ar/O_2 plasmas)**
  - **Extend the model capability to different chemistries and reactors.**
  - **Assess process ESH impact.**

System



Experimental System*

- Diagnostic ICP
  - Multiple Diagnostics
  - Fits 6-in wafer
  - Well-defined boundaries
  - Axisymmetric

Model

- 2D, Fluid Model
- Ar/O_2 ICP as the preliminary test
- Femlab™ and Matlab™
  - Coupled neutral and plasma model
  - Easy to share / access
  - Easy to extend to different chemistries/systems

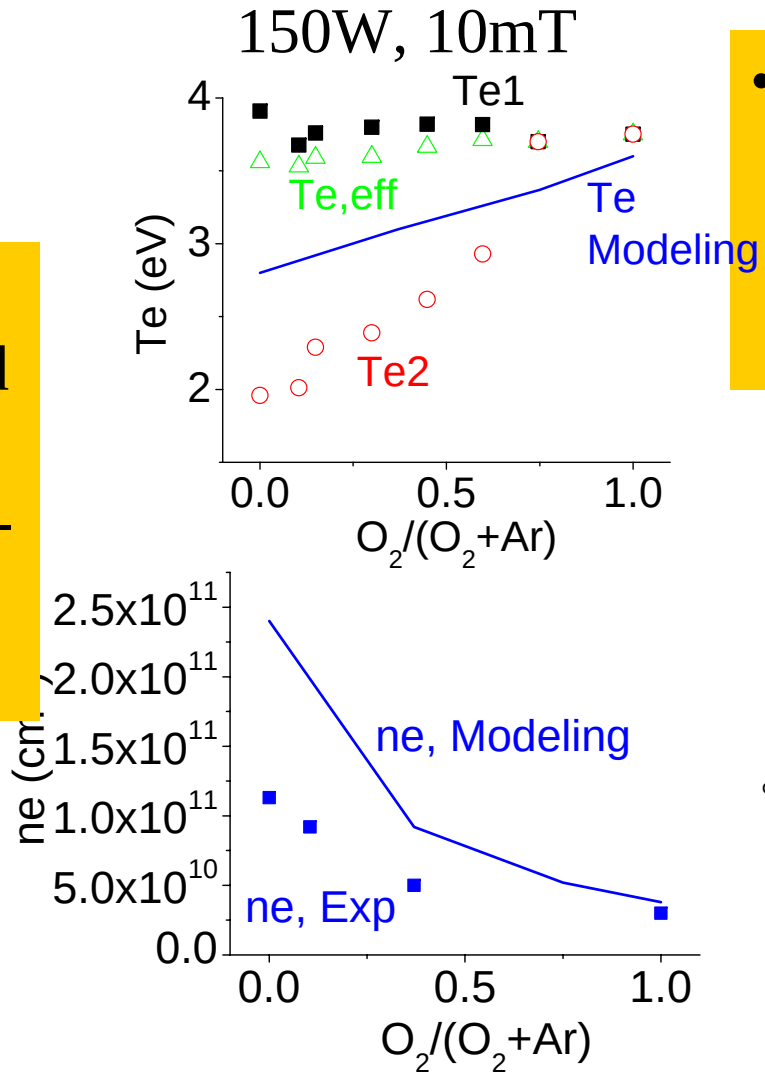
*H. Singh, et. al, J. Vac. Sci. Technol. **19**, 718 (2001),

Model Description

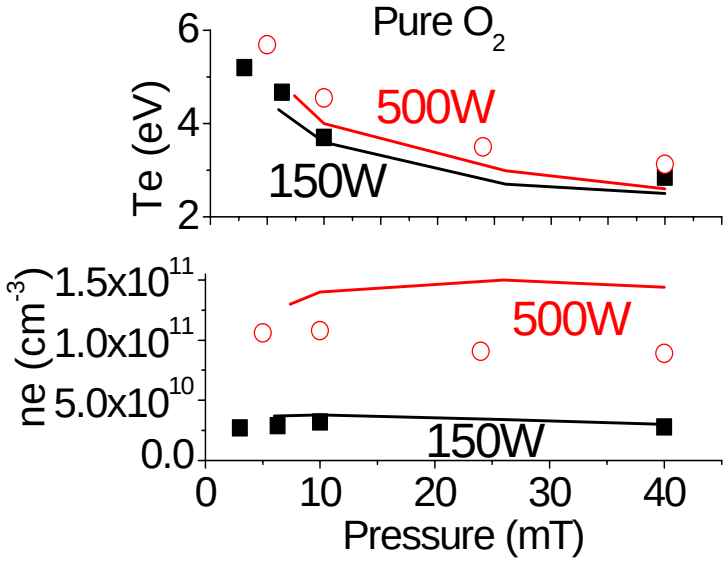
- A fluid model solving for neutrals, ions, electron temperature, and E-field.
- With the developed iteration scheme, able to handle up to 9 neutral species, and 8 charged species (totally 22 equations) with PC (~1GB memory). Model is shown robust and easy to converge.
- Chemistries in Ar/O_2 plasmas:
  - Neutrals: ground state Ar, O_2, O, and metastable O_2 and O
  - Ions: Ar^+, O_2^+, O^+, O^-
- Model and Experiment Comparison
  - ne profile, center ne, and Te,
  - n_O , total ion flux and composition at the wall.

ne and Te comparison in Ar/O_2 Plasmas

In pure Ar, not accurate ne and Te prediction. Caused by non-Maxwellian EEPF.



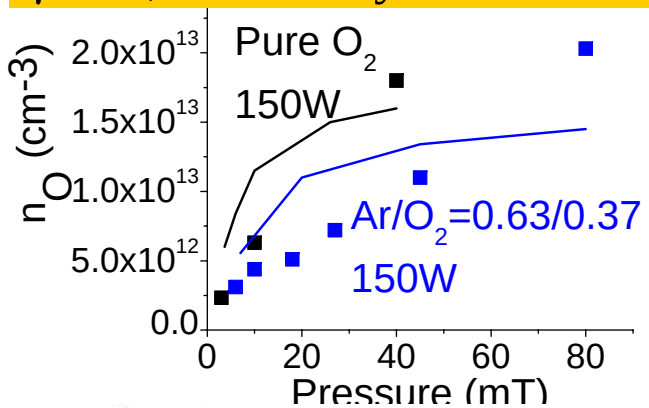
- Maxwellian EEPF at O_2-rich conditions*.
  - Good Te prediction
  - Good ne prediction

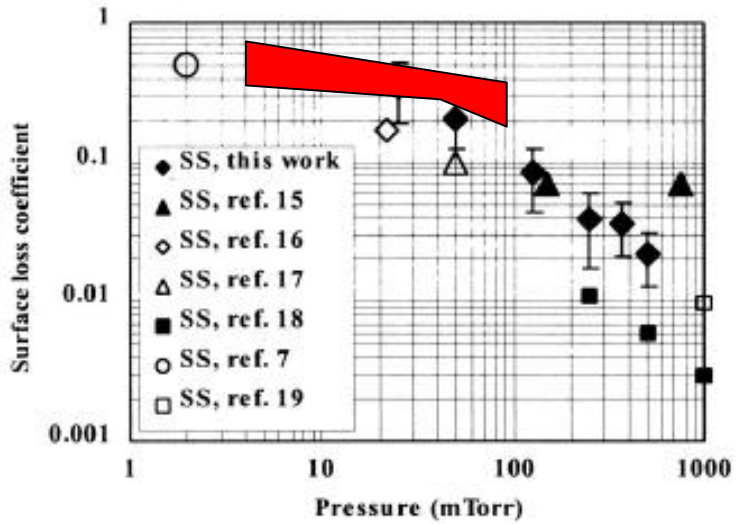


*H. Singh, et. al., J. Appl. Phys. **88**, 3889 (2000)

nO , Ip and its composition comparison

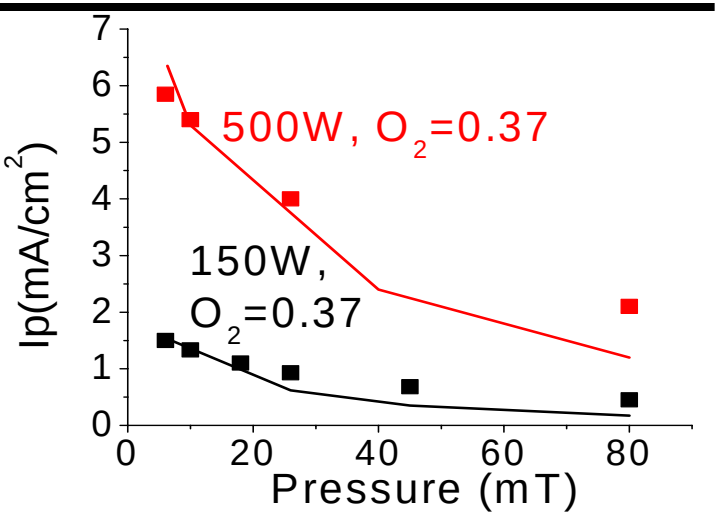
γ=0.3, and Cosby's cross sections

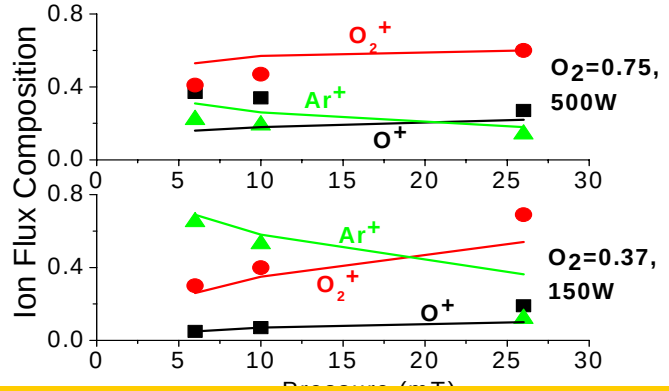




S Gomez, W. Graham et. al. J. Appl. Phys. **81**, 19 (2002)

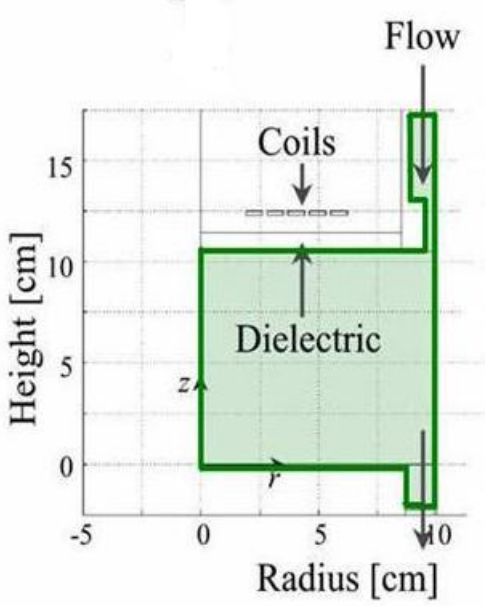
- **γ=γ(p), and Cosby's cross sections.**

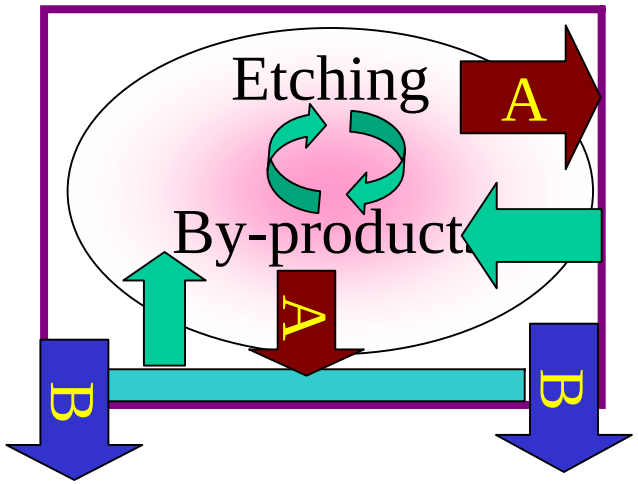


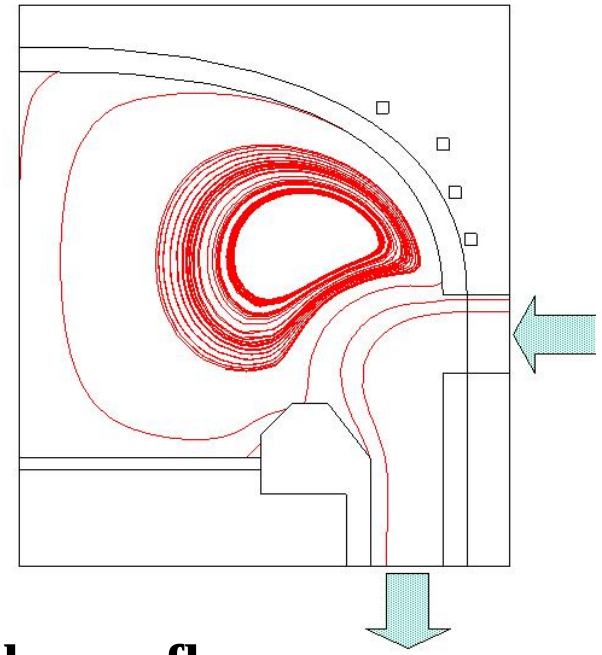


- **Captures Ip and its composition.**
  - **Ip is more controlled by u_b(Te).**
  - **Significant charge exchange.**

Achievement and ESH Significance







- **An ICP predictive model, couples neutral and plasma flow**
  - **Easy to converge, to share, and flexible (chemistries and systems).**
  - **Validated by a diagnostic ICP in Ar/O_2 plasmas.**
- **ESH significance: for commercial tools, e.g. AMAT Al etcher**
  - **Predicting pollutant flux to the wall and to the emission.**
  - **Predicting the condition that minimizes pollutant emission.**

Acknowledgement

- NSF/SRC ERC for Environmentally Benign Semiconductor Manufacturing
- University of California Discovery Grant through the Feature Level Compensation and Control Project
- Victor Vartanian, Brian Goolsby, Peter Ventzek, Da Zhang, Shahid Rauf, and Laurie Beu, Motorola APRDL
- Krishna Saraswat and Jim McVittie, Stanford (materials, device, profile)
- Rafael Reif and Ajay Somani, MIT (experiment)
- Bing Ji, Air Products (etch gases, plasma characterization)
- John Daugherty and Harmeet Singh, Lam Research (tool, wall interactions)

Thrust C

Factory Integration

Overview

Thrust C Focus and Objectives

Resource Use Minimization

Novel Low-energy Water Purification and Wastewater Treatment

Water Use Reduction During Wafer Rinsing

Water Reuse and Recycle

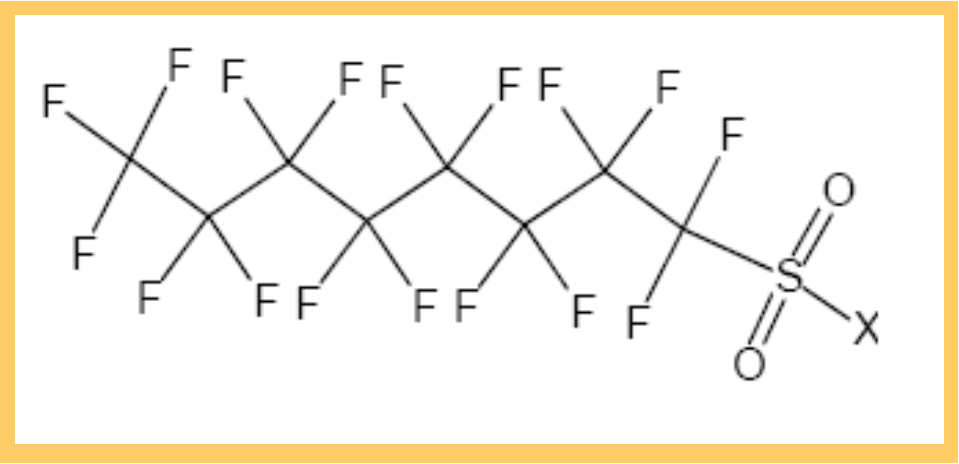
ESH Impact Assessment

Tools and Techniques for Rapid ESH Assessment of Chemicals:

- New chemicals
- New process-generated by-products

Development of Techniques for Integrated Assessment of ESH Impact

Treatment of PFOS in Semiconductor Effluents



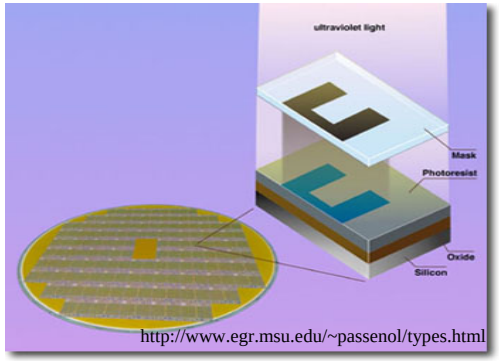
Reyes Sierra and Jim Farrell

Dept. Chemical & Environmental Engineering
University of Arizona

PFOS: A Critical Material in Semiconductor Manufacturing

PFOS/PFAS are critical constituents of leading edge photoresists for use as photoacid generators (PAGs) and surfactants in anti-reflective coatings.

Increasing evidence of the significance of PFOS/PFAS as persistent - bioaccumulative – toxic (PBT) contaminants.



Photolithography Semiconductor Industry

Regulatory agencies in numerous industrialized countries have initiated studies to quantify the use of perfluorinated chemicals, assess their potential risks, and consider regulations restricting or banning their use.

Need for Effective Treatment Methods

- In 2002, EPA finalized a Significant New Use Rule (SNUR) on 88 PFOS containing-formulations, requiring prior notice to the Agency for all manufacture/import except for specifically limited uses (eg. photomicrolithography in semiconductors).

- Excepted uses: low volume, low release, and no available substitutes.

- SNURs require notification to EPA 90 days in advance of commercialization of a chemical for a "significant new use". EPA can take action to limit or prohibit the new use.

- Need for effective methods to minimize environmental emissions of PFOS and maintain existing regulatory exemptions.

PFOS - Difficult for Treatment

Aerobic biotreatment: **Ineffective**

Sinclair & Kannan, EST, in press

Advanced oxidation treatment: **Ineffective**

O_3,O_3/UV,O_3/H_2O_2, H_2O_2/Fe^{2+} (Fenton's reagent)

Schroeder & Meester, J. Chromatog.A, 2005, 1082:110

Activated carbon: **Poor effectiveness**

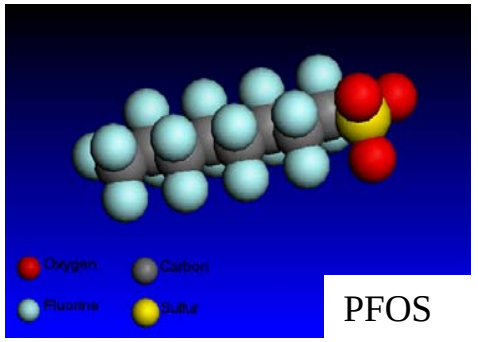
Unpublished reports

Membrane processes: **Expensive**

Disposal of concentrate!!

Properties of PFOS/PFAS

- Environmental fate and transport is poorly understood.
- Recalcitrance of fluorinated compounds:
  - Stable and chemically inert
  - High strength of C-F bond (485 KJ/mol)
  - Rigidity of perfluorinated chain
  - Absence of structures susceptible to electrophilic or nucleophilic attack.



PFOS

- PFOS does not appear to hydrolyze, photolyze or biodegrade under environmental conditions.

PFOS Research at the UofA

SRC/ERC seed project: Assessment of Physico-Chemical and Biological Methods for the Removal of PFOS in Semiconductor Effluents. (2005-2006). PI: R. Sierra[1]

NSF Small Grant for Exploratory Research: Electrochemical Degradation of Perfluorinated Compounds. (2005-2006). PIs: J. Farrell[1] and S. Raghavan[2]

SRC/ERC project: Reductive Dehalogenation of Perfluoroalkyl Surfactants in Semiconductor Effluents. PIs: R Sierra [1], N. Jacobsen [3], V. Wysocki [3]

SRC/ERC project: Destruction of Perfluoroalkyl Sulfonates in Semiconductor Effluents using Boron Doped Diamond Film Electrodes . PIs: J. Farrell [1], R. Sierra [1] , S. Raghavan [2]

[1] Dept. Chem. & Environ. Eng.; [2] Dept, Materials Science & Eng., [3] Dept. Chemistry

Objectives

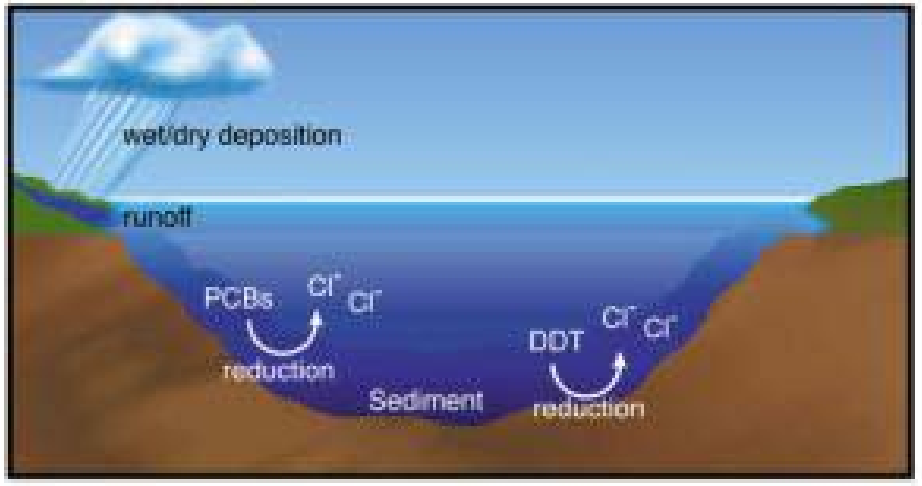
Evaluate the effectiveness of four approaches for the removal of PFOS in semiconductor effluents:

- Microbial reductive dehalogenation
- Biomimetic reductive dehalogenation
- Activated carbon adsorption
- Biosorption

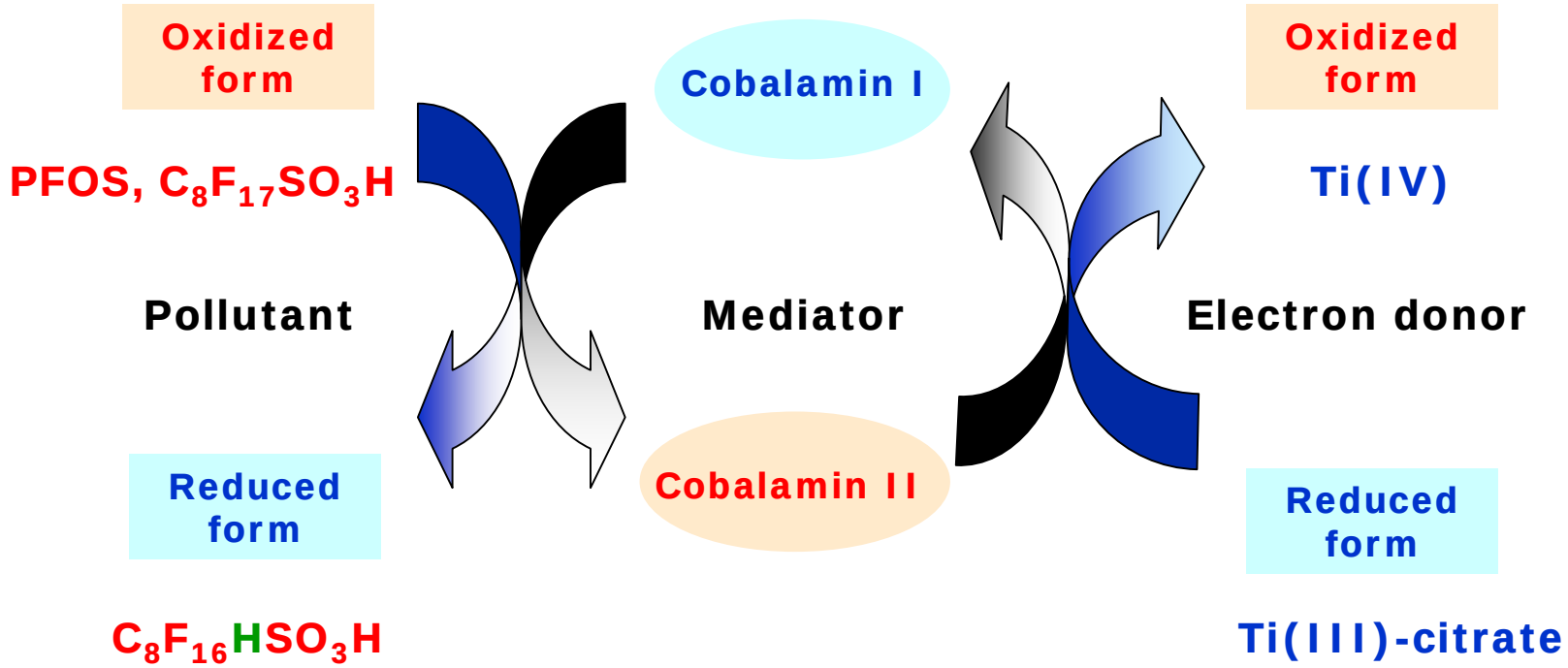
Reductive Dehalogenation

$$R\text{–}F + 2e^- + 2H^+ \text{––>} R\text{–}H + HF$$

Reductive dehalogenation is the main means of degradation of highly halogenated organics. Eg. PCE, PCBs, PBDEs.

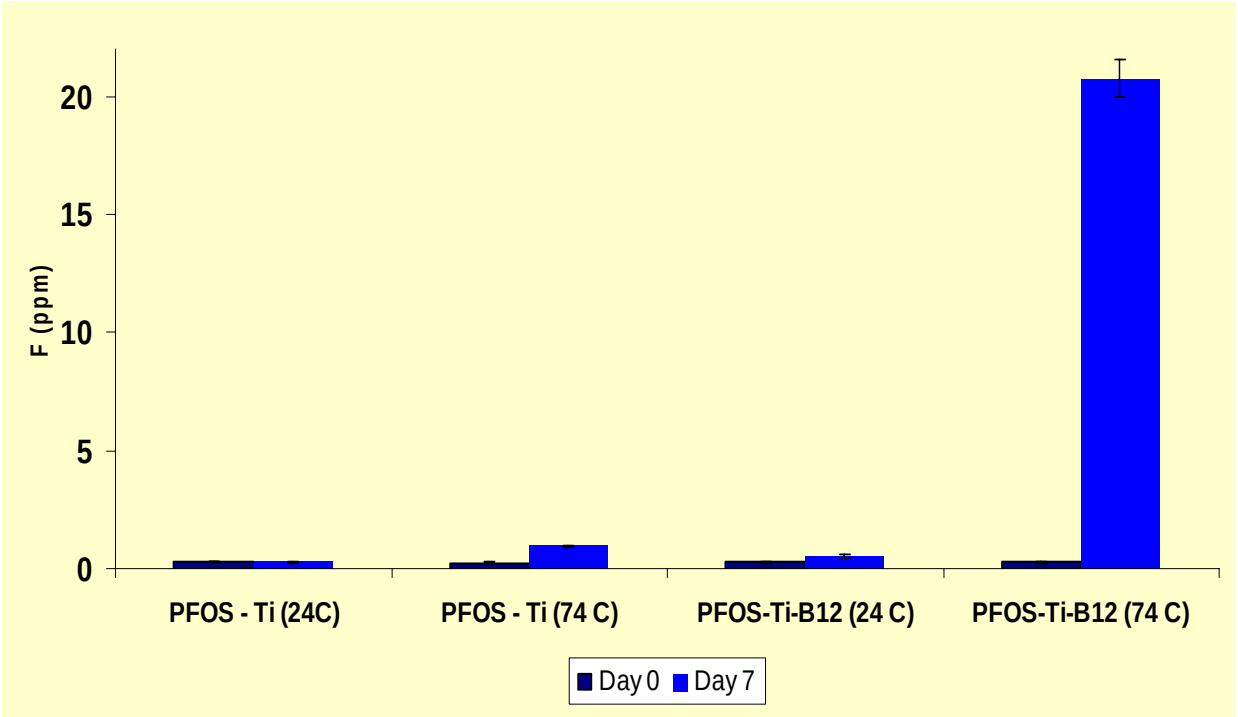


Reductive Dehalogenation



Reductive Dehalogenation:

Biomimetic Degradation with Ti(III)citrate/cobalamin



Preliminary evidence that some F atoms are removed from PFOS

Preliminary Conclusions

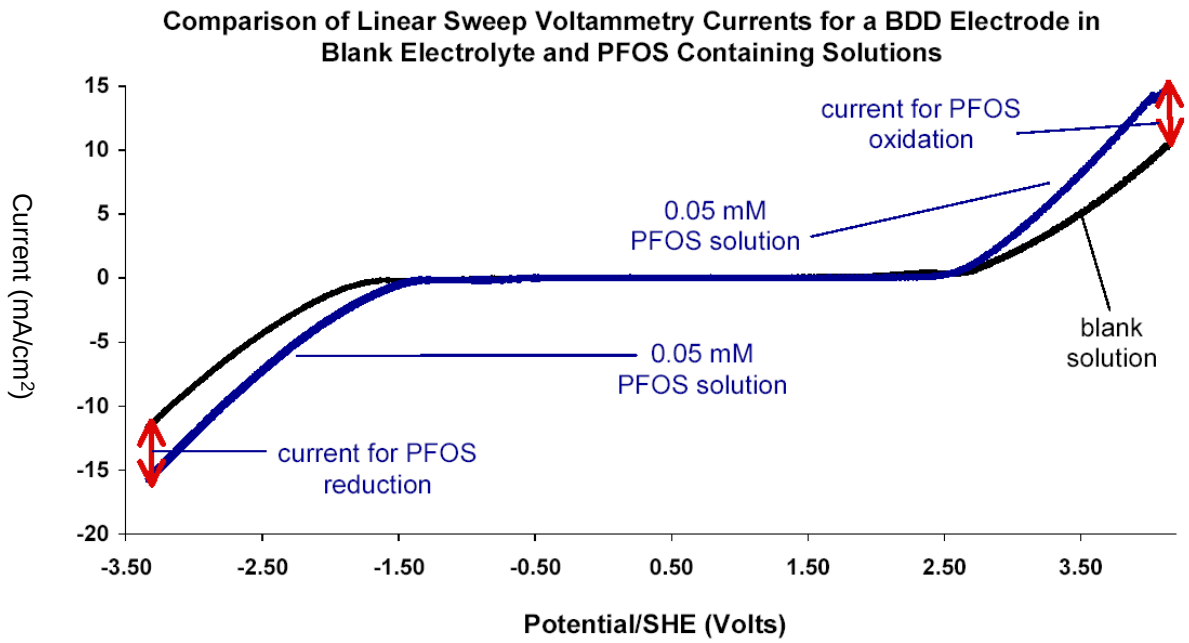
- PFOS is susceptible to biomimetic reductive dehalogenation by Ti(III) citrate/vitamin B12.
- Important implications: partially defluorinated PFOS derivatives, comparable to the products expected from reductive defluorination, are susceptible to biodegradation by aerobic bacteria.
- These findings suggest that microbial reductive defluorination of PFOS might be possible.

Objectives

Investigate a new hybrid treatment technology involving *electrochemical* and *microbial concepts* for the removal of PFOS and related perfluorinated organic compounds in semiconductor effluents.

- Determine the feasibility of electrochemical destruction of PFOS and related PFAS compounds using boron doped diamond (BDD) film electrodes.
- Determine the degree of electrolysis required to generate products that are readily biodegraded in municipal wastewater treatment plants.
- Develop an adsorptive method using hydrophobic zeolites and/or anion exchange resins for concentrating PFAS compounds from dilute aqueous solutions.

Preliminary Results



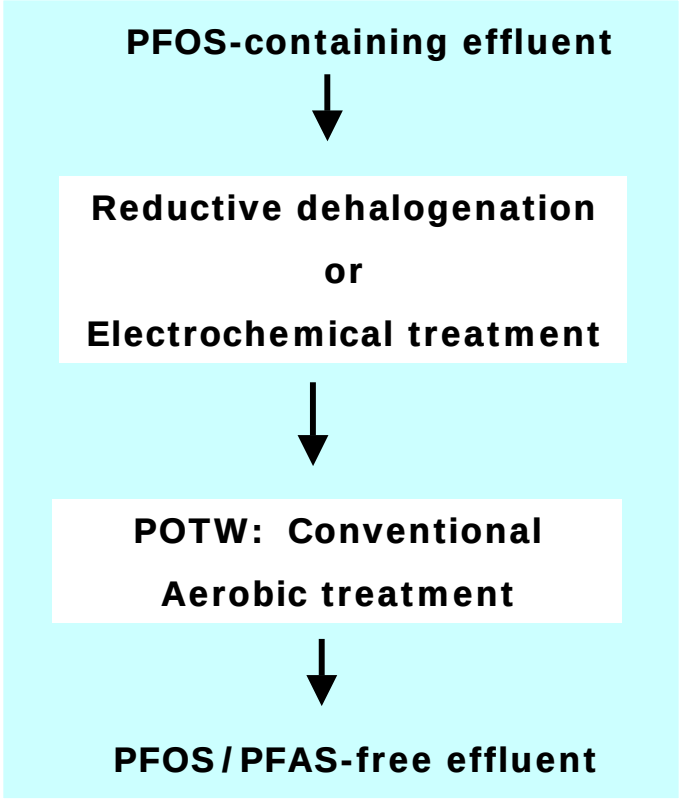
PFOS can be both oxidized and reduced at Boron Doped Diamond (BDD) film electrodes

Oxidation and reduction of PFOS releases fluoride ions

EHS Benefits

- Both reductive dehalogenation and electrochemical treatment of perfluorinated compounds are expected to lead to products amenable to biodegradation, which can be removed effectively in existing biological treatment infrastructure (eg. municipal wastewater treatment plants).

- Compound mineralization is advantageous over alternative techniques (e.g. adsorption, membrane processes, ion exchange) which generate residuals and brines.



Industrial Liaisons

Walter Worth:	Sematech
Thomas P. Diamond:	IBM
Jim Jewett:	Intel
Laura Mendicino:	Freescale Semiconductor
Tim Yeakley:	Texas Instruments

Lowering Resource Utilization During Cleaning, Rinsing, and Drying

Real-Time and In-Situ Detection of Residual Contaminants in Micro- and Nano- Structures

Subtask C-2-1

Jun Yan[1] , Kedar Dhane[1]
Bert Vermeire[2] and Farhang Shadman[1]

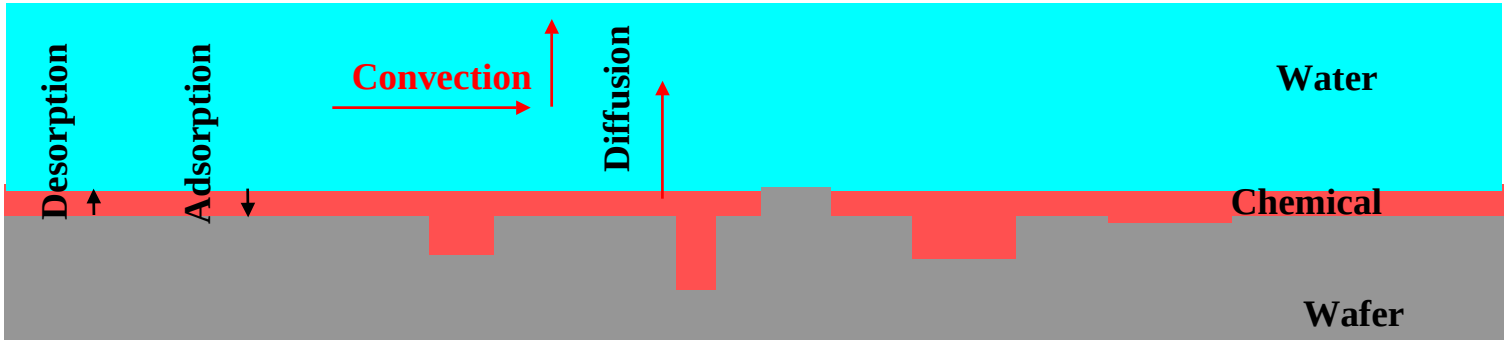
[1]Chemical and Environmental Engineering, UA
Electrical Engineering, ASU

Joint work with Freescale on Fab-scale experiments

NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

Objectives

- **Develop efficient cleaning, rinsing, and drying techniques; important to reduce: resource utilization, waste, processing time, and cost.**



Method of Approach

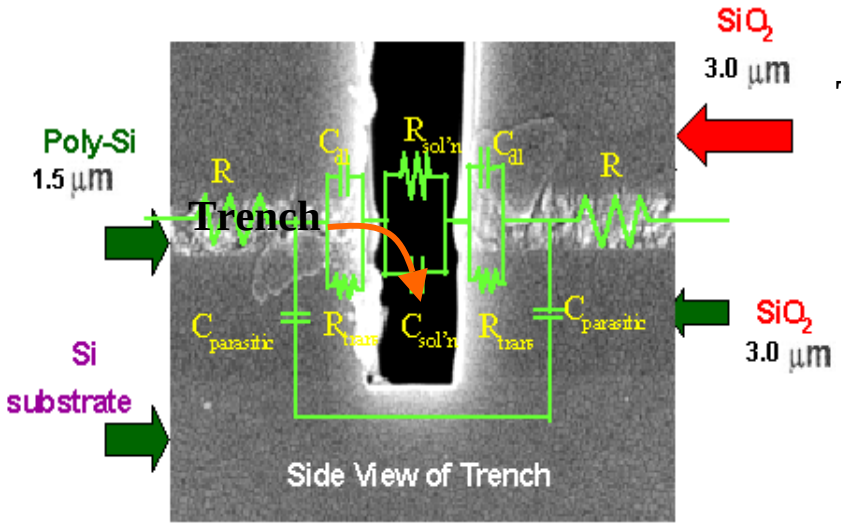
- **Understand the fundamentals of residual impurity removal from wafer surface and from inside micro- and nano- features**
- **Needed tool: on-line and real-time metrology technology for both research and Fab-level applications**

Fundamental Steps in Rinse Process

Factors	Bulk	Boundary Layer	Surface	Channels*
Primary Mechanism	convection	diffusion	desorption	diffusion/ desorption
Secondary Mechanism	dispersion	convection	multi-component displacement	desorption/ diffusion
Characteristic Time	L/U	d^2/D	$1/k_d$	$I/k_d + (cd)^2/D_{eff}$
Process Time Scale (sec)	1 - 3	10 - 60	10^{-1} - 10^5	1 - 10^6
Effect of Flow	direct, strong	indirect, mild	no effect	no effect
Effect of Temperature	negligible	mild	strong	mild
Effect of Additives	no effect	no direct effect	potentially strong effect	potentially strong effect

* Width <10 micron, aspect ratio>4

Electro-Chemical Residue Sensor (ECRS)



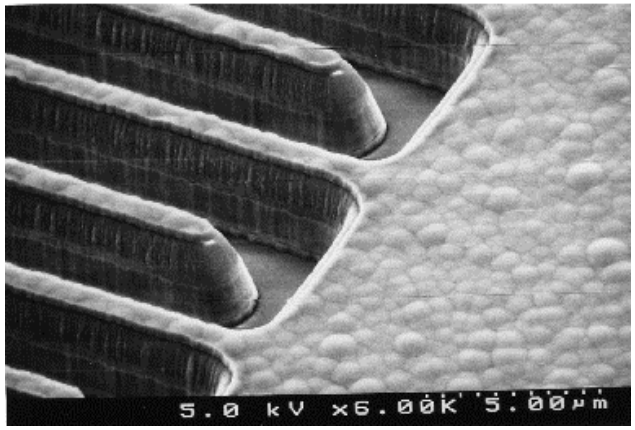
Trench solution impedance

measured trench interface impedance

$$Z_{trench} = \frac{1}{\frac{1}{Z_{total} - 2 \times Z_1} - \frac{1}{Z_3}} - 2 \times Z_2$$

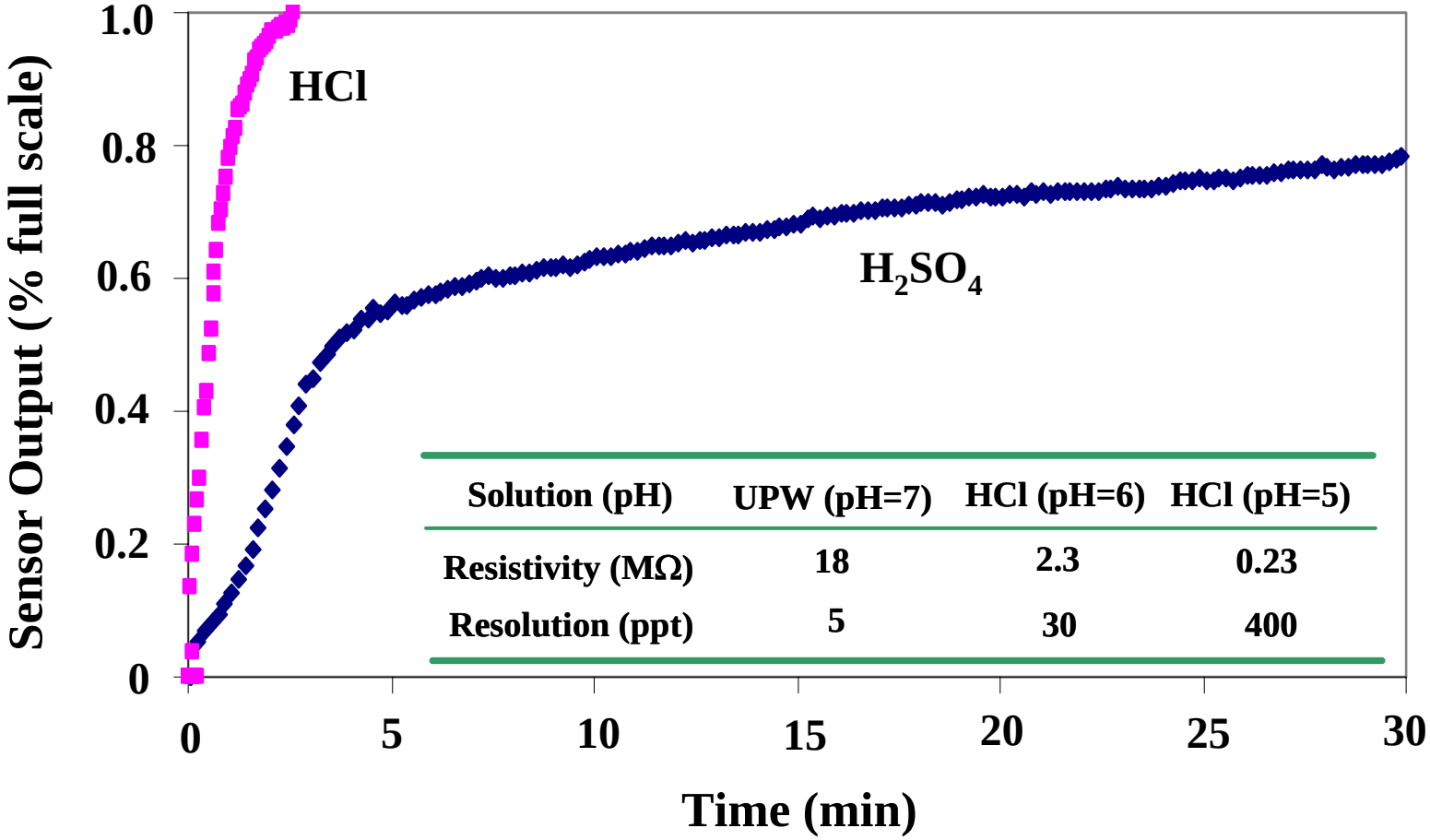
measured with impedance analyzer

calculated from material properties



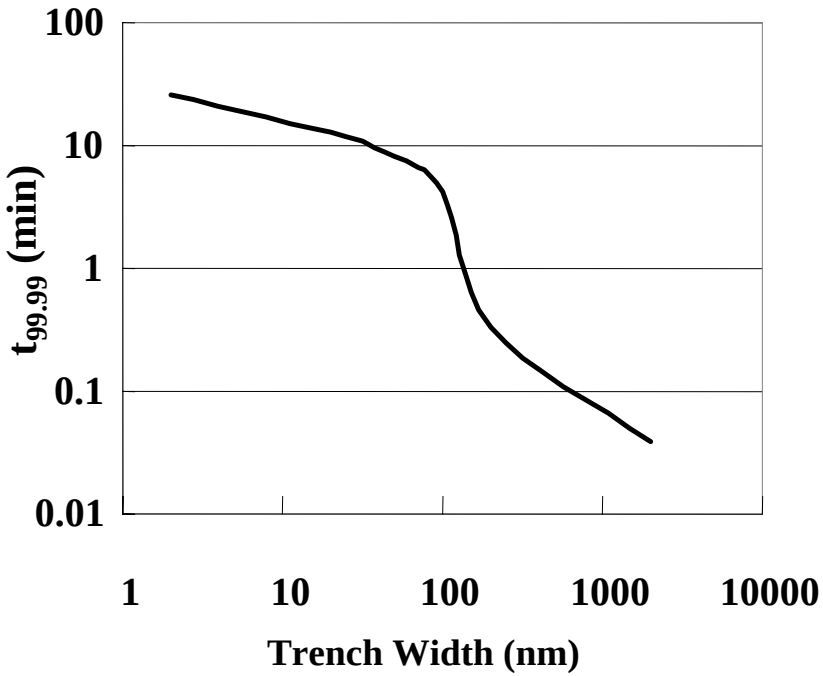
Z_{trench} is related to the impurity concentration in the trench during rinsing and drying.

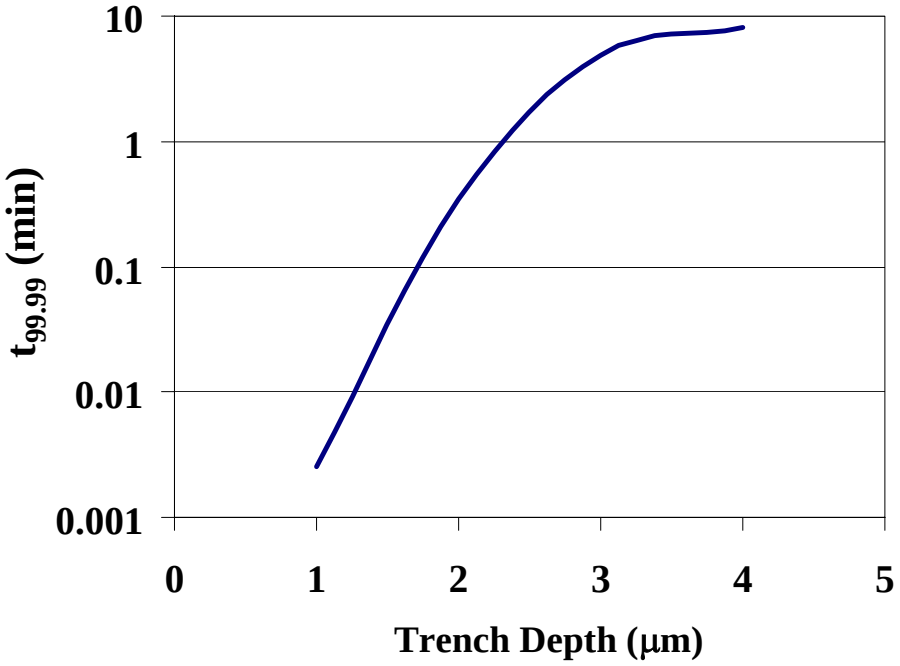
ECRS Sensitivity to Impurity Concentration and Type



Solution (pH)	UPW (pH=7)	HCl (pH=6)	HCl (pH=5)
Resistivity (MΩ)	18	2.3	0.23
Resolution (ppt)	5	30	400

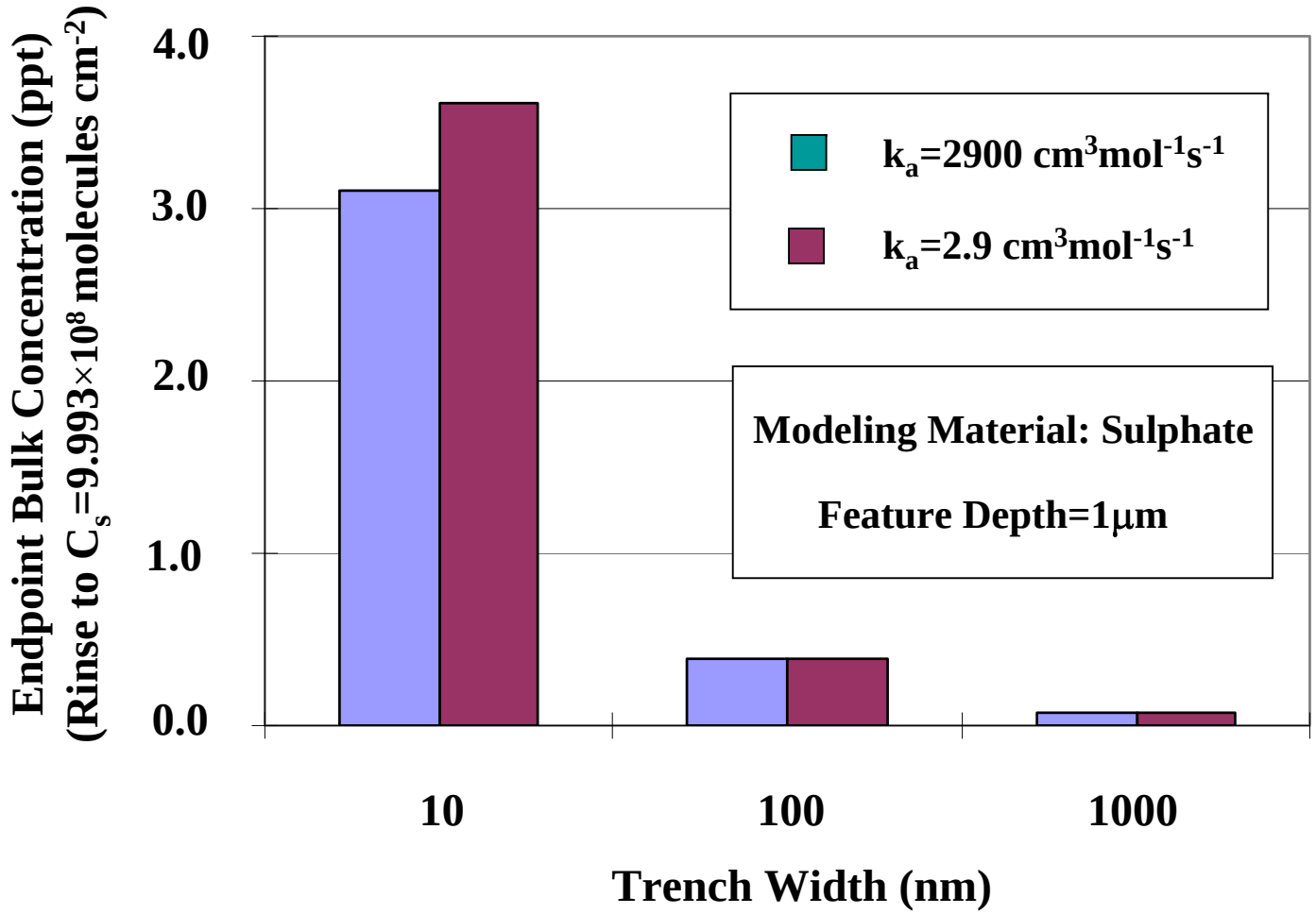
Dependence of Cleaning Dynamics on Feature Size



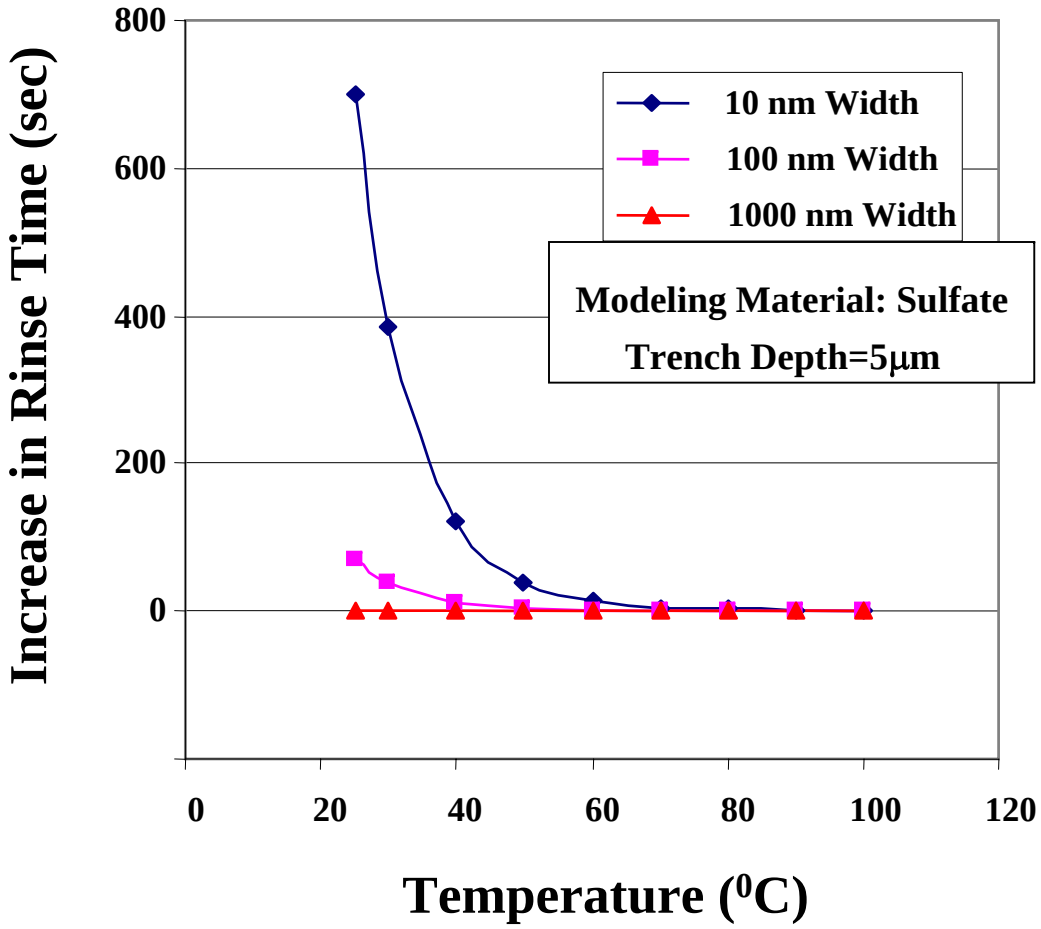


$t_{99.99}$ is the time needed for 99.99% clean up of residual sulfate ion

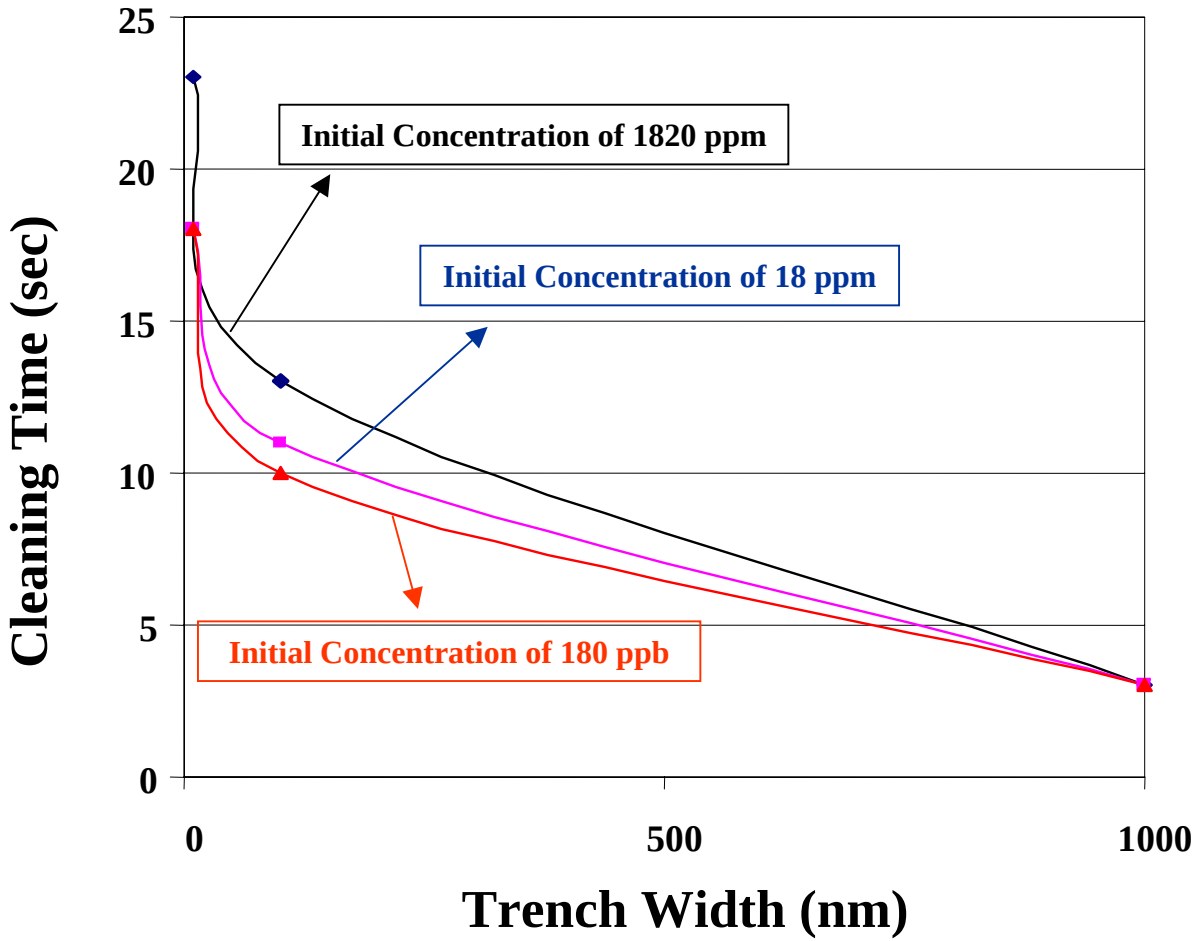
Effect of Feature Size on End-Point Contamination



Effect of Temperature and Feature Size on Required Rinse Time

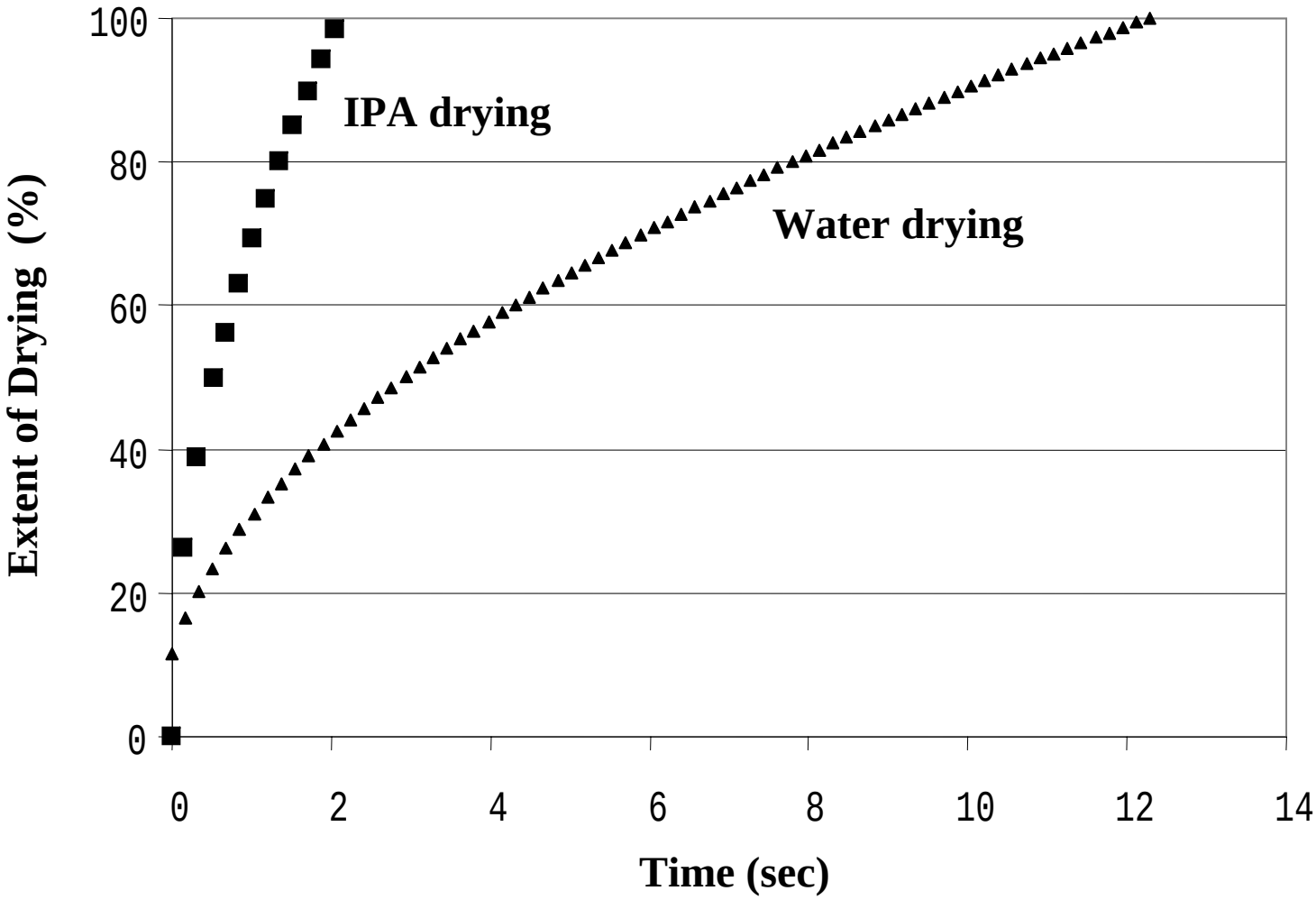


Effect of Feature Size on High-Temperature Cleaning Time

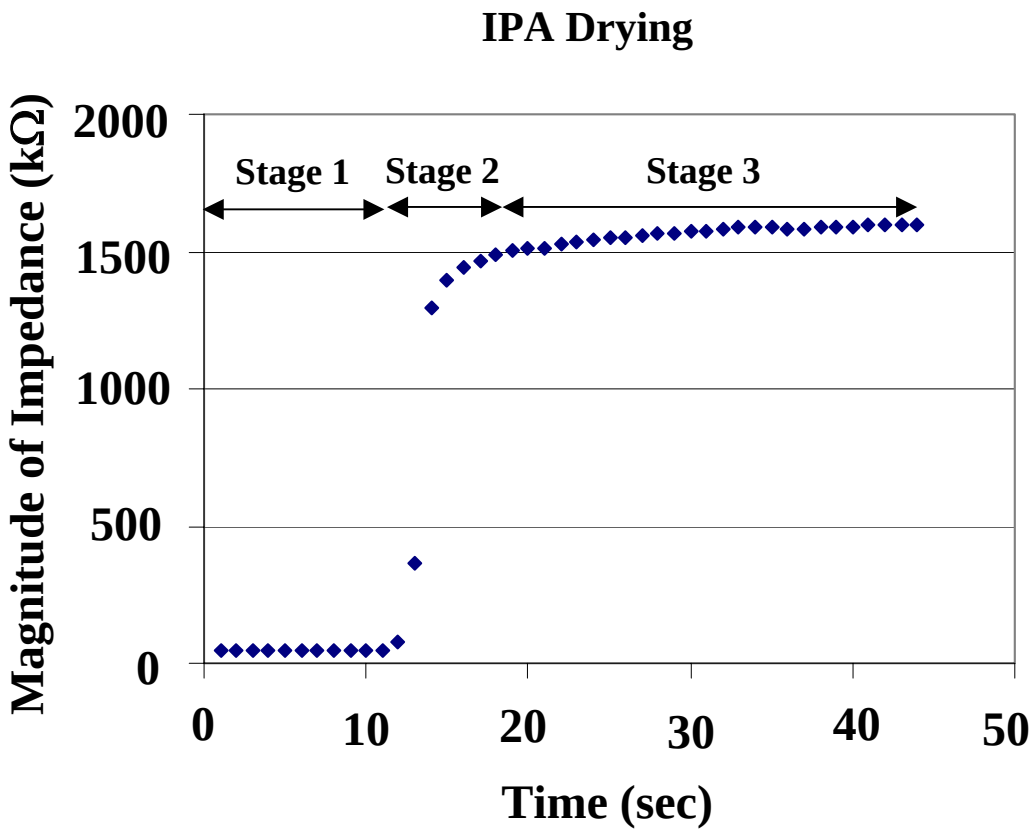


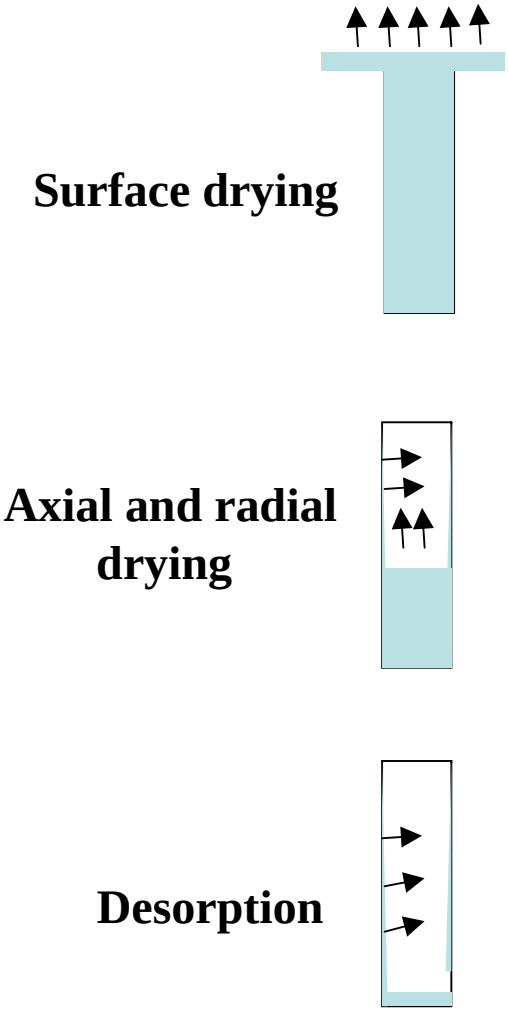
Cleaning time is to achieve surface concentration 9.993×10^8 molecules/cm^2
Contaminant: residual sulfate ion; trench depth: 5μm

Sensor Response to Drying Processes

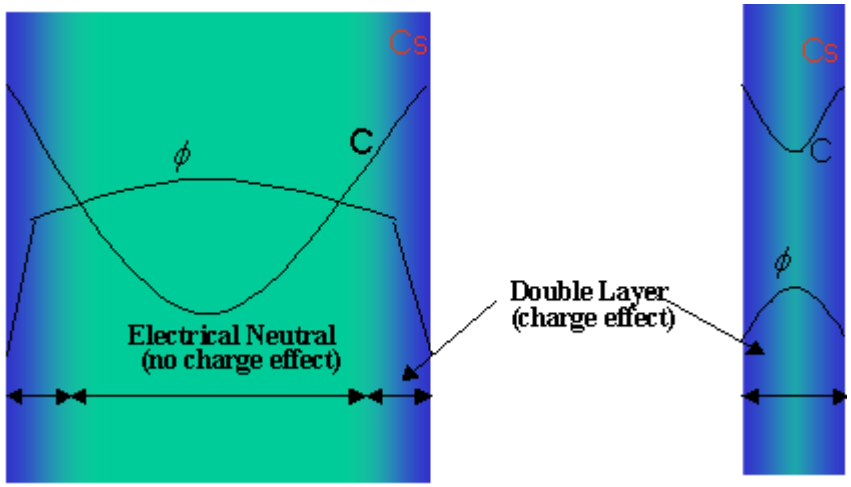


Sensor Reveals Drying Mechanism





Electrostatic Interactions



Mass Balance equations:

$$\frac{dC}{dt} = \nabla \cdot (D_{AB} \cdot \nabla C + z \cdot \lambda \cdot F \cdot C \cdot \nabla \phi)$$

$$\frac{\partial C_S}{\partial t} = \left[k_a C(S_0 - C_S) - k_d C_s \right]$$

$$\nabla^2 \phi = -\frac{\rho_e}{\varepsilon\varepsilon_0} = -(\rho_\infty e / \varepsilon\varepsilon_0) * \exp(-z * e * \phi / (k * T))$$

The electrostatic interactions become more significant as feature size decreases and purity requirements increase.

Lowering Resource Utilization During Cleaning, Rinsing, and Drying

Drying of Thin Porous Films and Micro- and Nano-Structures

Subtask C-2-5

Junpin Yao, Asad Iqbal, Harpreet Juneja, and Farhang Shadman

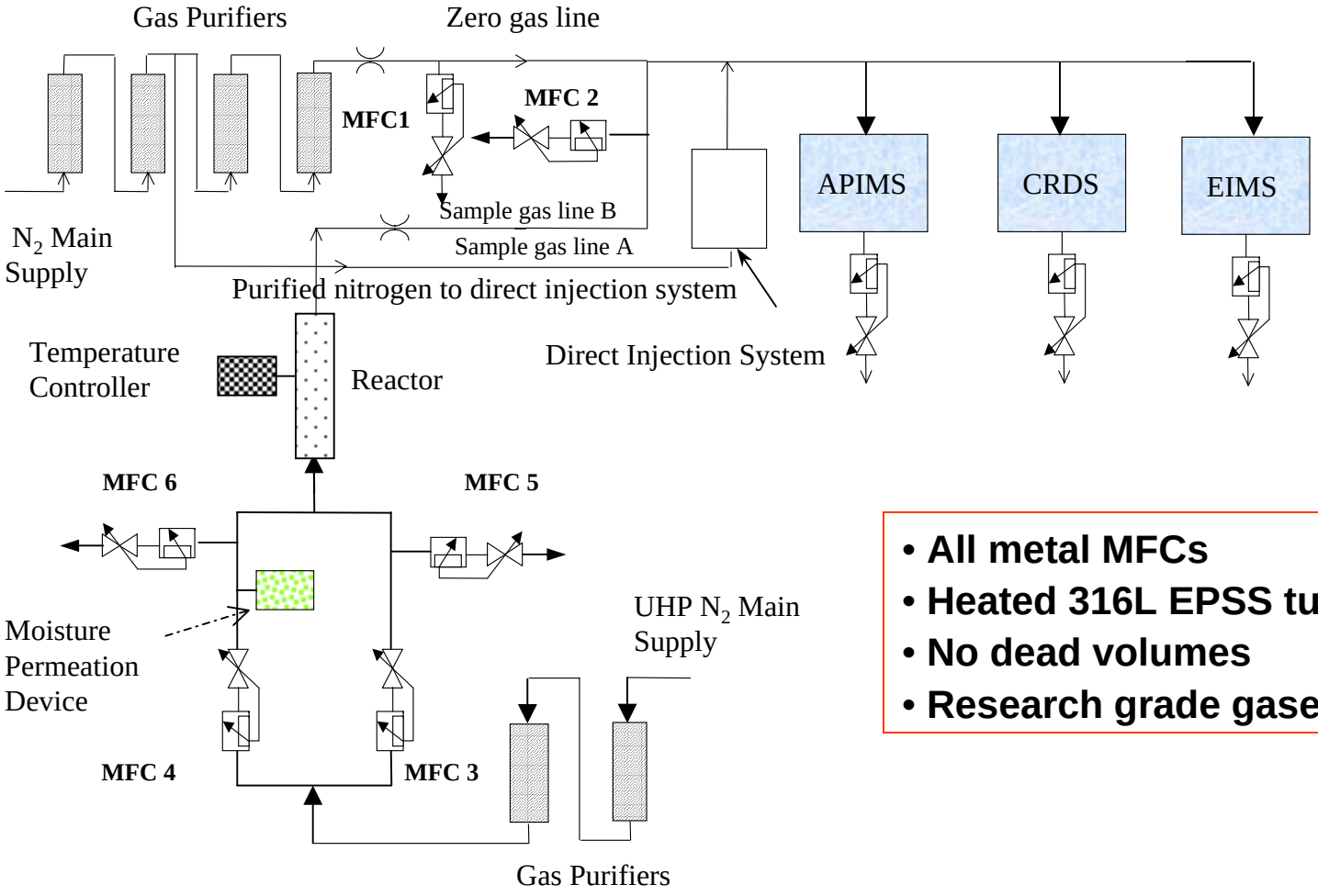
Department of Chemical and Environmental Engineering

University of Arizona

Jointly with Sematech Interconnect Group

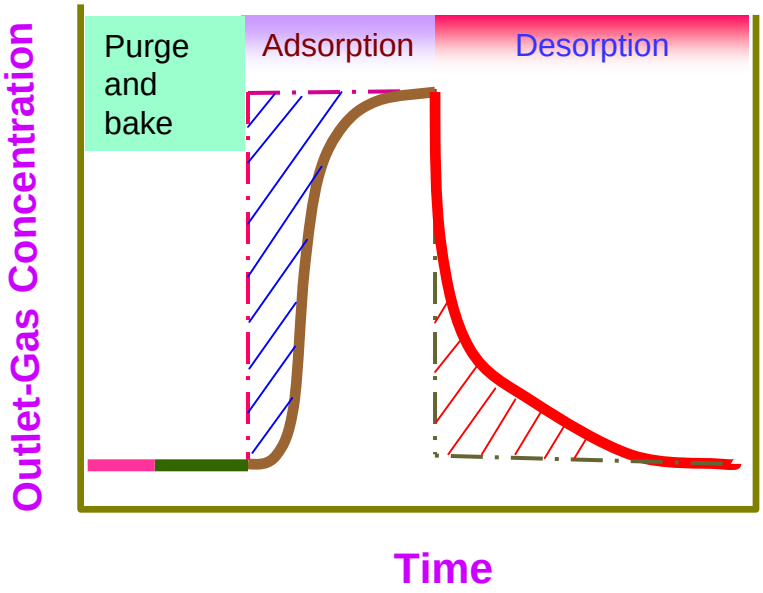
NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

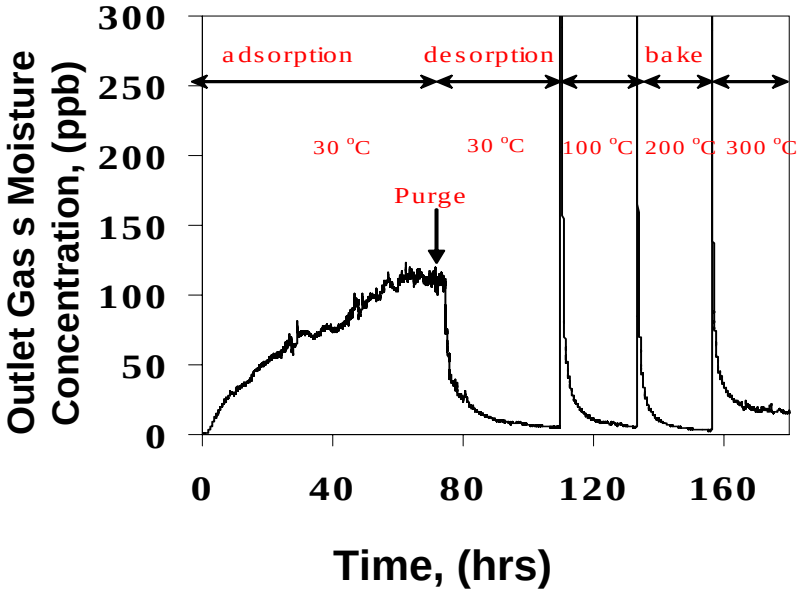
Experimental Setup



- **All metal MFCs**
- **Heated 316L EPSS tubing**
- **No dead volumes**
- **Research grade gases**

Experimental Procedure





Experimental procedure

Adsorption at 30°C

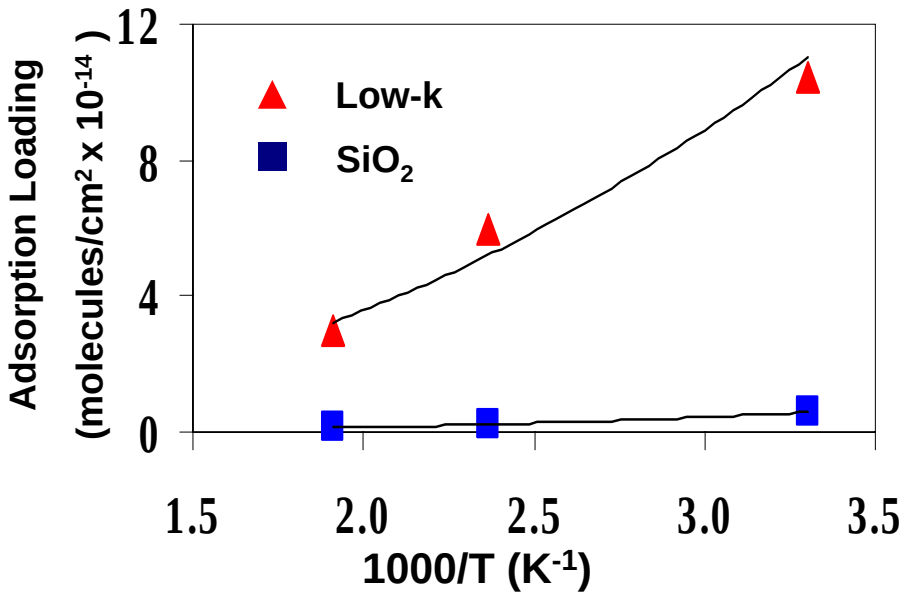
Desorption at 30°C

Bake-out at 100, 200 & 300°C

Temporal profile of adsorption (challenge 110 ppb moisture), followed by temperature-programmed desorption as measured by mass spectrometer

Moisture Adsorption Loading

Challenge Concentration : 56 ppb



- **Low-k has much higher sorption loading than SiO_2**

SiO_2

Δ Electronegativity	1.7
-OH site density (#/cm²)	4.6 x 10^{14}

p-MSQ

$$C_{film0} = C_{gp0}\varepsilon + C_{s0}(1-\varepsilon)$$

$$C_{s0} = C_{gb0} * S$$

C_{gbo} = challenge moisture concentration

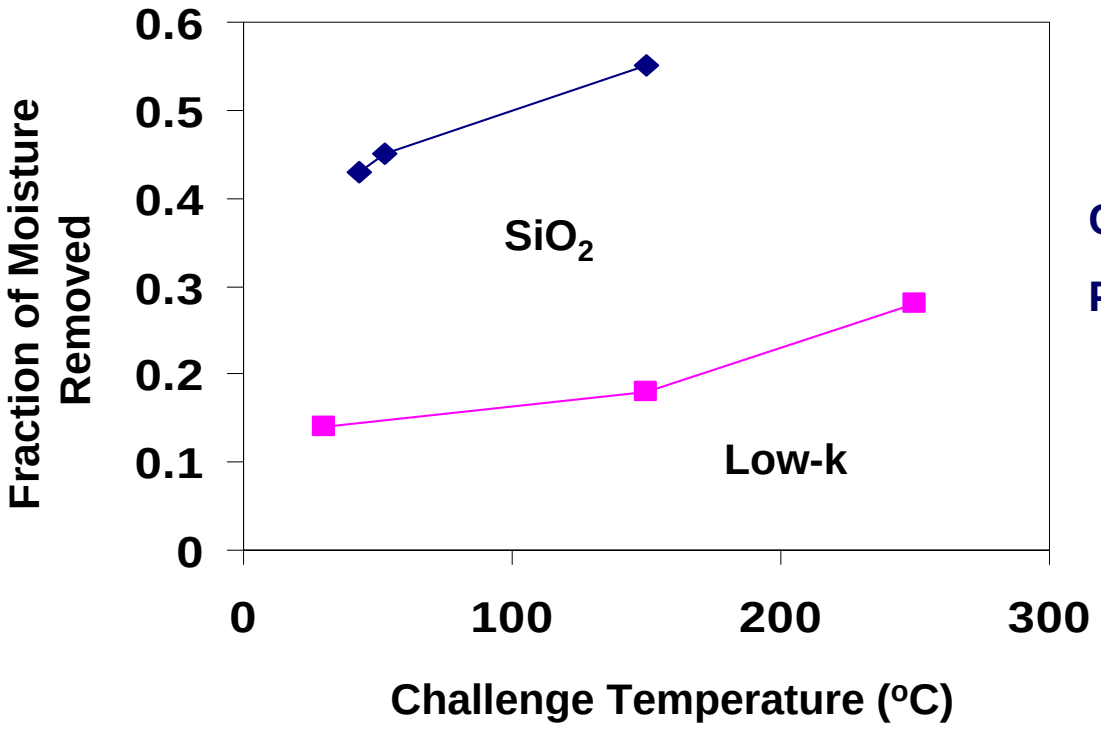
C_{gpo} = equilibrium moisture conc. in the pore

C_{so} = equilibrium moisture conc. in the matrix

C_{filmo} = total moisture loading in molecules per unit volume of the film

ε = porosity, *S* = solubility

Moisture Retention after Isothermal Purge



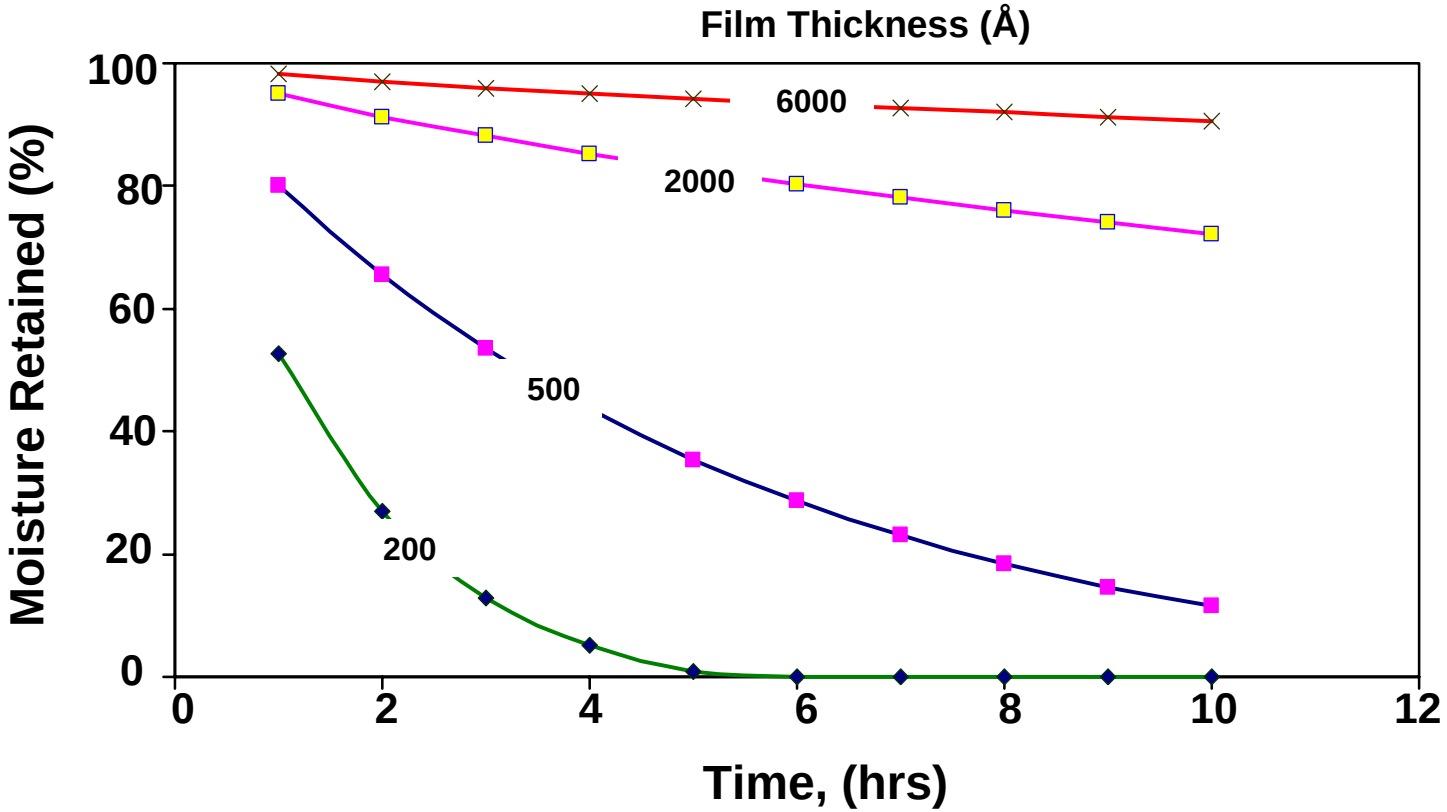
Challenge Conc: 56 ppb

Purge Time: 10 hrs

- **45-50% of adsorbed moisture removed from SiO_2 during isothermal N_2 purge**
- **Only 15-25% of absorbed moisture removed from low-k**

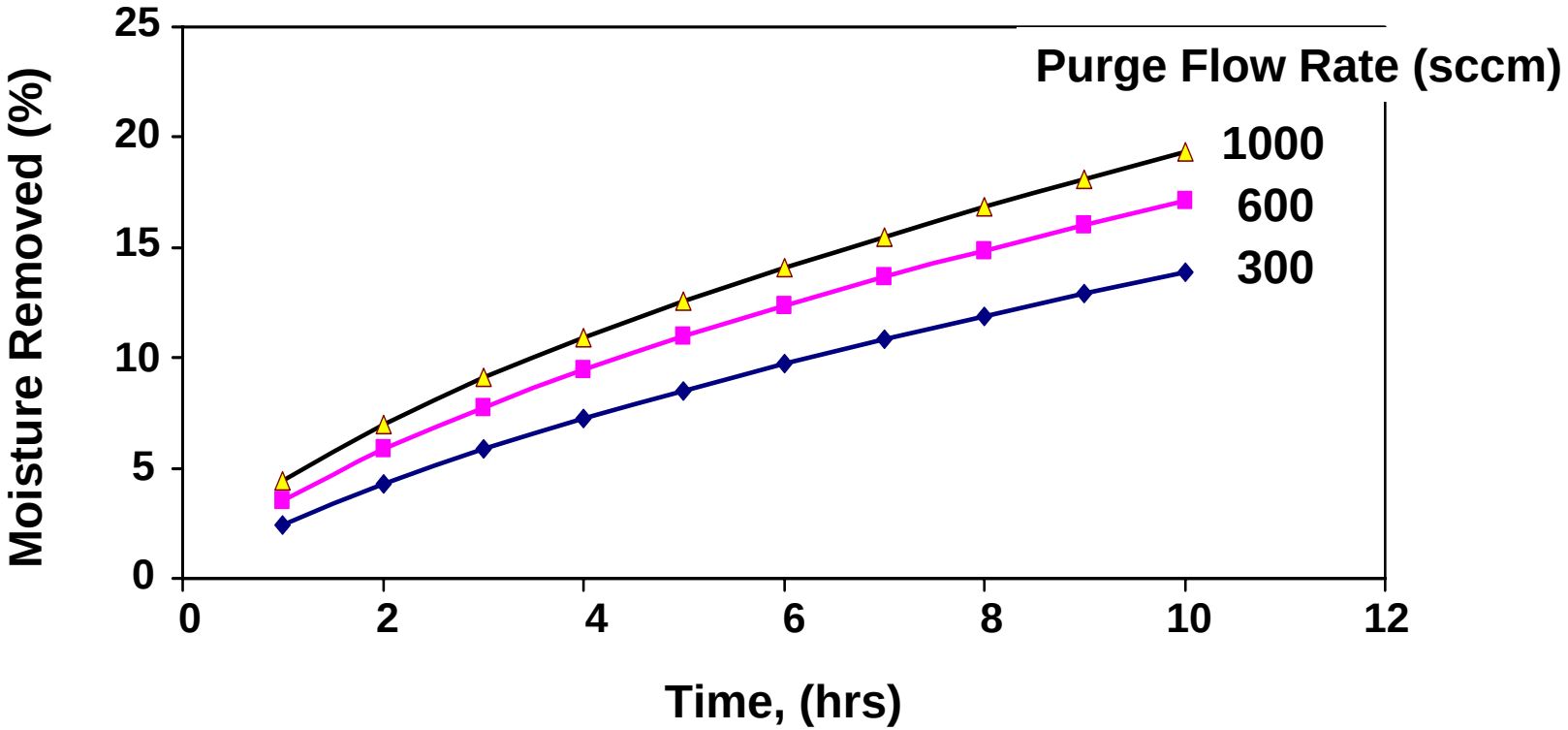
Effect of Low-k Film Thickness

Challenge Conc: 56 ppb; Temperature: 30°C; Porosity: 0.48



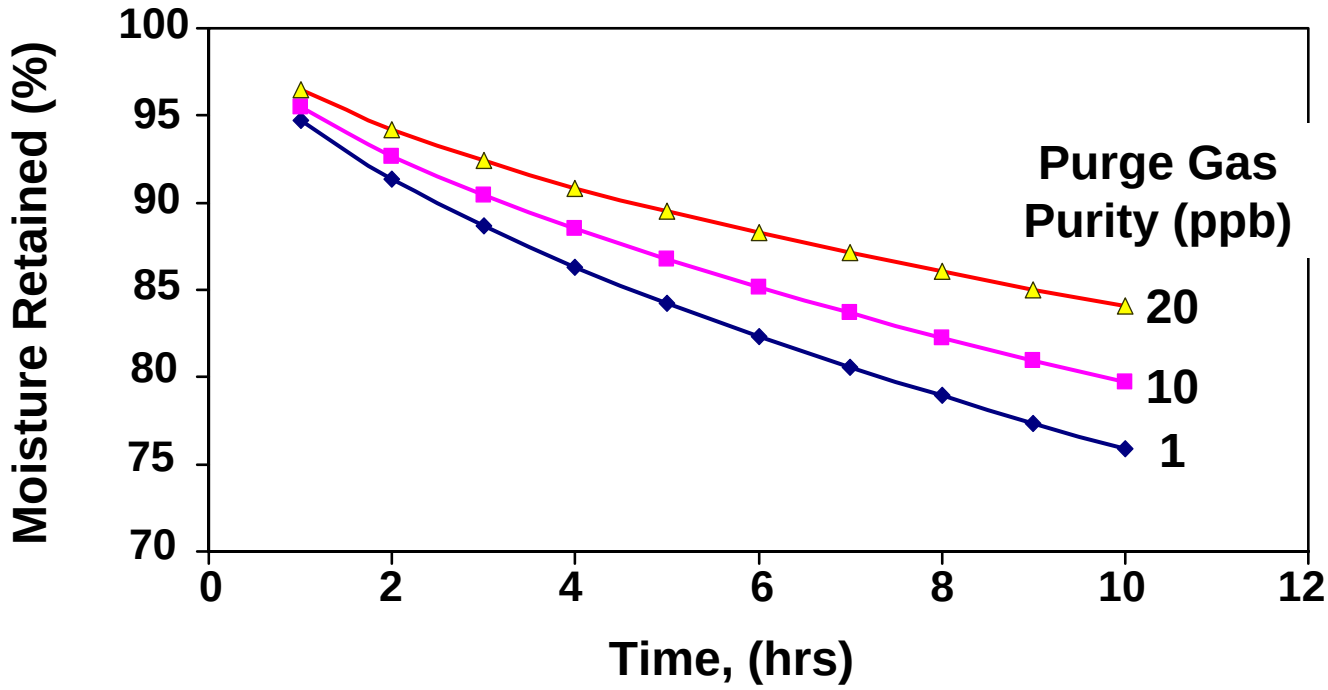
Effect of Purge Gas Flow Rate

Challenge Conc: 56 ppb; Temperature: 30°C; Porosity: 0.48



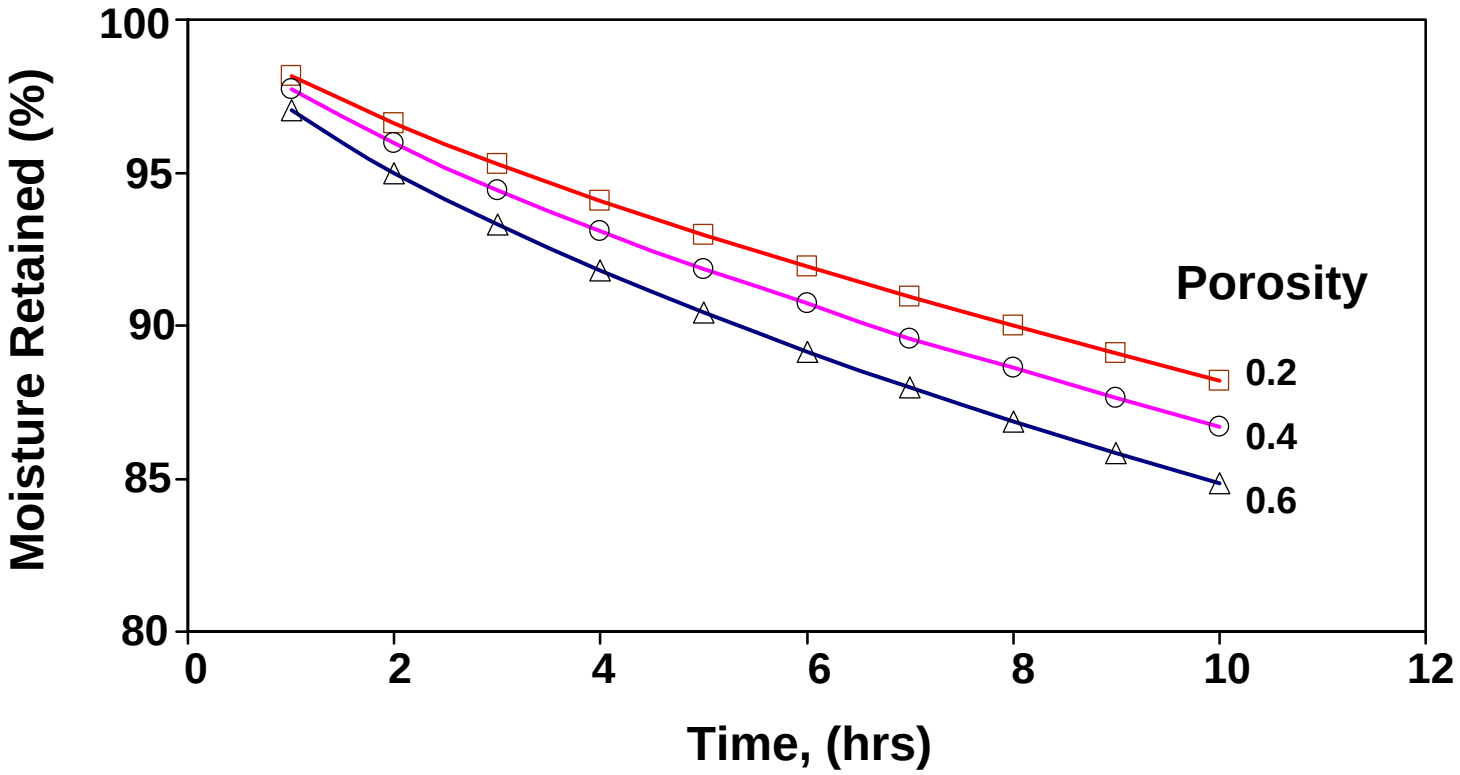
Effect of Purge Gas Purity

Challenge Conc: 56 ppb; Temperature: 250°C; Porosity: 0.48



Effect of Low-k Film Porosity

Challenge Concentration : 56ppb; Temperature : 30°C



Acknowledgement

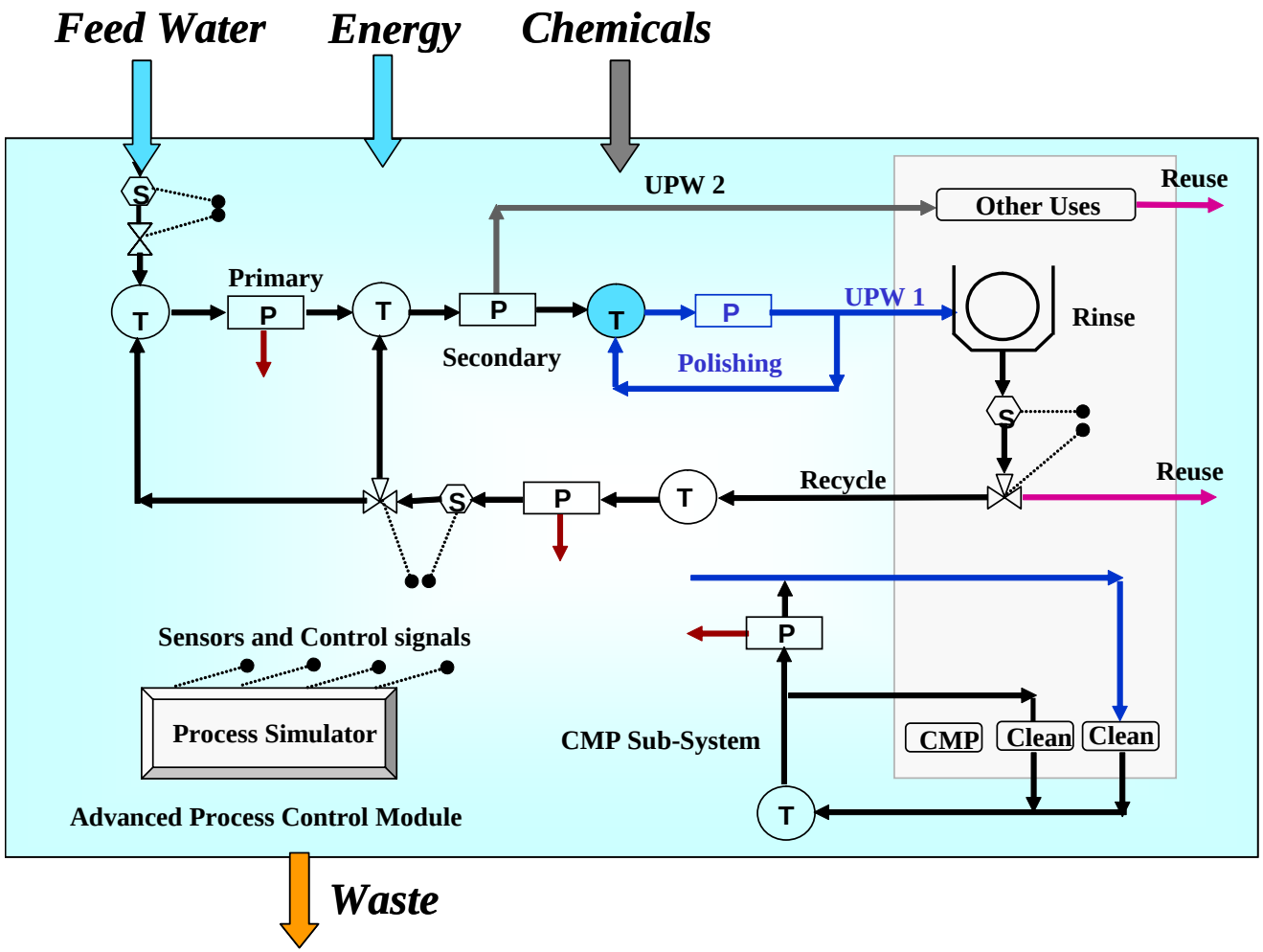
- **SEMATECH: providing samples**
- **Freescale: joint work on testing the ECRS in a commercial rinse tool.**
- **American Semiconductor: assistance in fabrication**
- **On Semiconductor: joint work on testing test the ECRS in a commercial drying tool.**
- **Environmental Metrology Corporation (start-up): joint work for commercialization**

Highlights of

Other Thrust C Projects

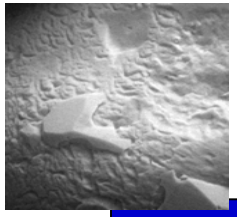
Process Simulators and Test Beds for Water Recycling

Blowers, Ela, Shadman (UA)



Bio-Treatment of Waste Containing Organics and Copper

Field, Ogden, Sierra (UA)



Effluent recycle

Fab Wastewater

$SO_4^=$

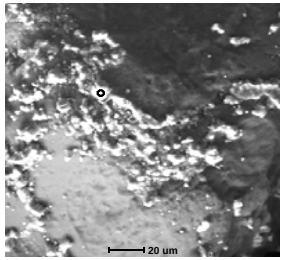
Heavy metals

Organics

Crystallization Reactor

Sulfidogenic Bioreactor

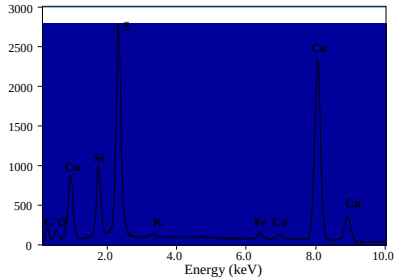
Treated Wastewater



Metal Sulfides

Sulfate reduction

Removal of organics



SO_4^{2-} + Organics → HS^- + CO_2

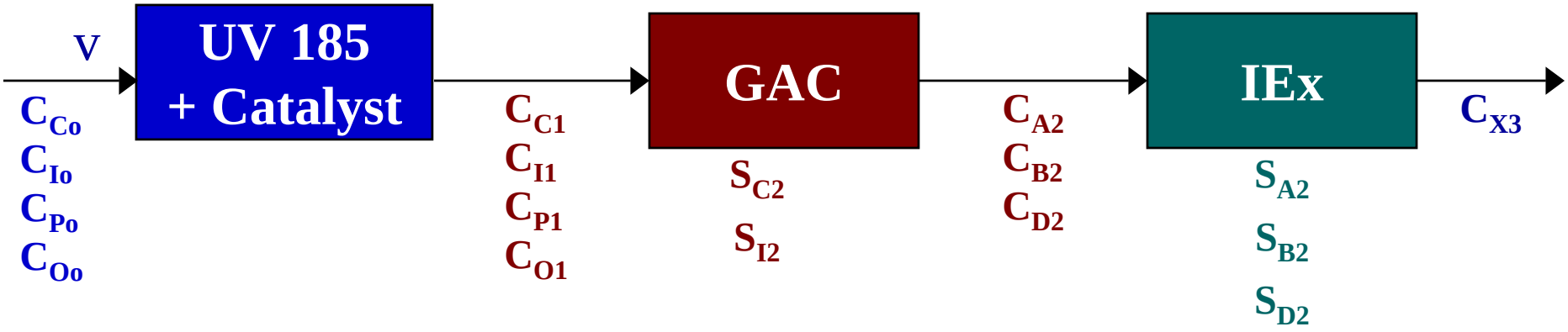
(Electron donor)

$S^=$ + M^{2+} → MS ↓

Metal Sulfide

Low-Energy Hybrid Purification of Water

Shadman (UA)

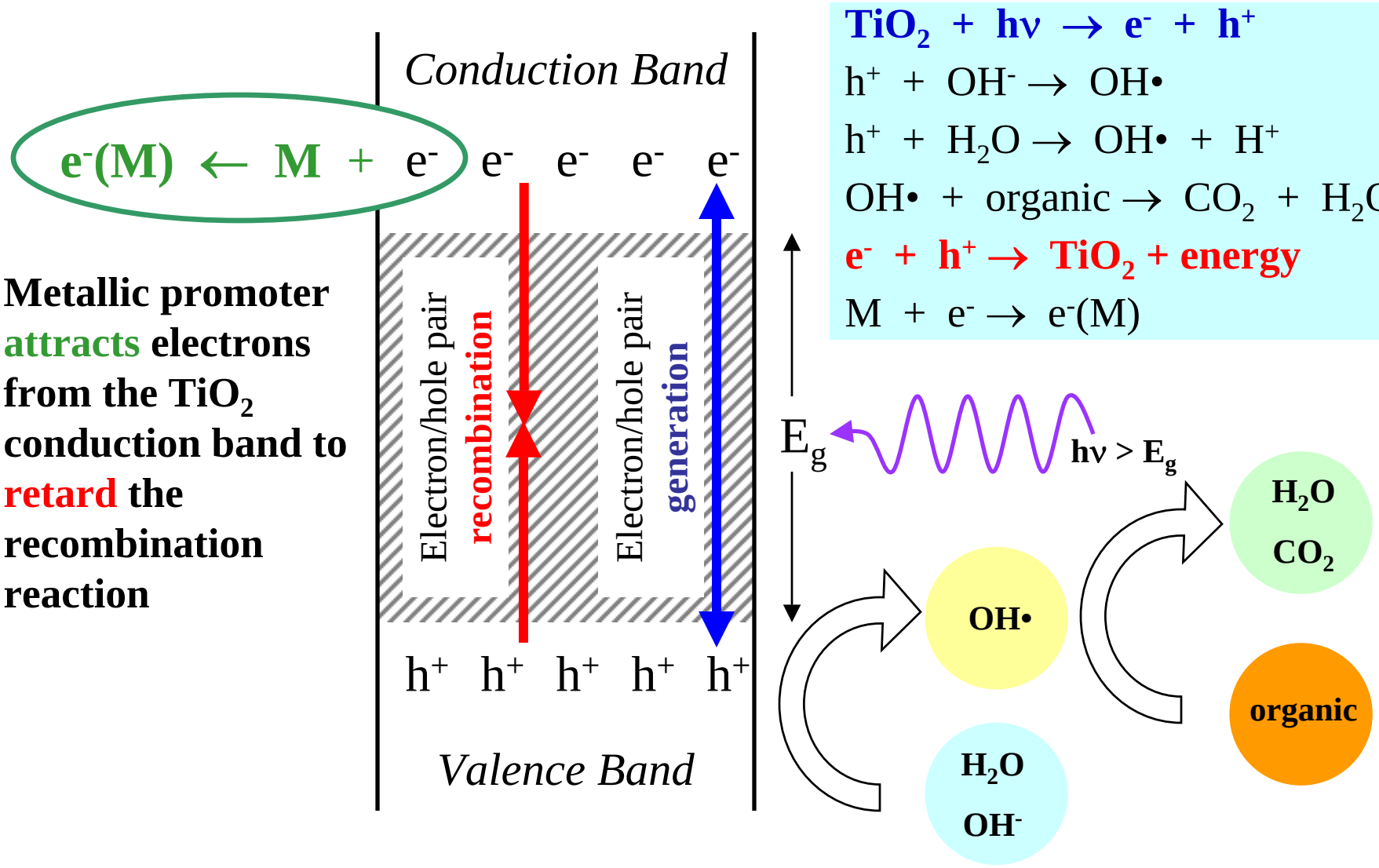


$$H_2O + h\nu \xrightarrow{k_1} O$$
$$C + h\nu \xrightarrow{k_2} I$$
$$C + O \xrightarrow{k_3} I$$
$$I + O \xrightarrow{k_4} P$$

$$C + X_{GAC} \xleftrightarrow{k_{aC_2}, k_{dC_2}} C.X_{GAC}$$
$$I + X_{GAC} \xleftrightarrow{k_{aI_2}, k_{dI_2}} I.X_{GAC}$$
$$C.X_{GAC} + O \xrightarrow{k_5} P$$
$$I.X_{GAC} + O \xrightarrow{k_6} P$$
$$C + O \xrightarrow{k_7} I$$
$$I + O \xrightarrow{k_8} P$$
$$O + GAC \xrightarrow{k_9} \text{Products}$$

$$A + B.X \xleftrightarrow{k_{10}, k_{-10}} A.X + B$$
$$A.X + D \xleftrightarrow{k_{11}, k_{-11}} A.X.D$$
$$B.X + D \xleftrightarrow{k_{12}, k_{-12}} B.X.D$$
$$D + Y \xrightarrow{k_{13}} D \bullet Y$$

Role of Promoters in TiO_2 Catalytic Oxidation



Metallic promoter attracts electrons from the TiO_2 conduction band to retard the recombination reaction

$TiO_2 + h\nu \rightarrow e^- + h^+$

$h^+ + OH^- \rightarrow OH\bullet$

$h^+ + H_2O \rightarrow OH\bullet + H^+$

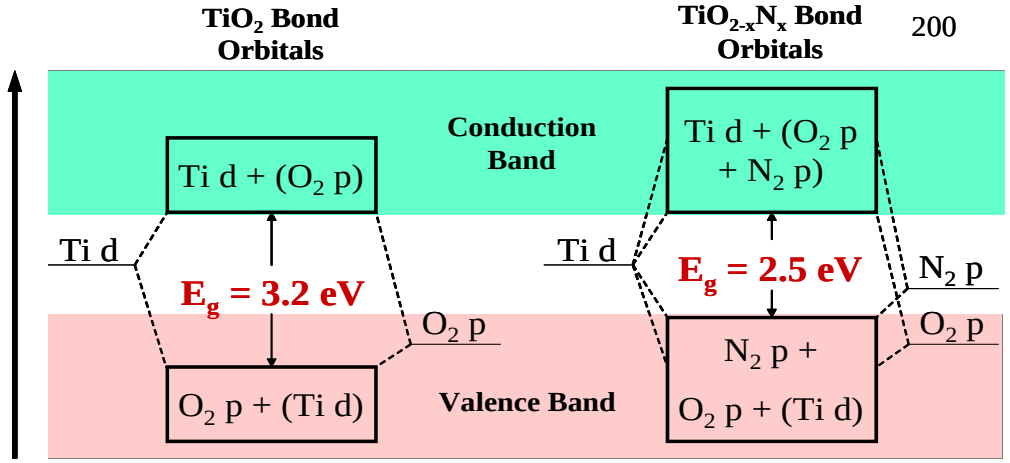
$OH\bullet + \text{organic} \rightarrow CO_2 + H_2O$

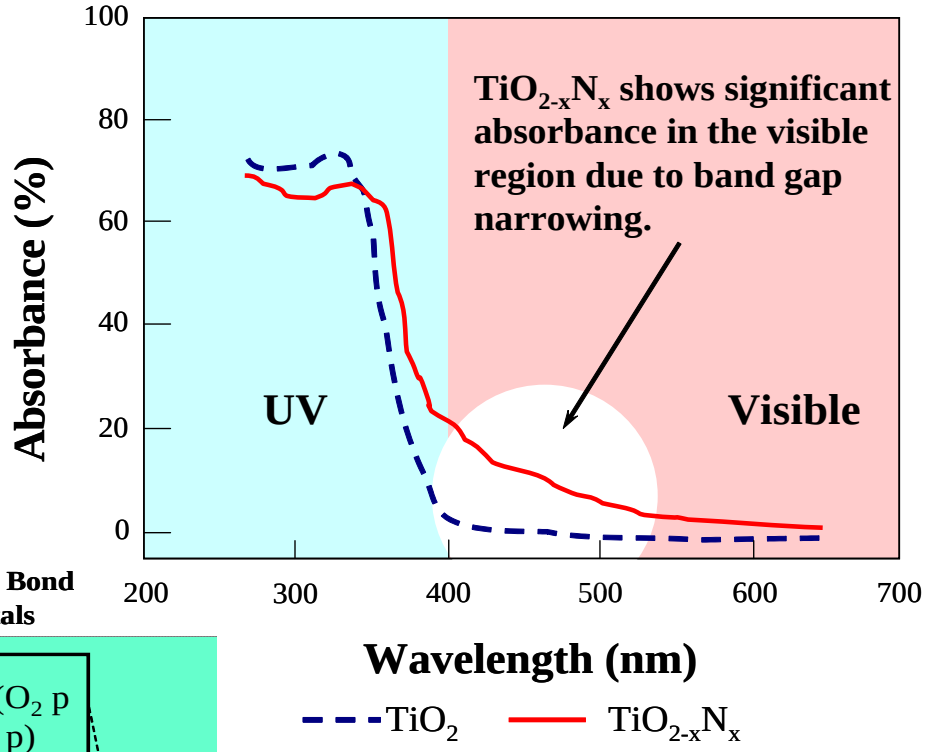
$e^- + h^+ \rightarrow TiO_2 + \text{energy}$

$M + e^- \rightarrow e^-(M)$

Search for Improved Promoters in TiO_2 Catalytic Oxidation

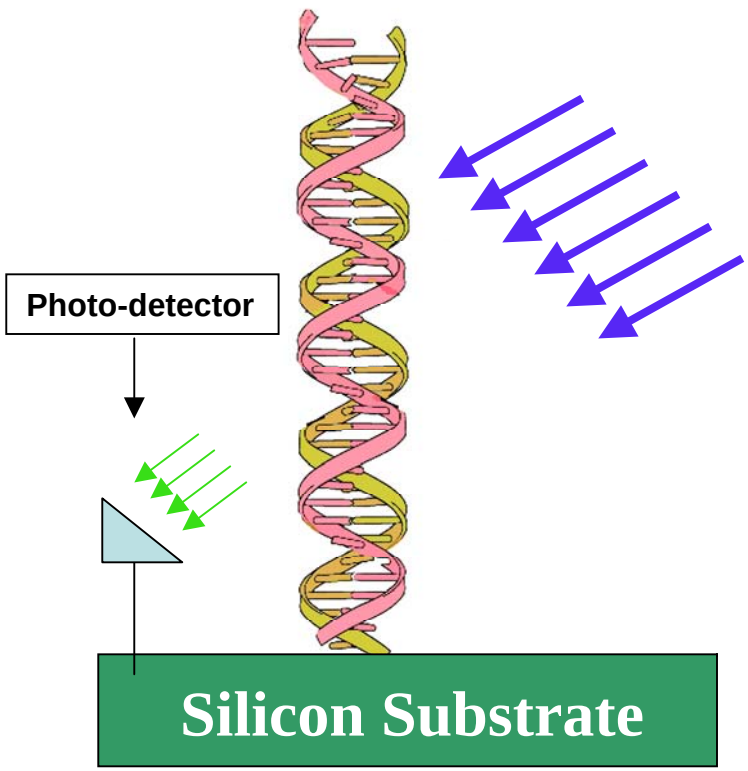
Addition of nitrogen decreases the energy band gap, thus increasing the electron-hole generation and UV utilization efficiency.



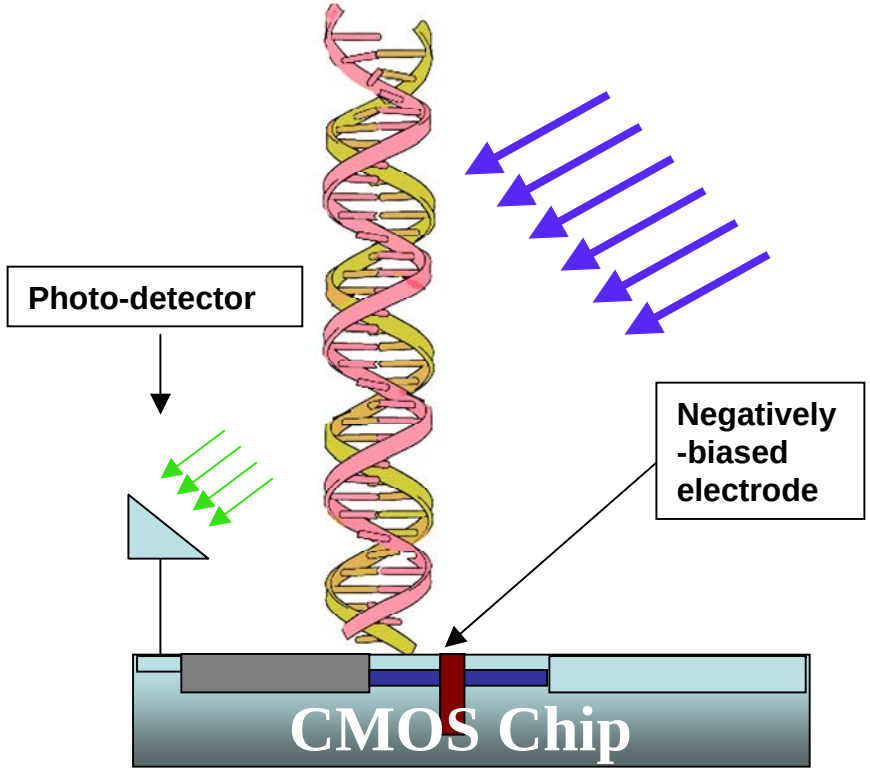


CMOS-Based Micro-Arrays for Rapid Assessment of Chemical Toxicity

Mathine, Runyan (UA, NIEH Centers)



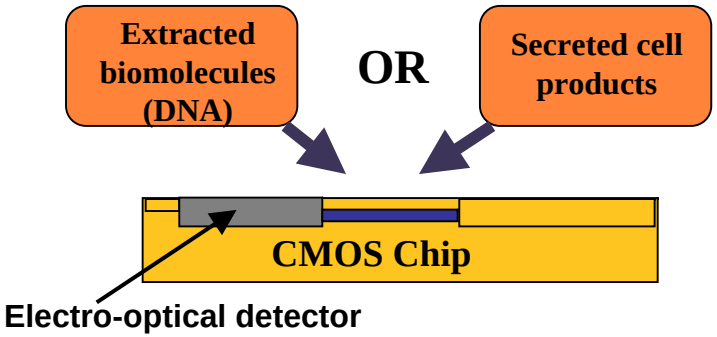
Current Technology

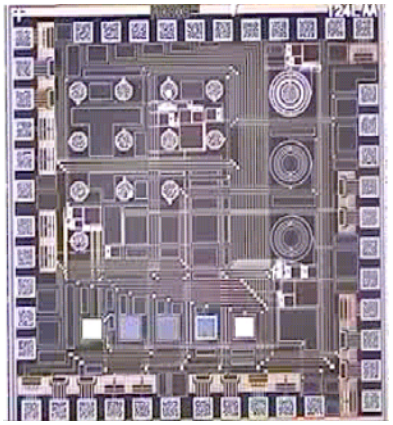


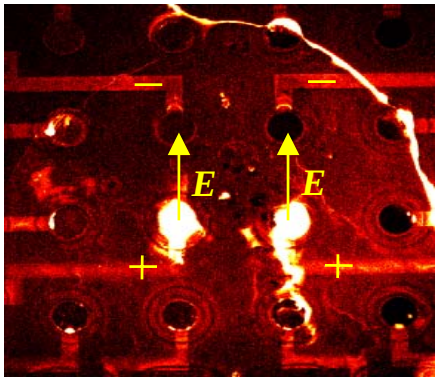
Novel Technology

Disclosure filed for patent application

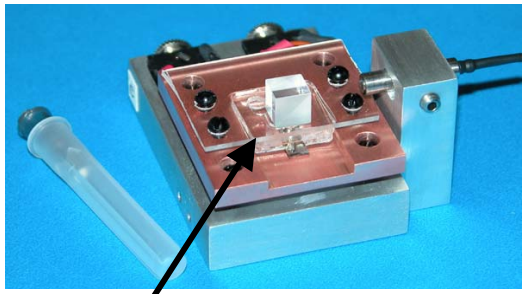
Methods of Approach

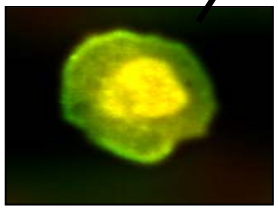




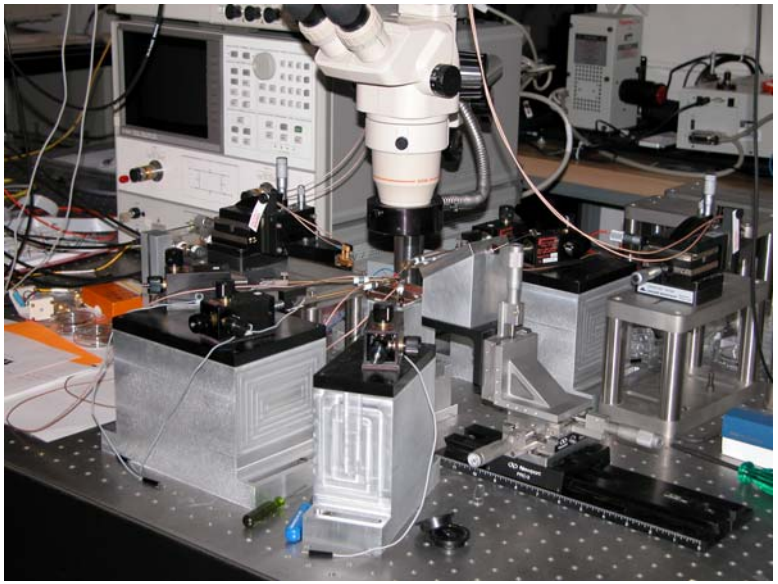


Cell-Based Biosensor





Cells Cultured in the Bio-Chamber



Seed Projects Partially Sponsored by ERC

Ogden, Blowers, Raghavan (UA)

1. **Treatment of Copper in CMP Waste Streams Using Polyethyleneimine**

2. **Filtration and Biotreatment Scheme to Reclaim and Recycle CMP Wastewater**

3. **Megasonic Cleaning in Semi-Aqueous and Non-Aqueous Media**

4. **Minimizing Usage of IPA for Tool Cleaning**

Graduate Students in Thrust C

- Brett Belongia (Mykrolis)
- Dawn Lowman (U Utah Medical School)
- Iouri, Beregovskii, (JPL)
- Gray Bohon (Intel)
- Elizabeth Castro
- Kai Chen
- Gary Chen (Micron Technology)
- Soon Chon (Intel)
- Brian Conaghan
- John Croft (Intel)
- John DeGenova (TI)
- Kedar Dhane
- Daniel Frayer (Bechtel)
- Victor M Gamez
- Andrew Hebda (Freescale)
- Jeremy Hollingsworth (Brown and Caldwell)
- Asad Iqbal
- Harpreet Juneja
- Kon-Tsu Kin (ITRI)
- Elena Krikanova (IBM)
- Nikhil Krishnan (Columbia University)
- Taehoon Lee (Cypress Semiconductor)
- Yi Ling
- Yi Liu
- Majid Mansoori (TI)
- Sergio Martinez (TI)
- Morven McAlister (Pall)
- Lillian Mena-Acevedo (Pharmacia)
- Robert Morris (Raytheon)
- Valeria Ochoa
- Yierra Padillas
- Viraj S. Pandit
- Srinivasan Raghavan (TI)
- Prashant Raghu (Intel)
- Gregory Romas (TI)
- Karla Romero (AMD)
- Arturo Ruiz-Yeomans (AMD)
- Farrokh Salek
- Michael Schmotzer
- Matt Scholz (Max Planck Institute)
- Daniel Seif (AMD)
- Hrishi Shende
- Peter Skrdla (Merck & Co.)
- Leah, Stanley (Intel)
- Nadia Syvestry-Rodriguez
- Subramanian Tamilmani (Intel)
- Sara Thurwachter (McKinsey & Co.)
- Mohith Verghese (ASM)
- Worawan Maketon
- Baochun Wu (IBM)
- Jun Yan
- Jacky Yao
- Umur Yenal
- Chris Yim (AMD)

Thrust D
Dry Processing and Manufacturing Step Reduction

Faculty (in order of presentations):

Karen K. Gleason, Chemical Engineering, MIT	Task D.1
Christopher K. Ober, Materials Science & Engineering, Cornell	Task D.1
Anthony Muscat, Chemical Engineering, UA	Task D.5

Tasks:

D1: Solventless Lithography

D5: Supercritical CO_2 Processing (Muscat)

Notes:

D2: Additive Processing (graduated 2002)

D3: Decision Making (moved to Thrust C)

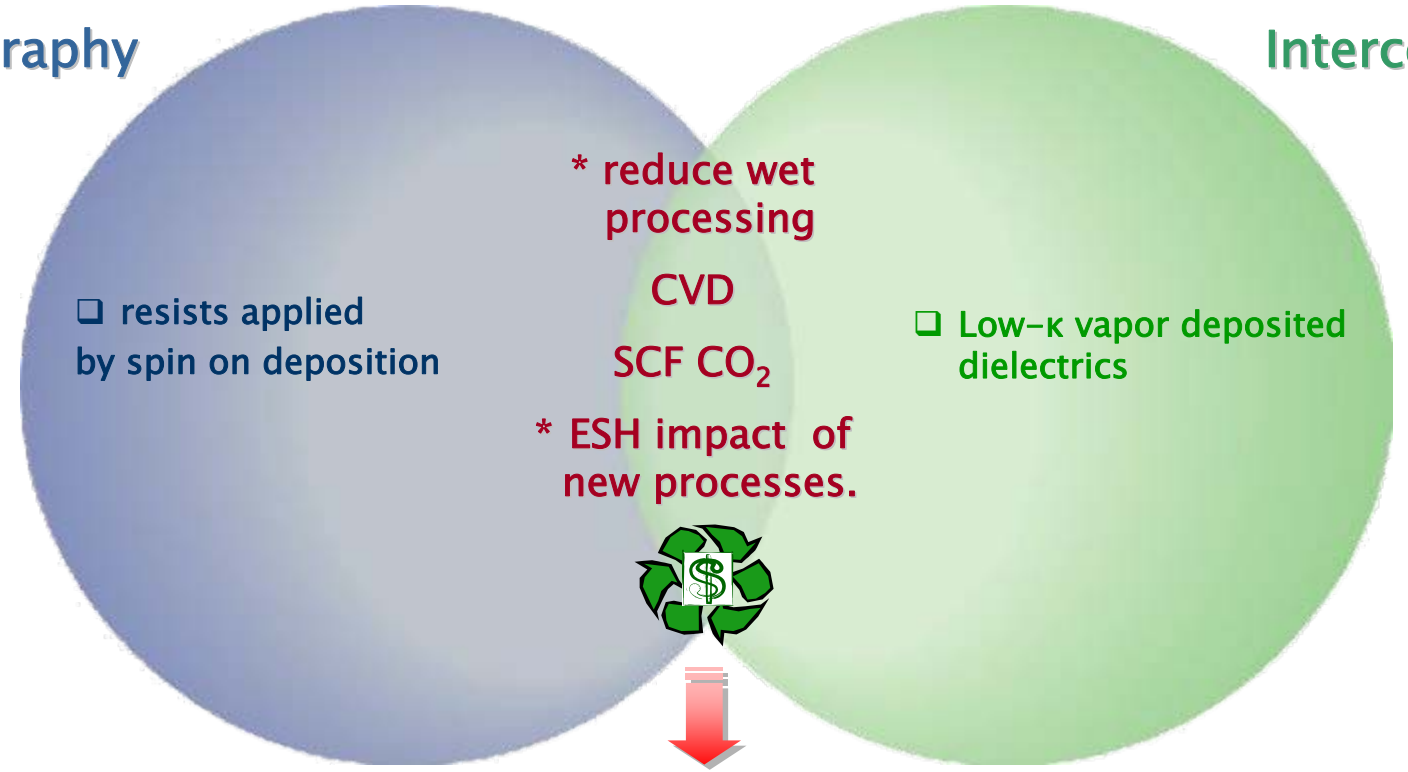
D4: Drop Ejection of Photoresist and Low k Dielectrics (graduated 2005)

Chemical Vapor Deposition: Direct Patterning and Selective Deposition Thrust D (Task 425.006)

Yu (Jessie) Mao, Hilton Pryce Lewis, Sal Baxamusa, and Karen Gleason
Department of Chemical Engineering, MIT

Nelson Felix, Victor Pham, Gina Weibel, and Chris Ober
Department of Material Science, Cornell

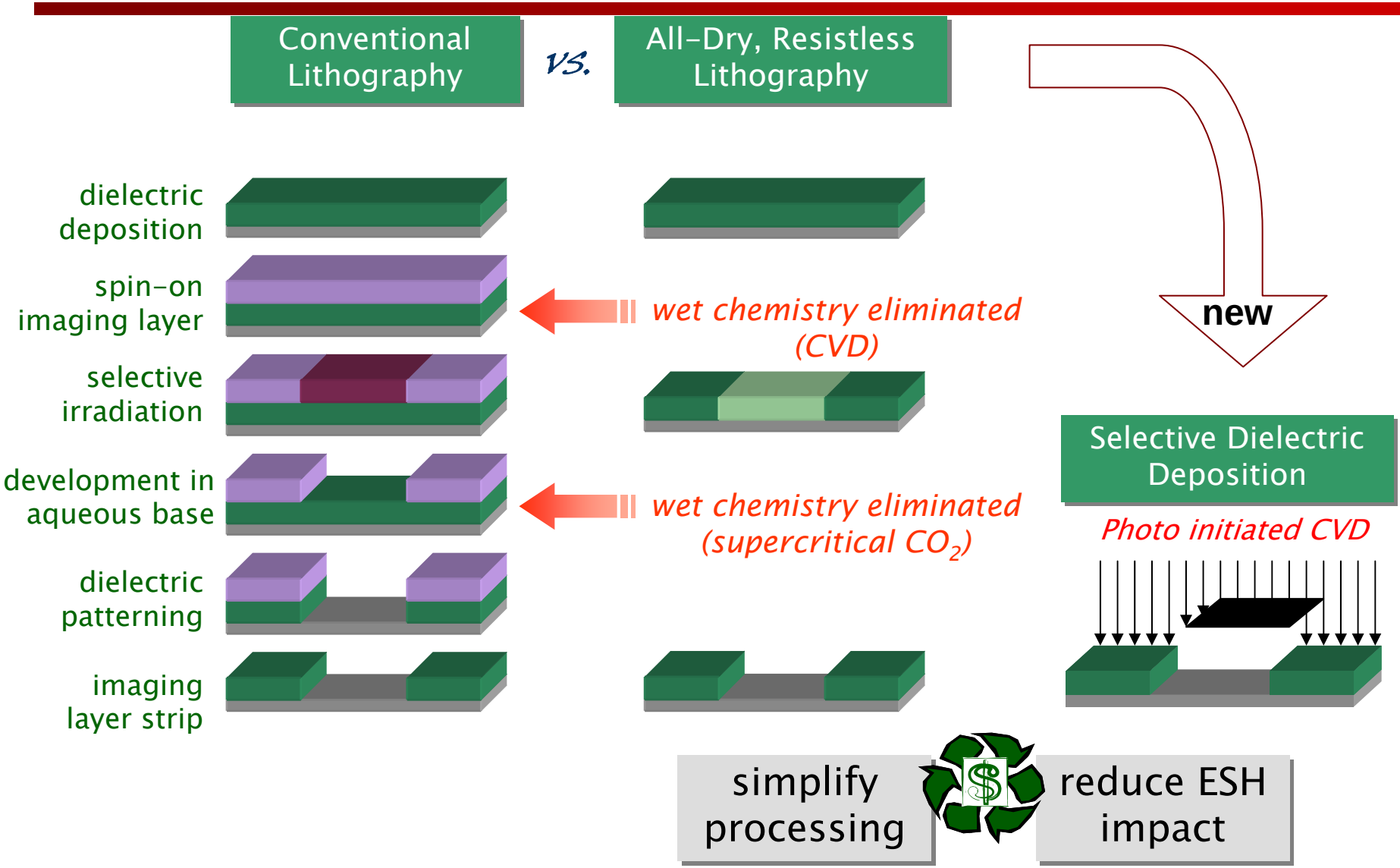
Opportunities for Thrust D



Goal: Superior Performance with Environmental Responsibility

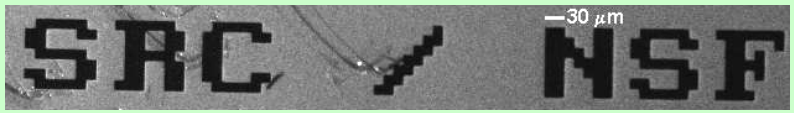
Started October 1998 via extension funding from NSF

Proposed Evolution of Dielectric Patterning

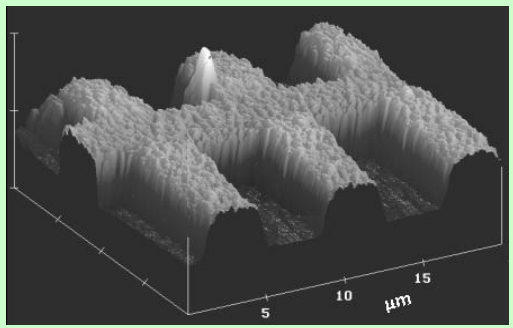


Progress in patterning of CVD Films

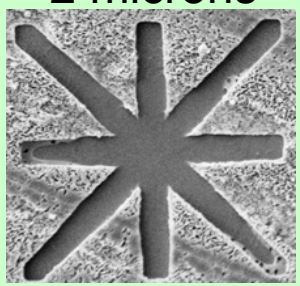
30 microns



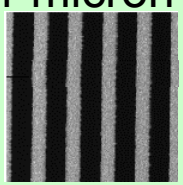
5 microns



2 microns



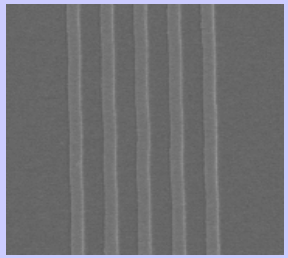
1 micron



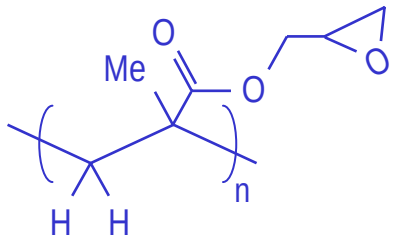
Low k dielectric films

Pryce Lewis HG, Weibel GL, Ober CK, and Gleason KK CVD 7, 195 (2001)

80 nm

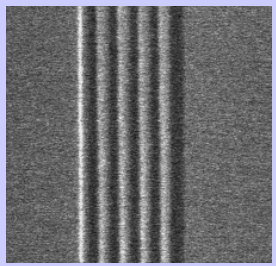


negative tone

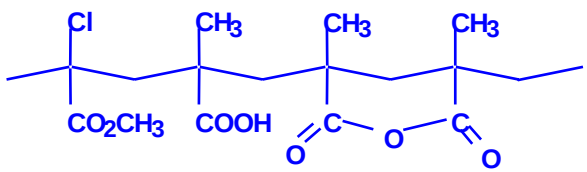


Mao Y, Felix NM, Nguyen PT, Ober CK and Gleason KK JVST B 22, 2473 (2004).

60 nm



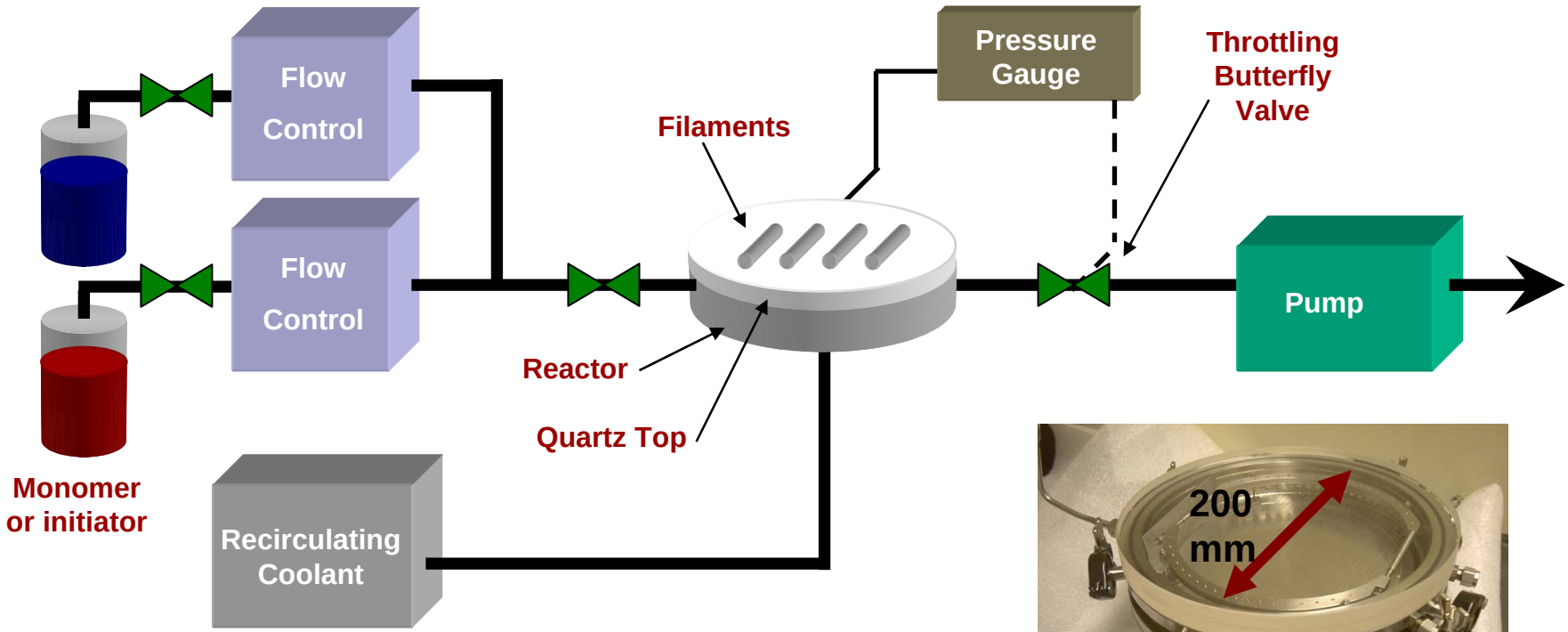
positive tone



Mao Y and Gleason KK Langmuir (in press).

iCVD photoresists

initiated CVD (iCVD)

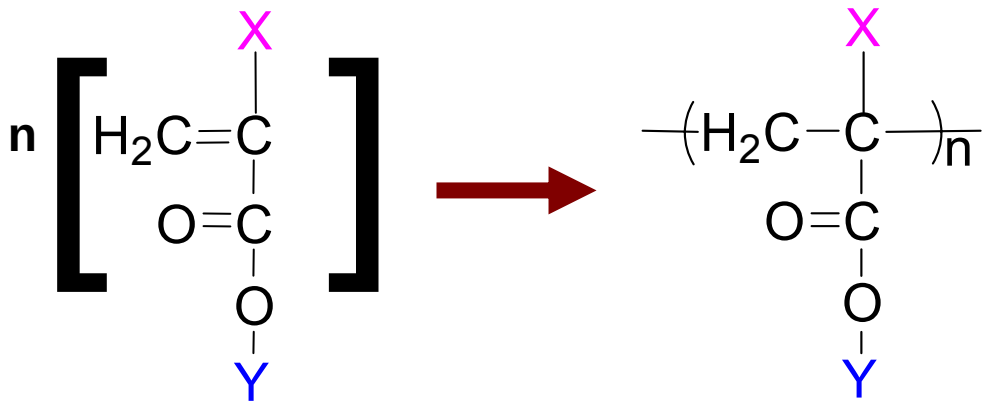


$$I\text{–}I \xrightarrow{\Delta} 2\,R^{\bullet} \quad \textit{initiation}$$

$$R^{\bullet} + n\,M \longrightarrow R\text{–}(M)_n^{\bullet} \quad \textit{propagation}$$

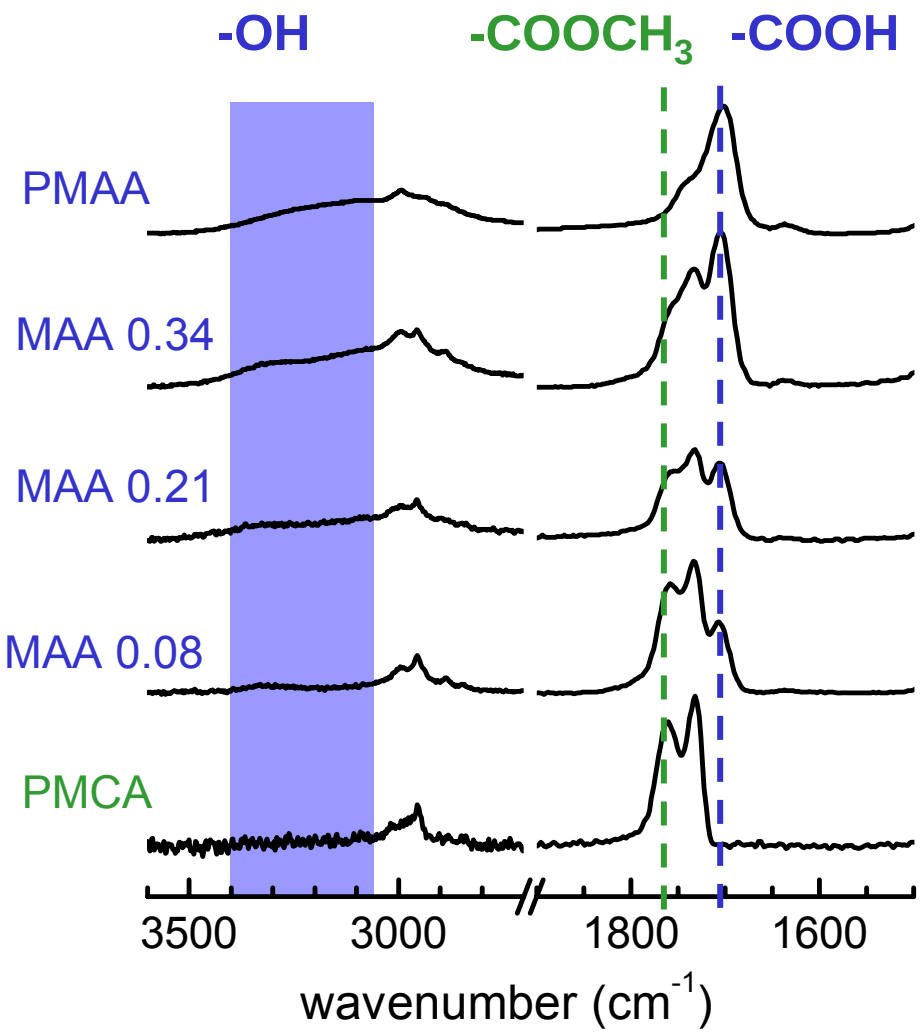
$$R\text{–}(M)_n^{\bullet} + R^{\bullet} \longrightarrow R\text{–}(M)_n\text{–}R \quad \textit{termination}$$

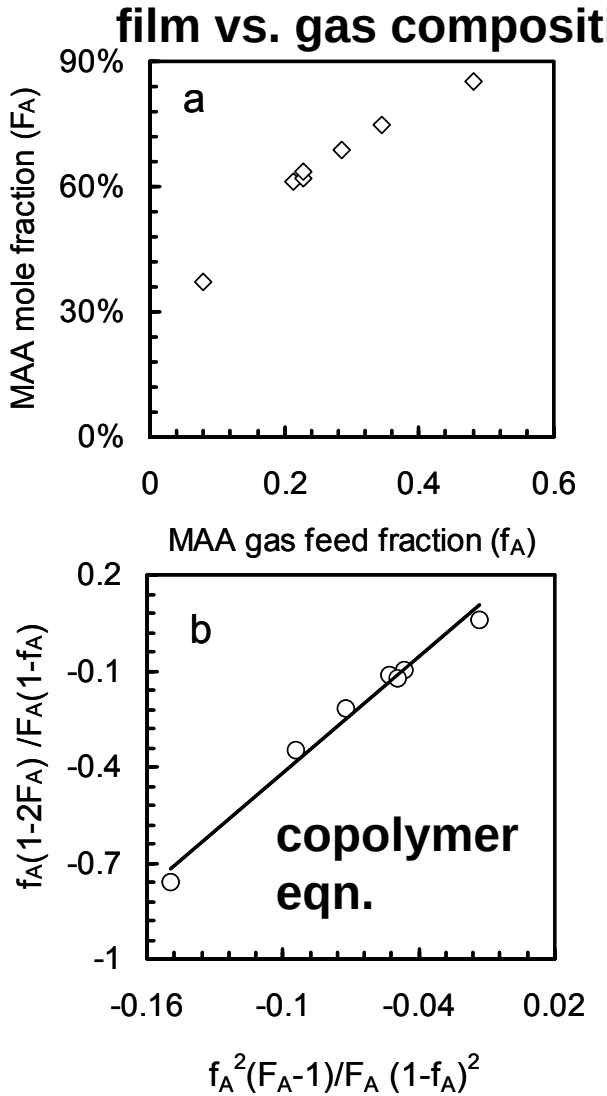
Polyacrylics by iCVD



	X	Y	
crosslink under irradiation	$-CH_3$	$—CH_2–CH(O)–CH_2$	poly(glycidyl methacrylate) **PGMA**
chain scission under irradiation	-Cl	$-CH_3$	poly(methyl α-chloroacrylate) **PMCA**
	$-CH_3$	$—O—C(=O)—R$	poly(methacrylic anhydride) **PMAH**

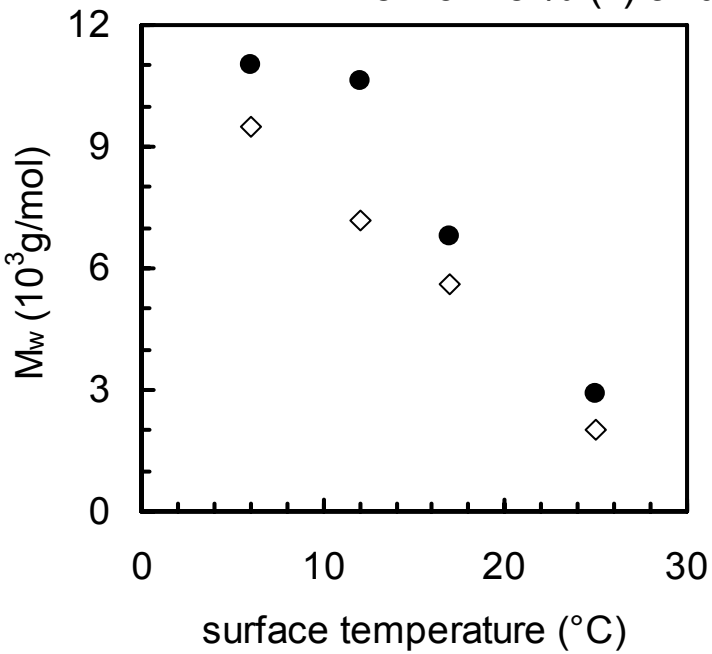
iCVD P(MCA-MAA) Copolymer

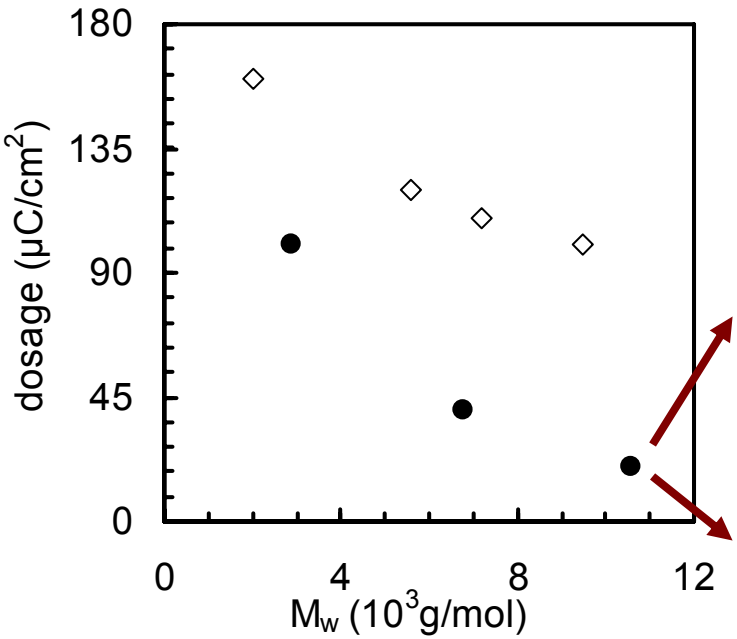


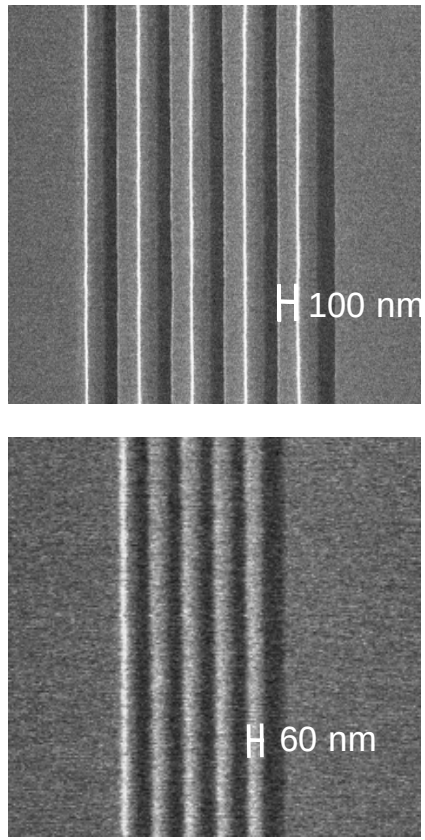


Control of MW and Sensitivity

P(MCA-MAA) iCVD copolymer thin films
with original MAA compositions
75-76 mol% (•) and 40-44 mol% (◊).



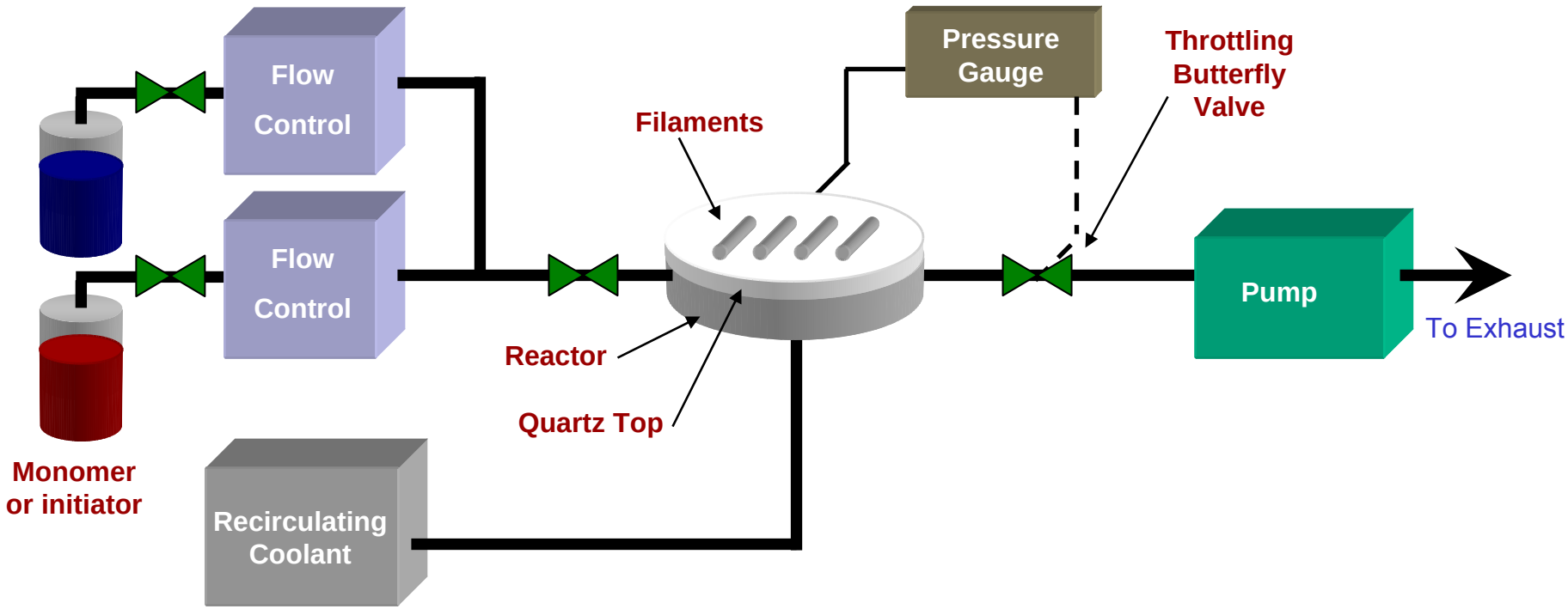




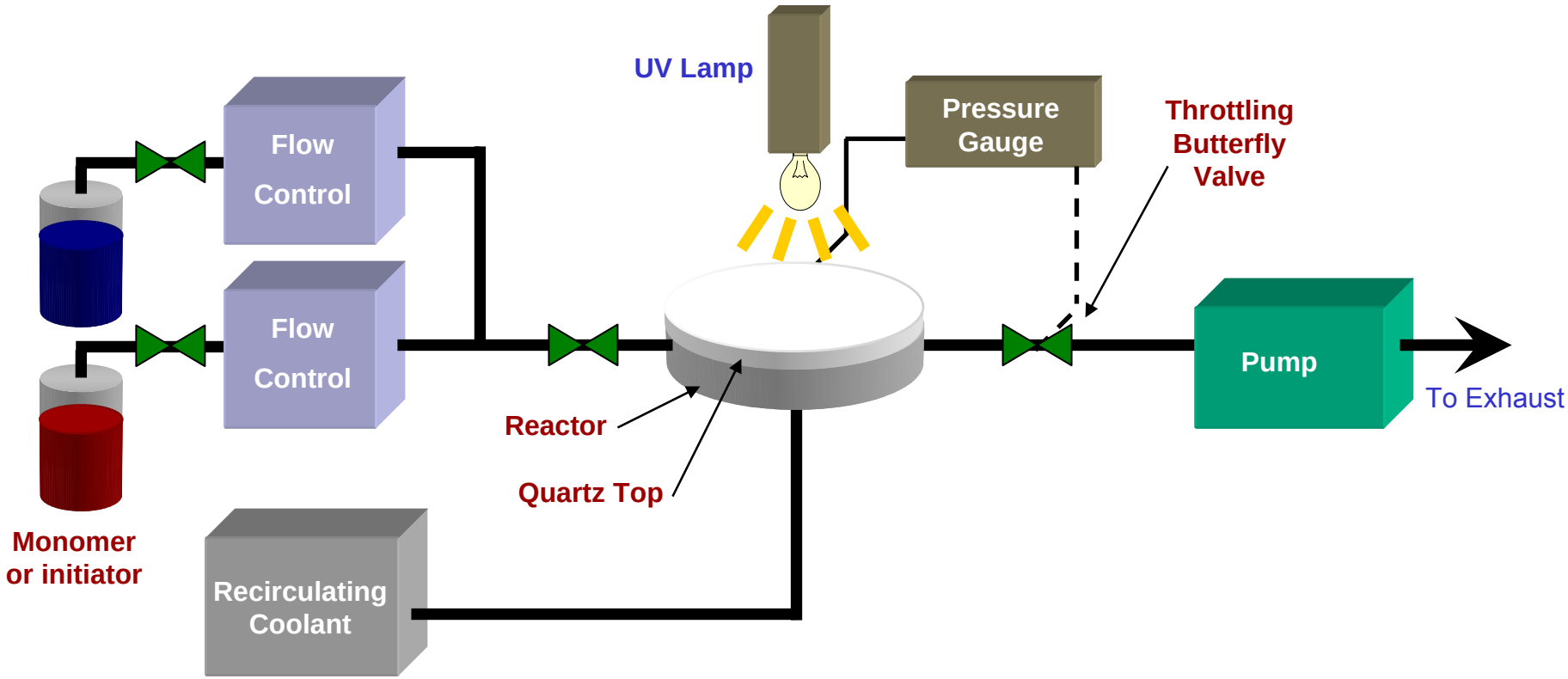
MW decreases with increasing surface temperature, indicating surface propagation.

Minimum dosage for complete removal of post annealed films decreases with MW and increase MAA fraction.

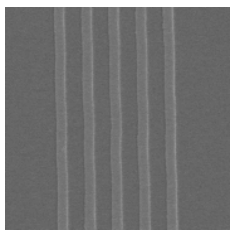
iCVD Reactor (hot filaments)



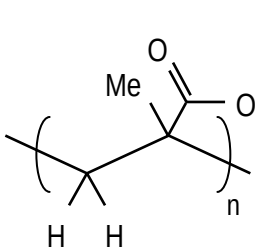
piCVD Reactor (no filaments)



FTIR poly (glycidyl methacrylate) [PGMA]



80 nm lines

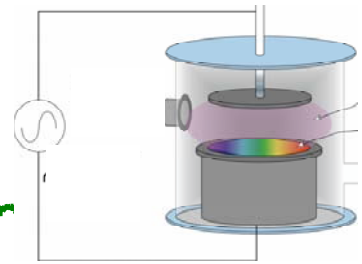


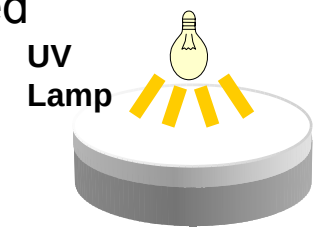
plasma enhanced CVD

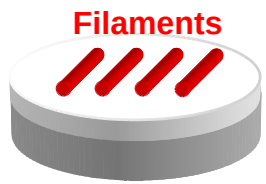
photo-initiated CVD

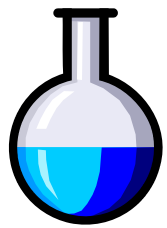
initiated CVD

solution synthesized









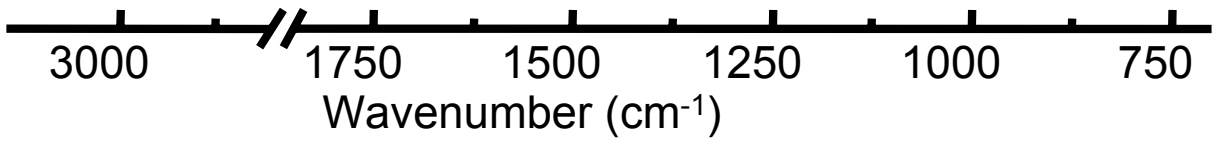
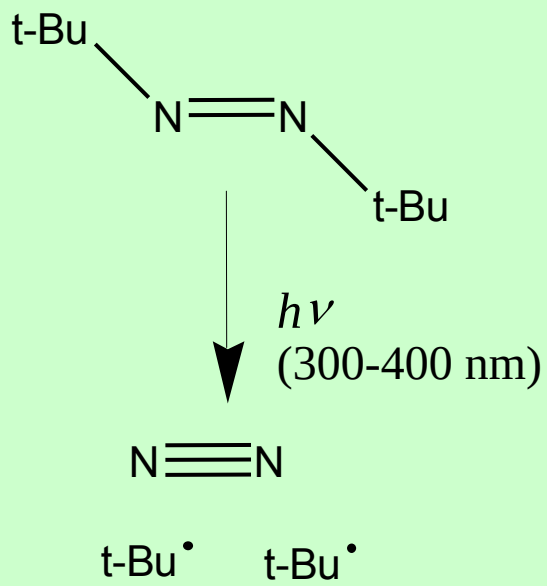
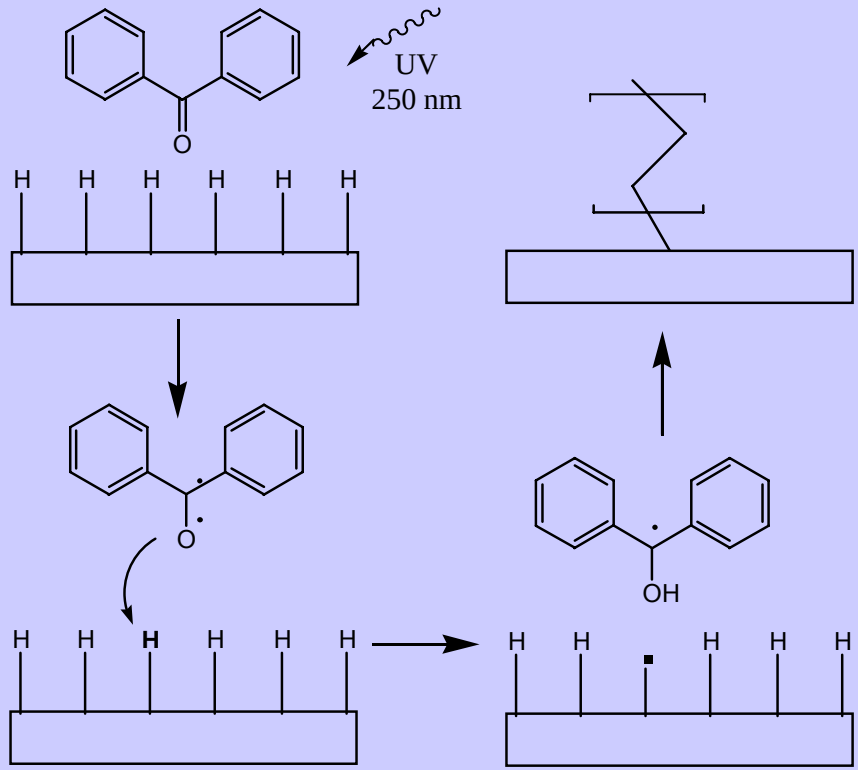


Photo-initiation

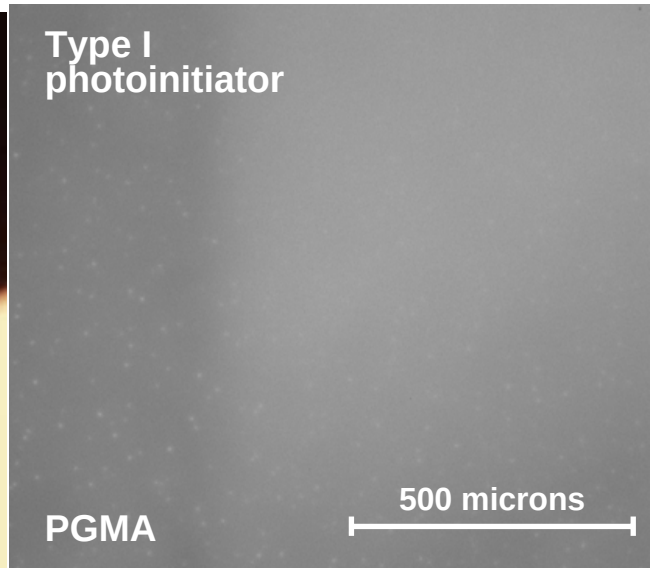
Type I (gas phase)

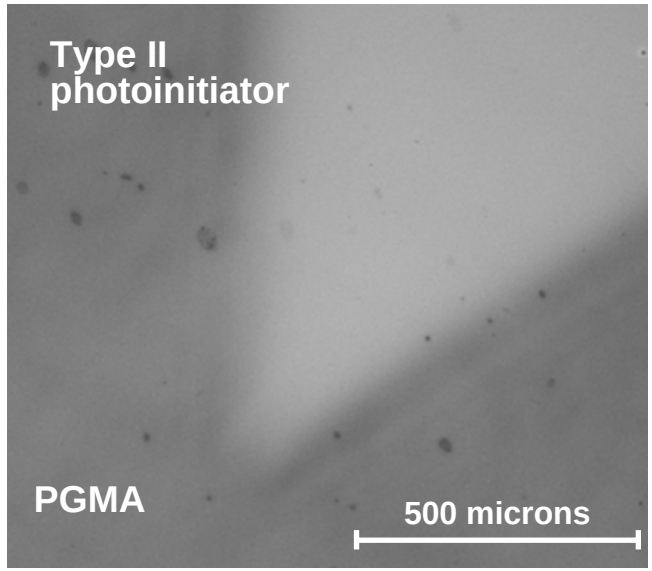


Type II (surface)



Preliminary Work: Selective Deposition by piCVD





resolutions improvement expected with
- **substrate preparation (H terminated wafers instead of PMMA films)**
- **exposure optics**

future work: demonstrate selective piCVD of low k films from commercial precursors and molecular glass precursors synthesized in the Ober group

Lithographic Processing Using Supercritical CO_2

Nelson Felix[1], Victor Pham[1], Gina Weibel[1], Yu (Jessie) Mao[2], Karen Gleason[2], James Watkins[3], and Christopher K. Ober[1]

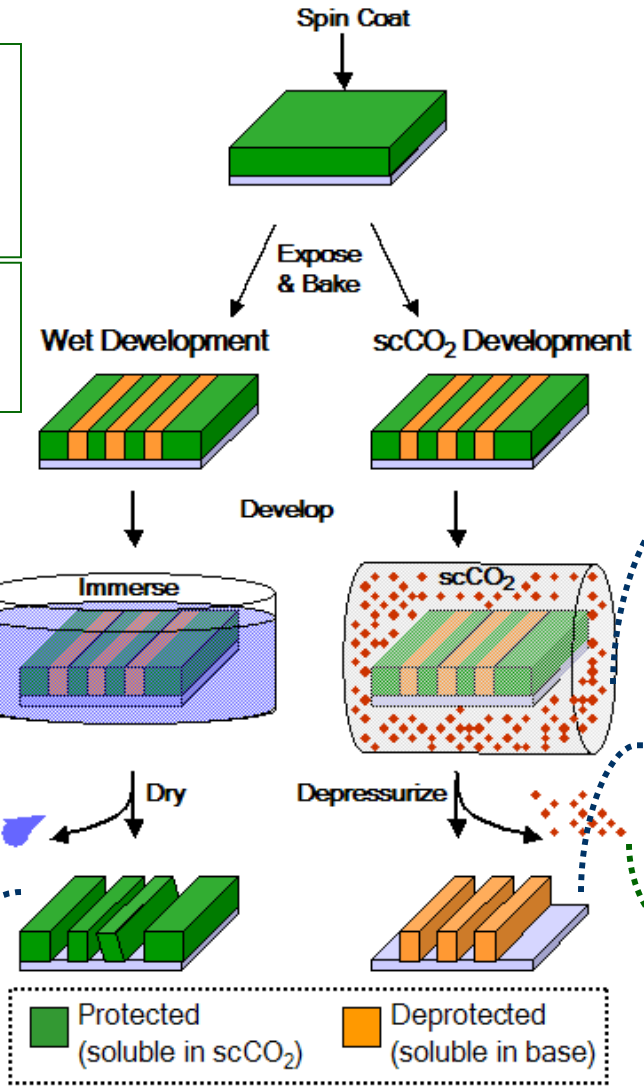
[1]Department of Materials Science, Cornell University
[2]Department of Chemical Engineering, Massachusetts Institute of Technology
[3]Polymer Science and Engineering Department, University of Massachusetts, Amherst

Advantages of Supercritical CO_2 Development

Elimination of organic solvents and ultra-pure water during processing

2 gram DRAM chip → 32 kg of water

Williams, et al., *Environ. Sci. Tech.*, **36**, 5504, (2002).



Liquid-like density, Tunable Solvating Power

Gas-like transport

Penetrates crevices, no residue

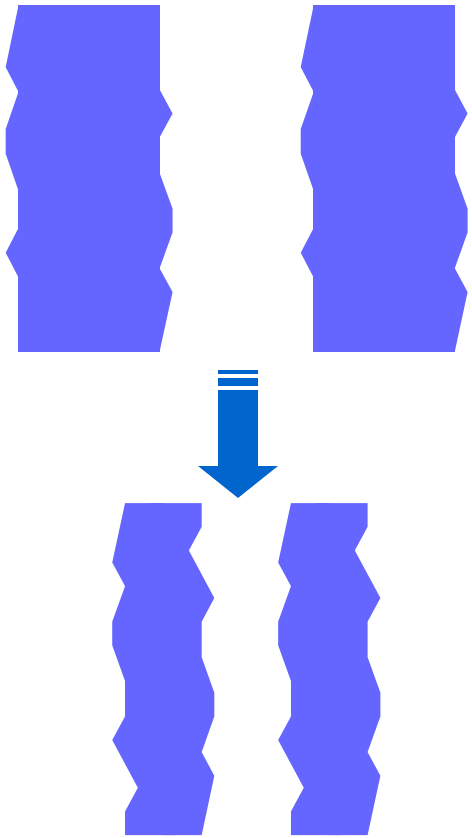
Harmful solvents are cleanly separated via depressurization

No surface tension, eliminates pattern collapse

Next Generation Lithography: Key Problems

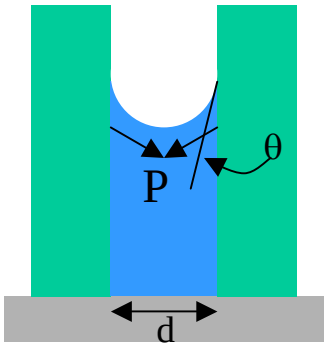
Pattern Variations

< 3nm for 32nm node



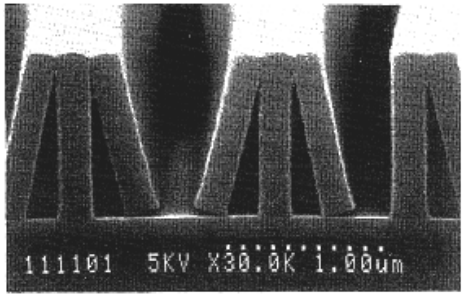
Pattern Collapse

Reduce surface tension



$$P = \frac{\sigma}{R} = \frac{2\sigma\cos\theta}{d}$$

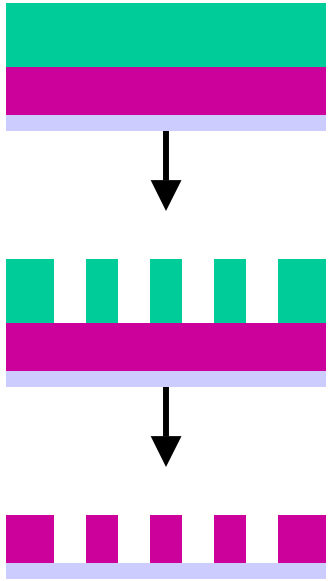
@ 50nm L/S, aspect ratios >2:1 collapse w/water



T. Tanaka, M. Morigami, N. Atoda, *JJAP*, **32**(pt1, 12B) 6059 (1993).

Non-polar Materials

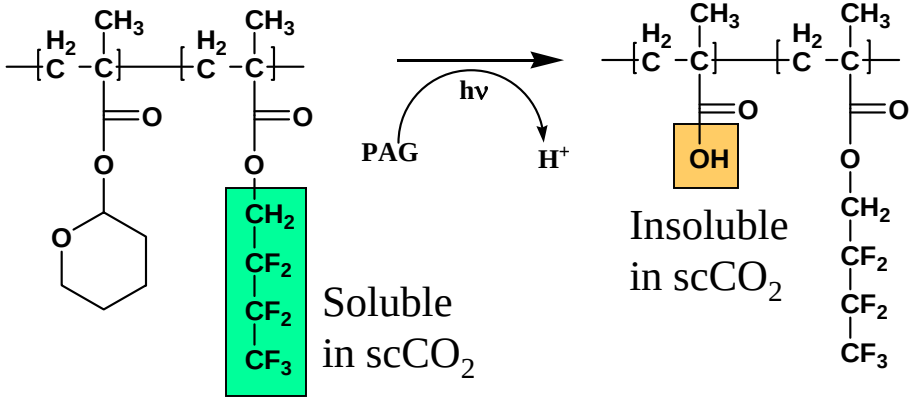
Low-κ applications



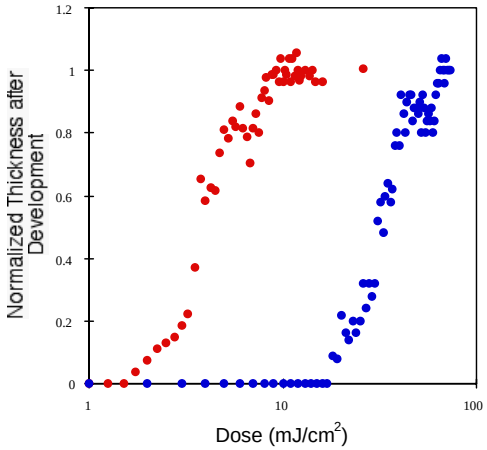
Lack of appropriate non-polar developers → Must use mulitple subtractive steps

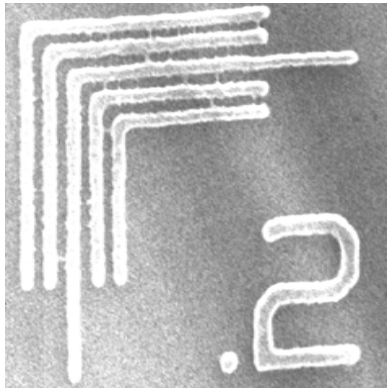
Fundamentals of Supercritical CO_2 Solubility

- Negative tone resists



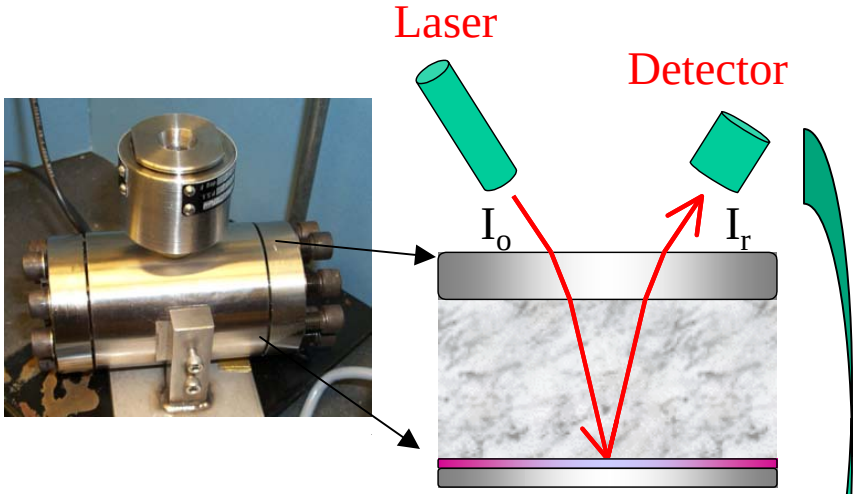
Contrast curves

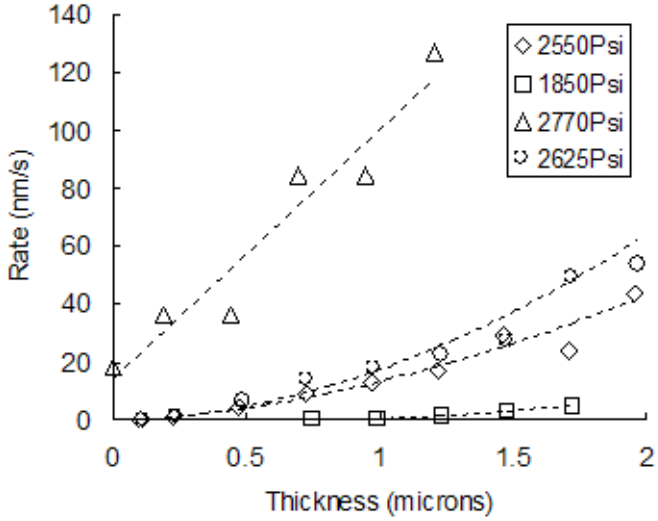




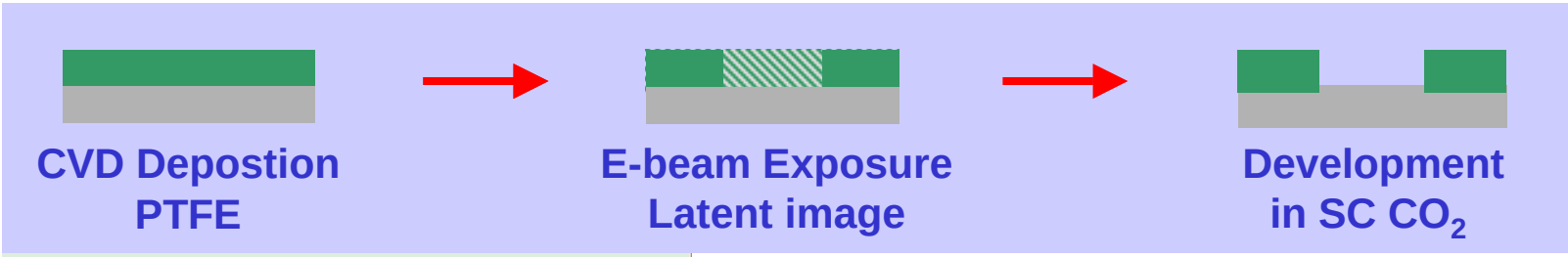
Sundararajan, et al., *Chem. Mater.*, **12**(1), 41, (2000).

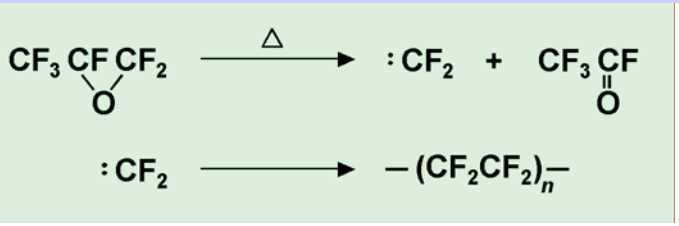
- Dissolution Rate Monitor

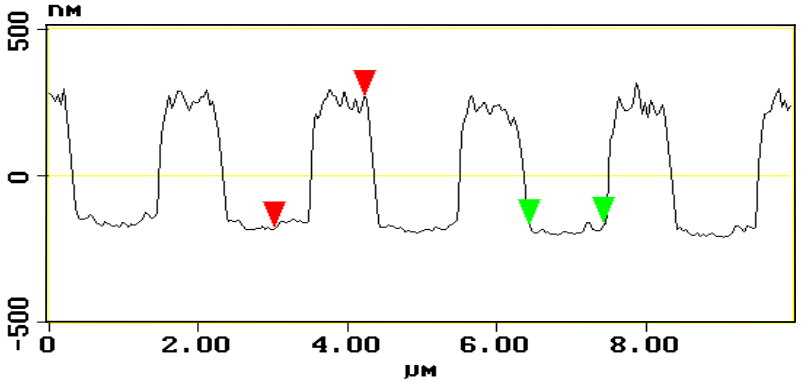




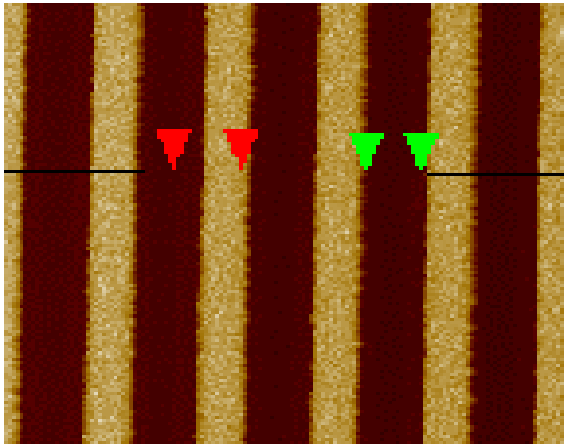
Processing Non-Polar Materials / Low-κ







Cross sectional View

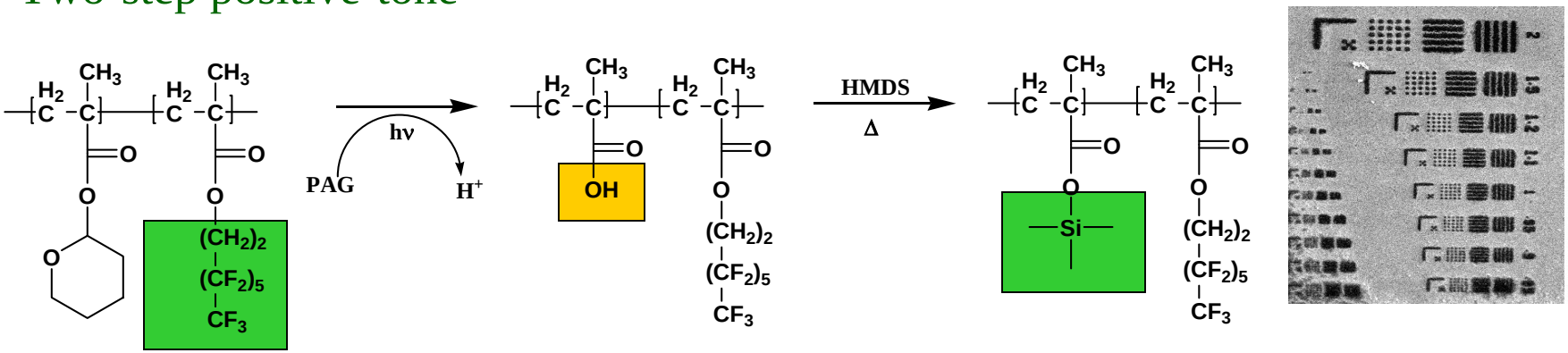


1.0 μ m L/S Pattern

- High selectivity between exposed and unexposed regions under supercritical CO_2 development conditions

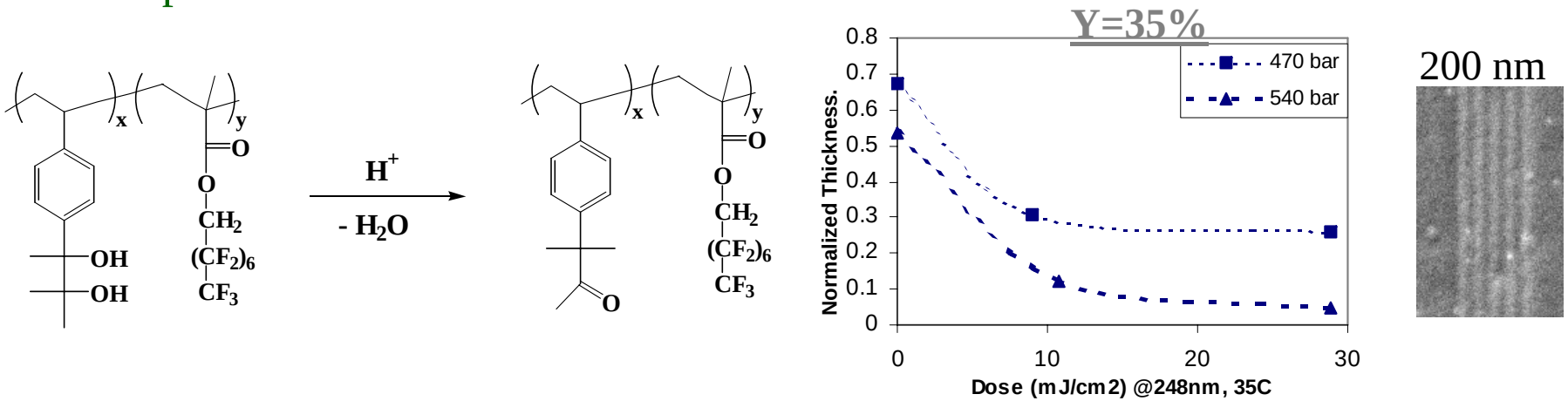
Positive Tone Resists for $scCO_2$ Development

Two-step positive-tone



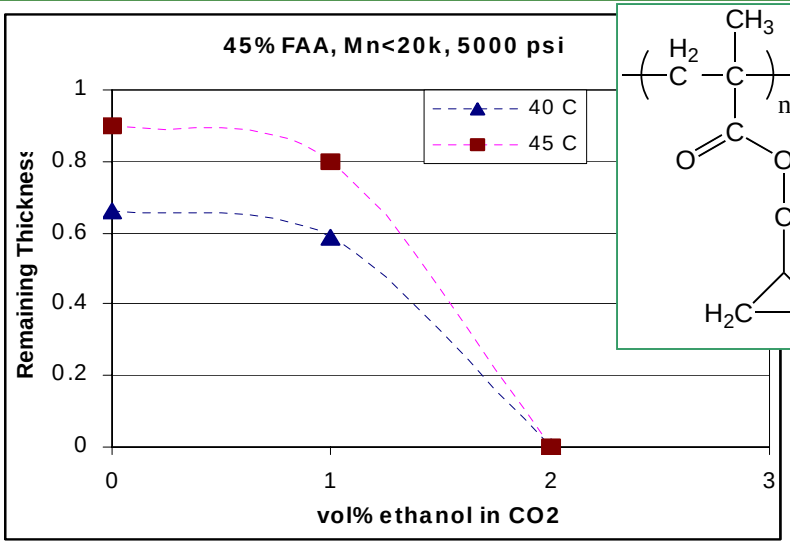
Pham, V Q.. et al., *Chem. Mater.* 15(26), 2003, 4893-5.

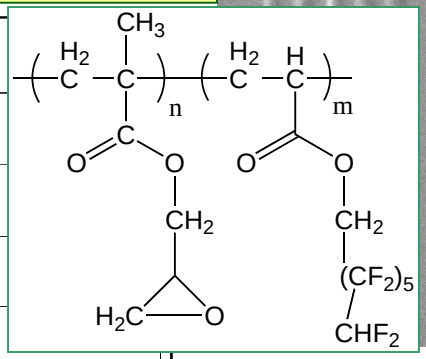
Intrinsic positive-tone!

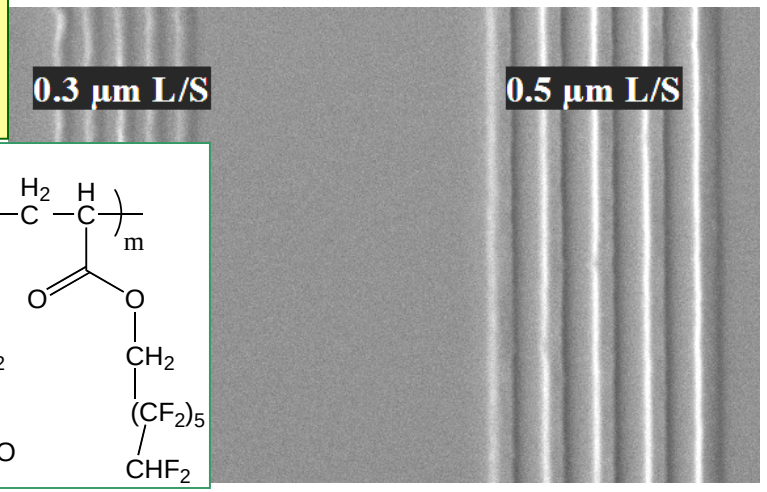


Reducing Fluorination: Using Cosolvents

- Increase solvent density
- Tune polarity of fluid
- Specific interaction with a comonomer





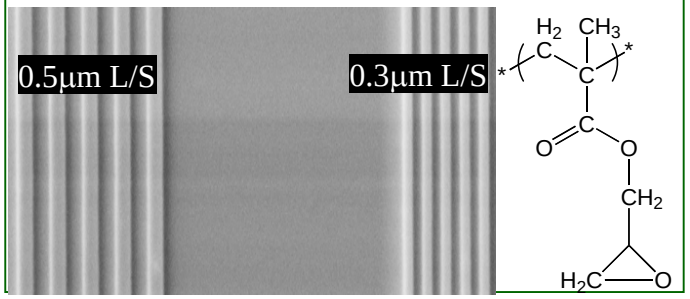


2 vol% ethanol (1.5mol%, 1.6wt%) in $scCO_2$

P = 5000 psi, T = 45°C, t = 10 min

- 1vol% **ethanol**….very little effect
- 2vol% **ethanol**….100% removal

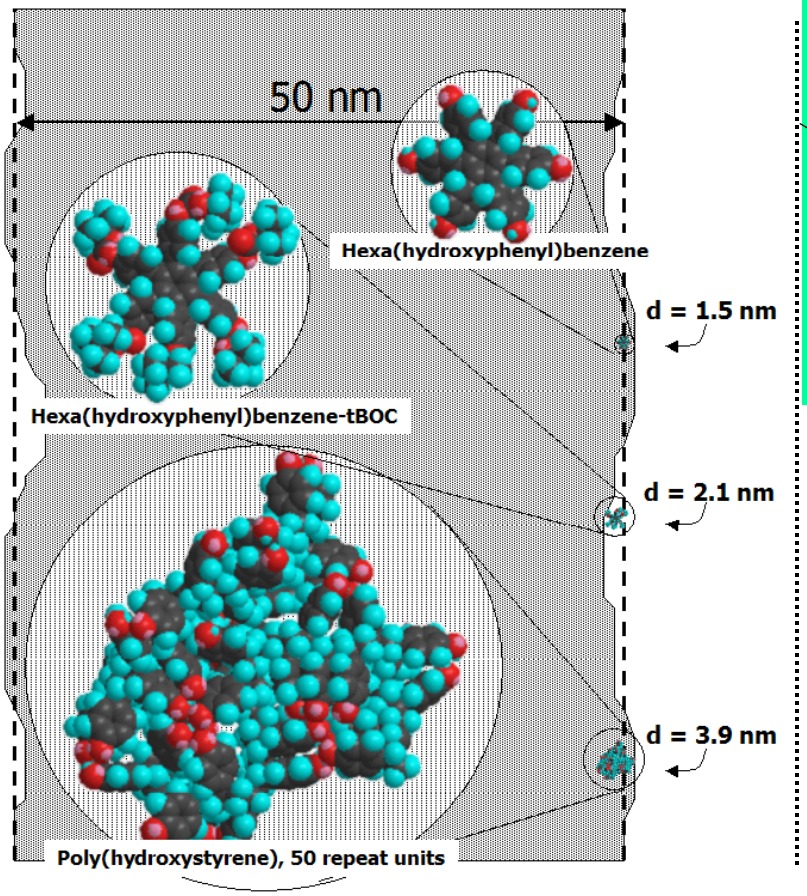
~2 vol% acetone

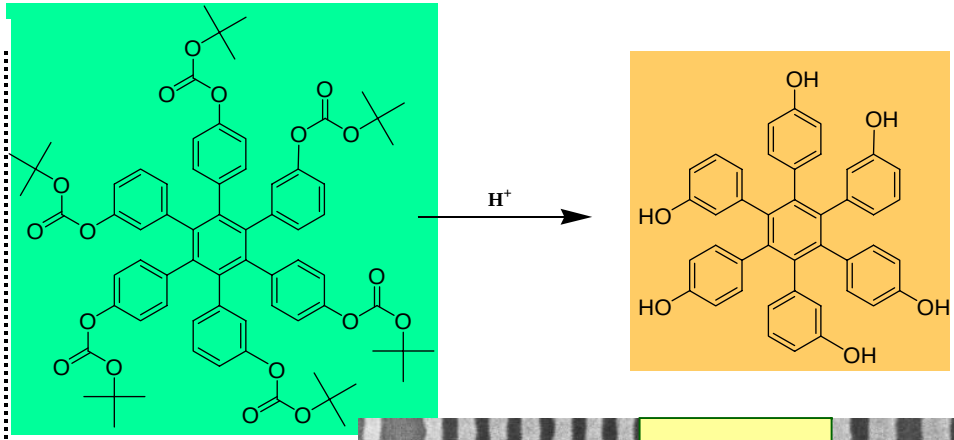


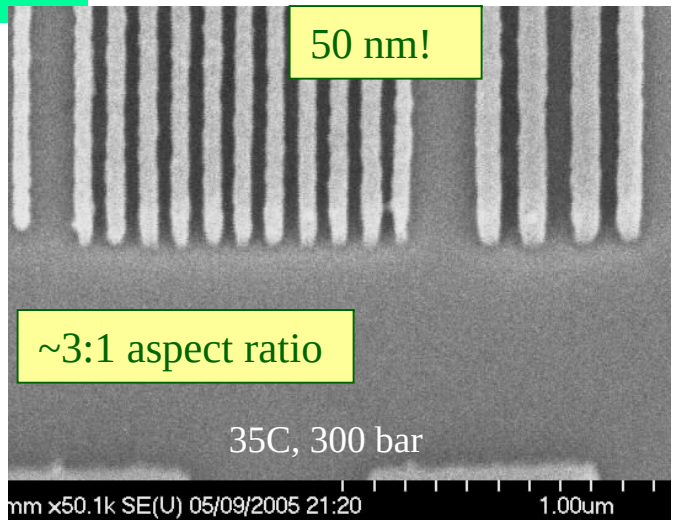
Mao, Yu; Felix, N. et al., *JVST B.*, **22**(5), 2004, 2473-8.

Molecular Glass Resists for CO_2 Solubility

Due to their small size, molecular glass resists of all types have **potential for CO_2 solubility…no fluorine needed**!



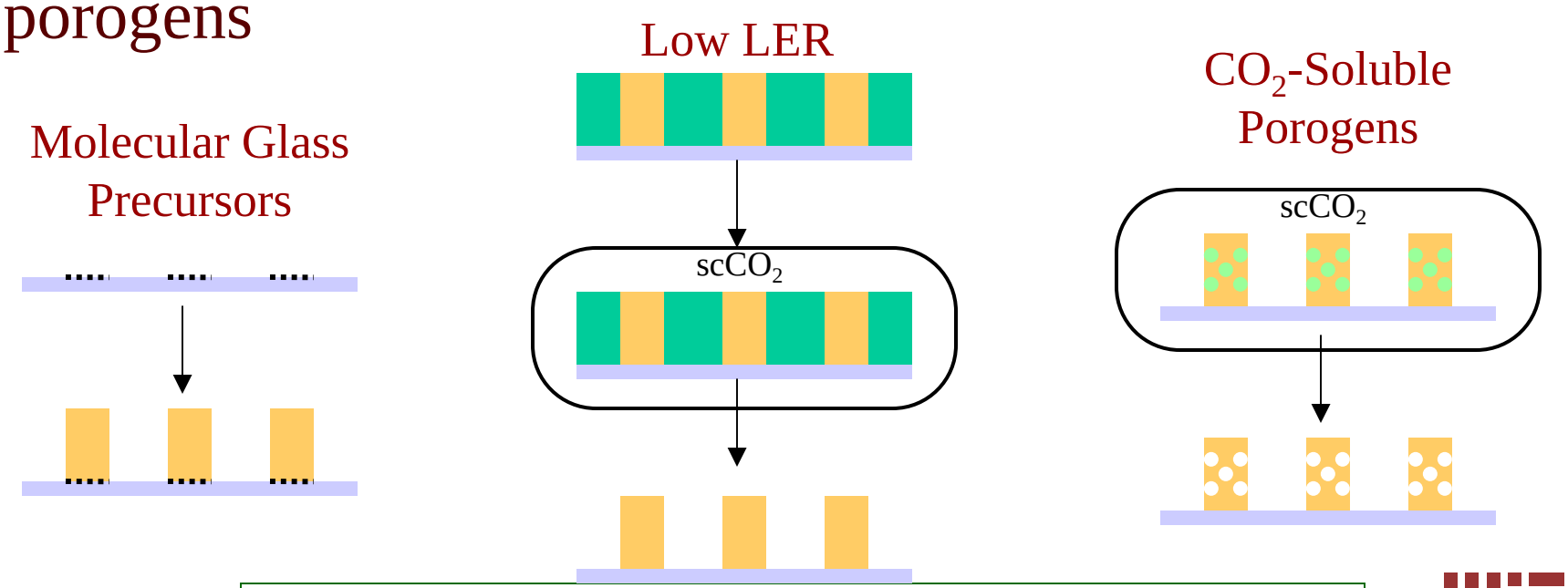




Advanced Materials, in press

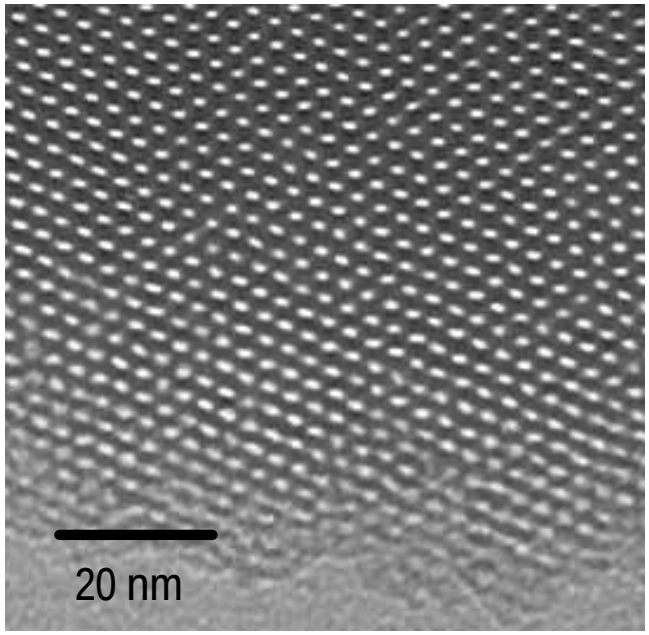
Future Projects

- Use film-forming precursors based on molecular glass photoresists
  - Comprised of structures similar to current C- and Si-based low-κ materials
- Use $scCO_2$ to develop features and remove sacrificial porogens

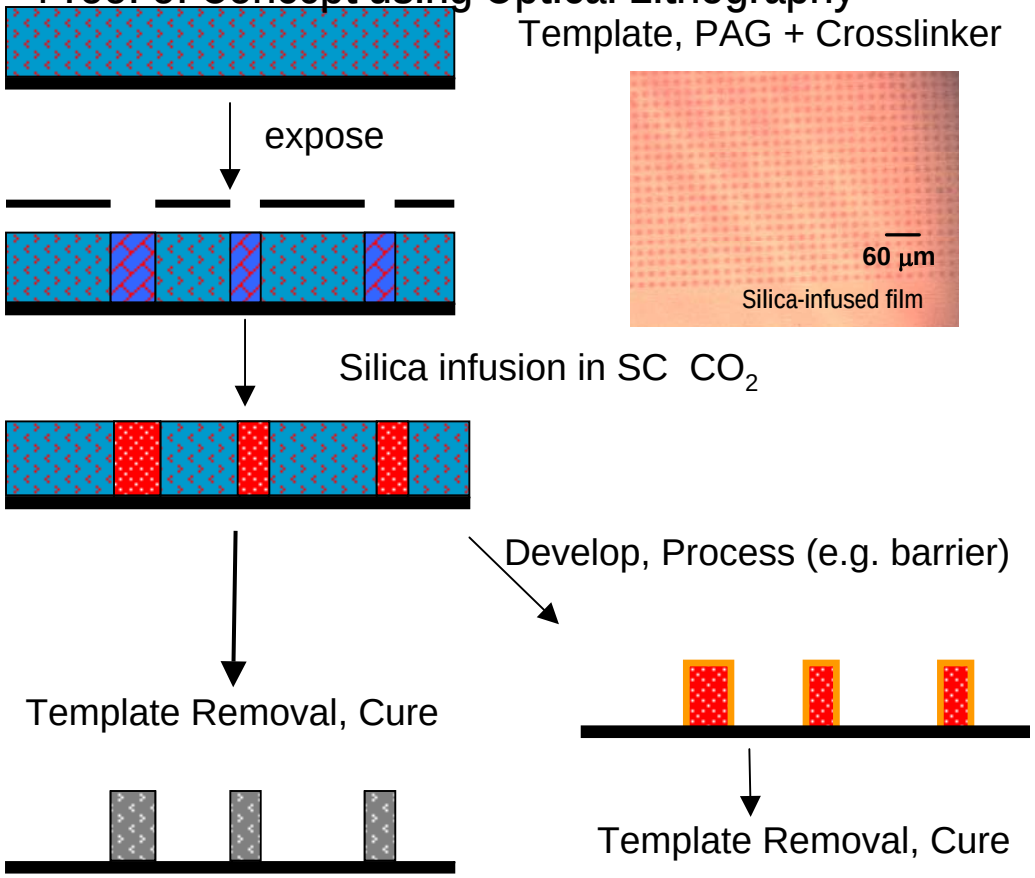


SCF Routes to ULKs and Directly Patterned Dielectrics

ULK Optimization:
2 nm Pores Using Stabilized Template Blends



Direct Patterning:
Proof of Concept using Optical Lithography



Yr 1. ULK Optimization: **Target:** Robust film, 2 nm pores, k less than 2.1, hardness > 1 GPa.

Yr 2. Direct Patterning: **First Target:** Homopolymer template, 20-30% microporosity (micropores< 1 nm)

Second Target: Block copolymer template, 40% porosity, micropores + mesopores (2-3 nm)

Pattering: Nanoimprint or optical

Chemistry on Semiconductor Surfaces in Supercritical CO_2

Bo Xie, Lieschen Choate, Eduardo Vyhmeister,
Michael Durando, and Anthony Muscat
Department of Chemical and Environmental Engineering
University of Arizona, Tucson, AZ 85721

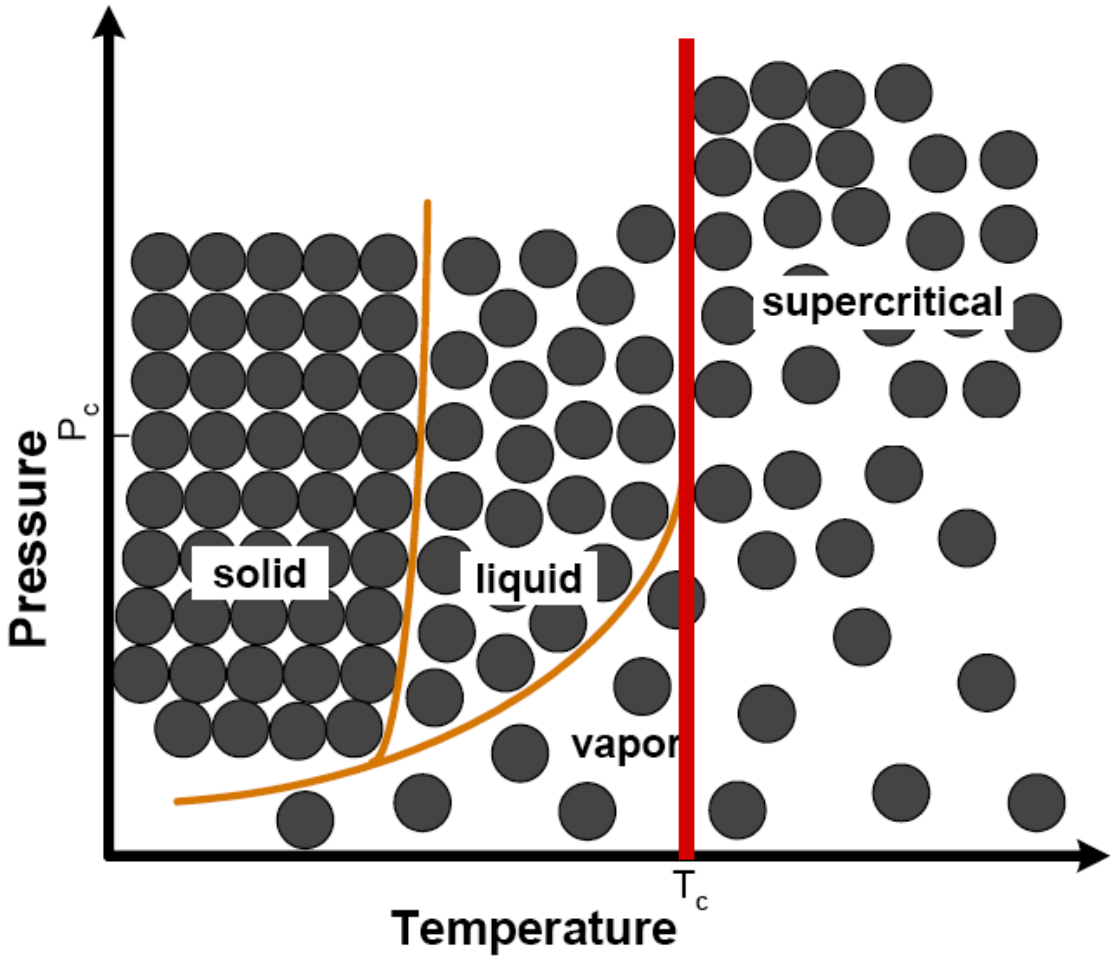
NSF/SRC EBSM ERC Annual Review
February 23-24, 2006 in Tucson, AZ

Microelectronics Applications of $scCO_2$

University Research

- Photoresist development – U. of Cornell/MIT
  Chem. Mater., **15**, 4893, 2003, *Chem. Vap, Dep.* **7**, 195, 2001
- Photoresist drying – U. of Wisconsin/IBM
  JVST B, **18**, 3313, 2000
- Spin coating – U. of North Carolina
  Ind. Eng. Chem. Res., **43**, 2113, 2004
- Metal and low-*k* film deposition – U. of Mass Amherst, U of Idaho
  Chem. Mater., **15**, 83, 2003., *Chem. Mater.* **16**, 2028, 2004, *Science*, **294**, 141, 2001, *Science*, **303**, 507, 2004
- Low-*k* film damage repair – U. N. Texas/TI, U. of Missouri/TEL/SSI, U. of Arizona
  J. Vac. Sci. Technol. B, **22**, 1210, 2004
- Low-*k* film pore capping – U. of N. Texas/TI, U. of Arizona
  Microelec. Engin., **80**, 17, 349, 2005
- SiGe surface preparation – U. of Arizona
  Mat. Sci. Semi. Proc., **8**, 1-3, 231, 2005
- Cu etching – U. of North Carolina, U. of Mass Amherst, U. of Arizona
  J. Am. Chem. Soc. **125**, 4980, 2003, *Chem. Mat.*, **17**, 1753, 2005

Supercritical Fluids: definition



SCF ≡ T > Tc

Where ΔP → continuous ⊗⟩

↓

tunable density

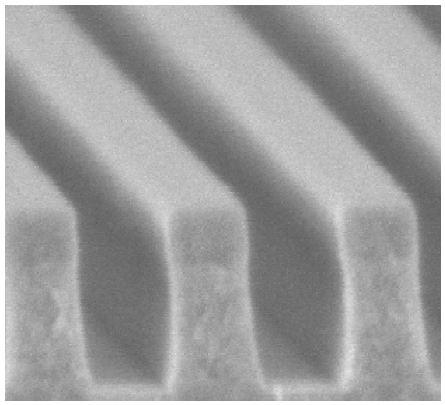
unique to region where T > Tc

&

fluid has properties intermediate between those of gas and liquid

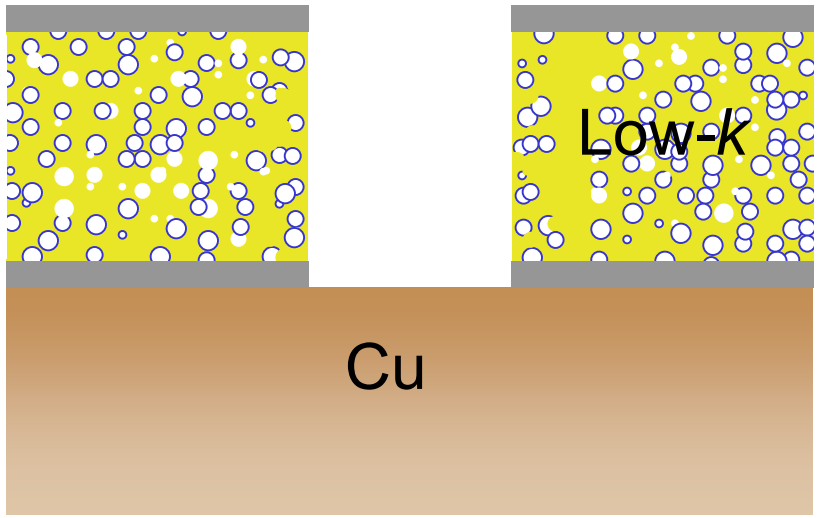
Cu/Low-*k* Process Integration

- Contamination
  - Etching and ashing residue
  - PR, Cu, Cu oxides, and barrier metal



- Veils
- Contamination trapped in pores
- **Damage**
  - **CH_3 depletion**
  - **Si-OH groups**

- **Preserve film properties**
  - **Dielectric constant**
  - **Hydrophobicity**

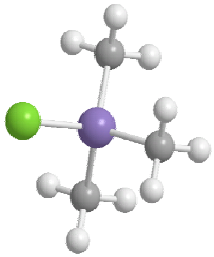


- Practical issues
  - **Pore sealing**
  - Cu barrier

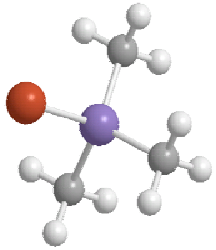
- Materials compatibility
  - low-*k* film
  - Cu interconnects
  - TiN or TaN diff. barriers
- Si_3N_4 or SiC etch stops

- Maintain device structure
  - Critical dimension
  - Etching profile
  - Remove Cu oxides without removing Cu

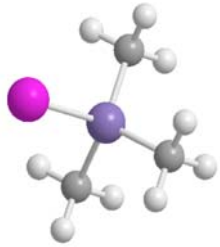
Repair & Capping Molecules



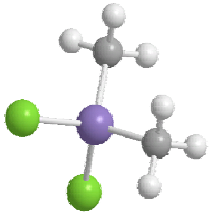
Trimethylchlorosilane
(TMCS, 0.44 nm)



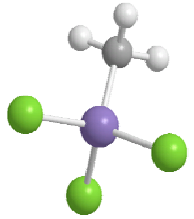
Trimethylbromosilane
(TMBS, 0.45 nm)



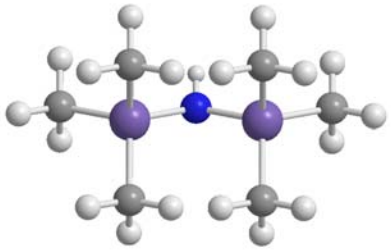
Trimethyliodosilane
(TMIS, 0.47 nm)



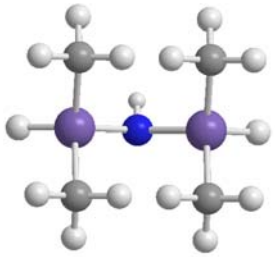
Dimethyldichlorosilane
(DMDCS, 0.44 nm)



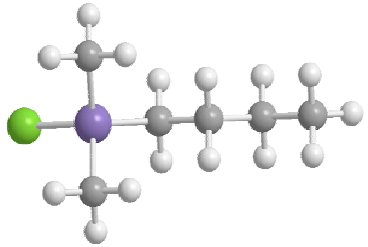
Methyltrichlorosilane
(MTCS, 0.43 nm)



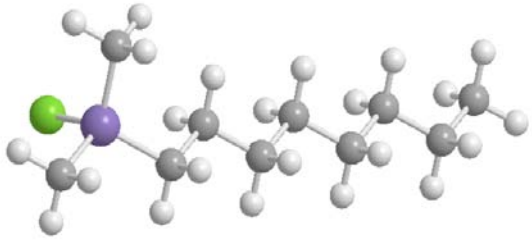
Hexamethyldisilazane
(HMDS, 0.78 nm)



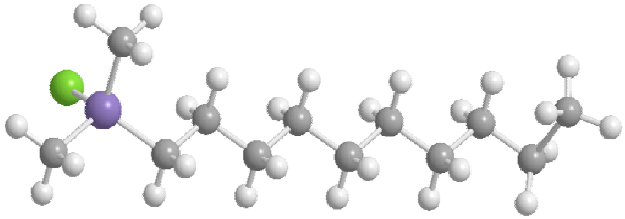
Tetramethyldisilazane
(TMDS, 0.59 nm)



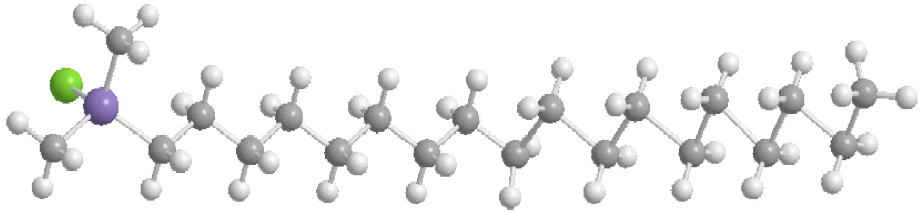
Butyldimethylchlorosilane
(BDMCS, 0.80 nm)



Octyldimethylchlorosilane
(ODMCS, 1.38 nm)



Decyldimethylchlorosilane
(DDMCS, 1.54 nm)

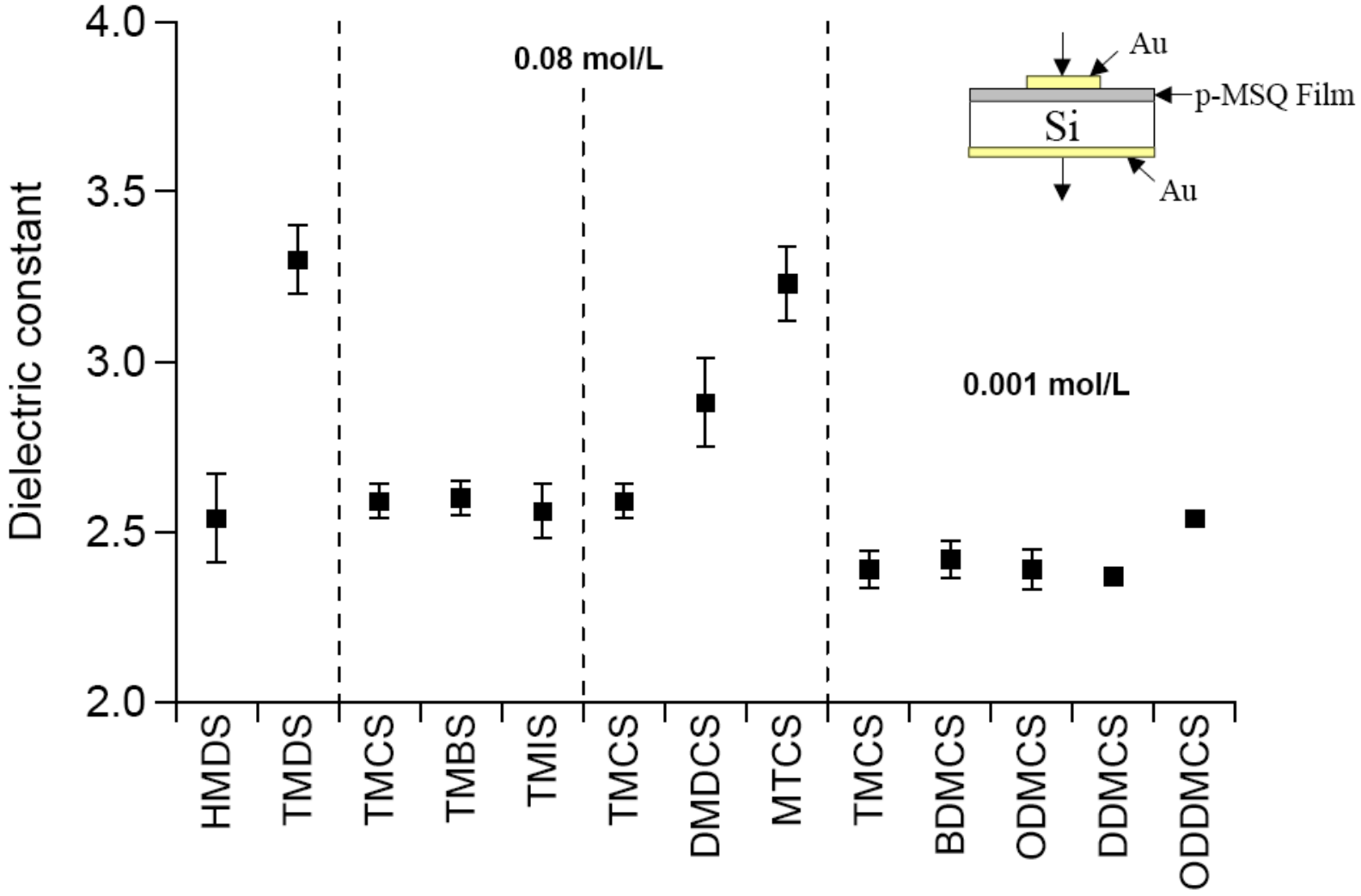


Octadecyldimethylchlorosilane
(ODDMCS, 2.27 nm)

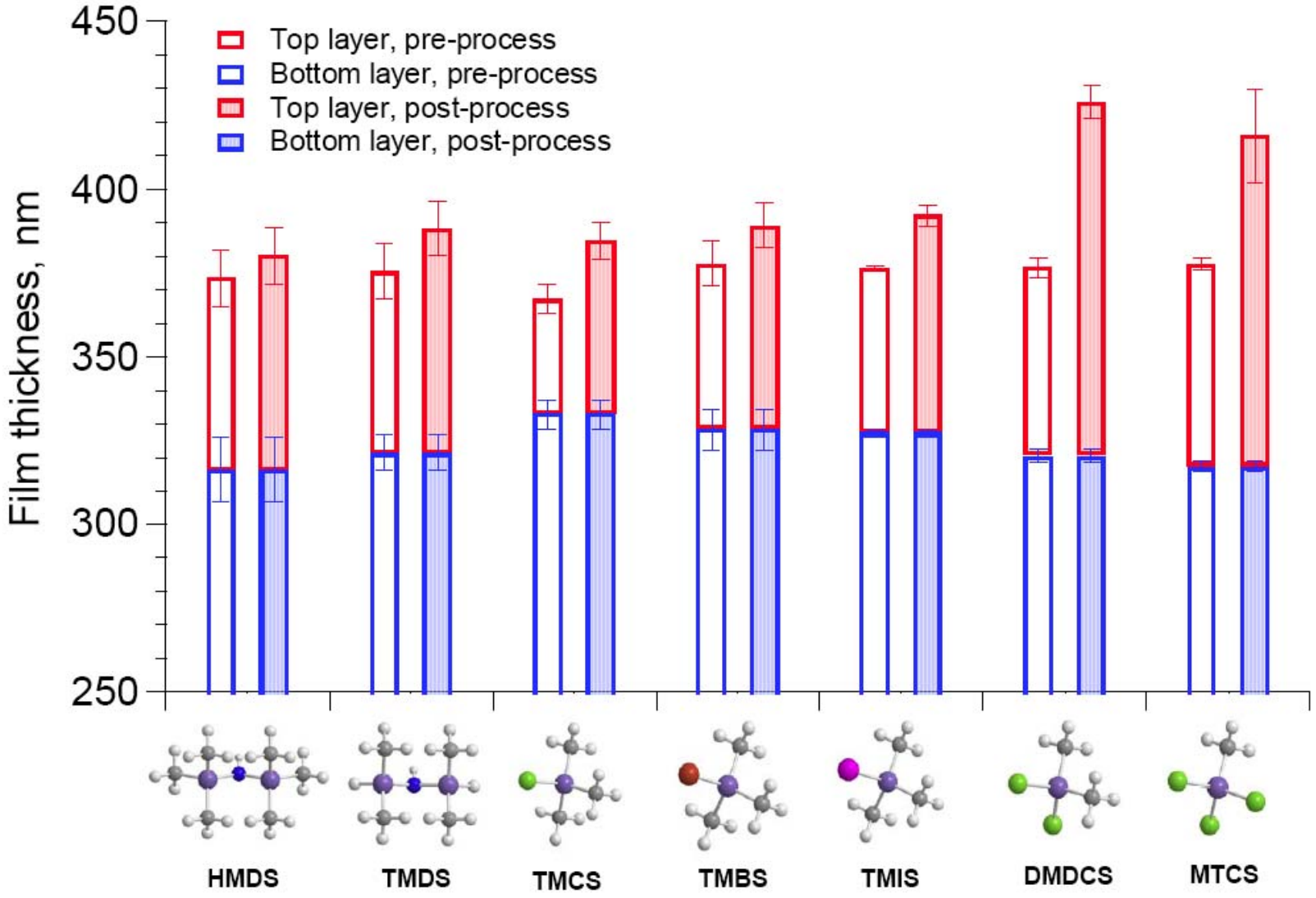
- **Leaving group effects in Cl, Br, I series**
- **One or more reactive head groups**
- **Chlorosilane vs disilazane**

Dielectric Constant after Silyl Treatments

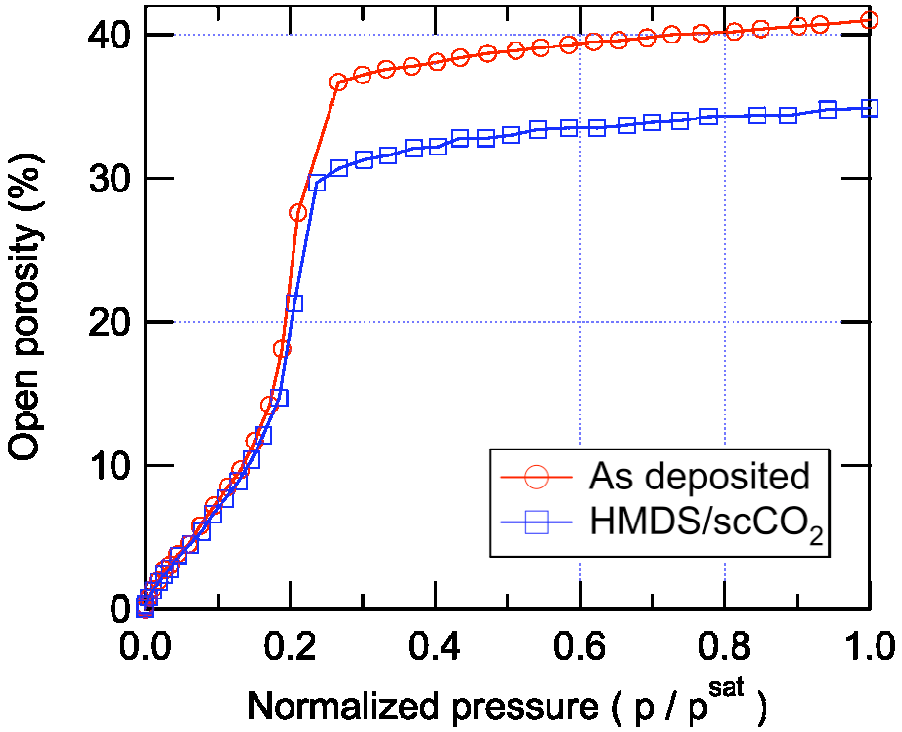
- 4284A Agilent Precision LCR Meter, 1MHz, -40V to +40V sweep
- 100nm thick, 0.1cm diameter Au gate, 100nm thick Au on the wafer backside
- Capacitance in accumulation is used to determine dielectric constant

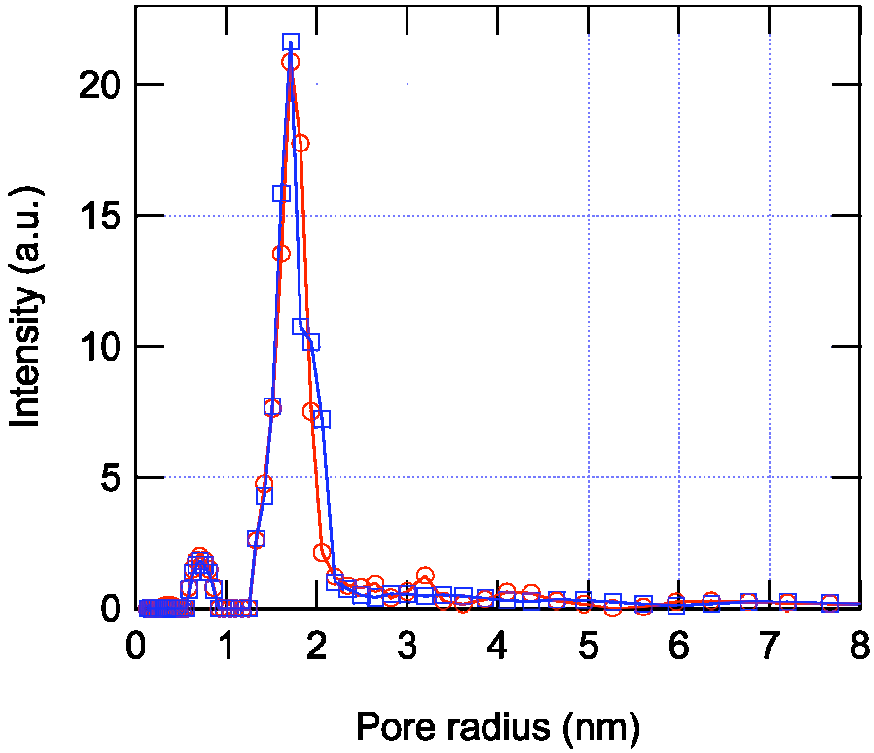


Film Thickness after Silyl Treatments



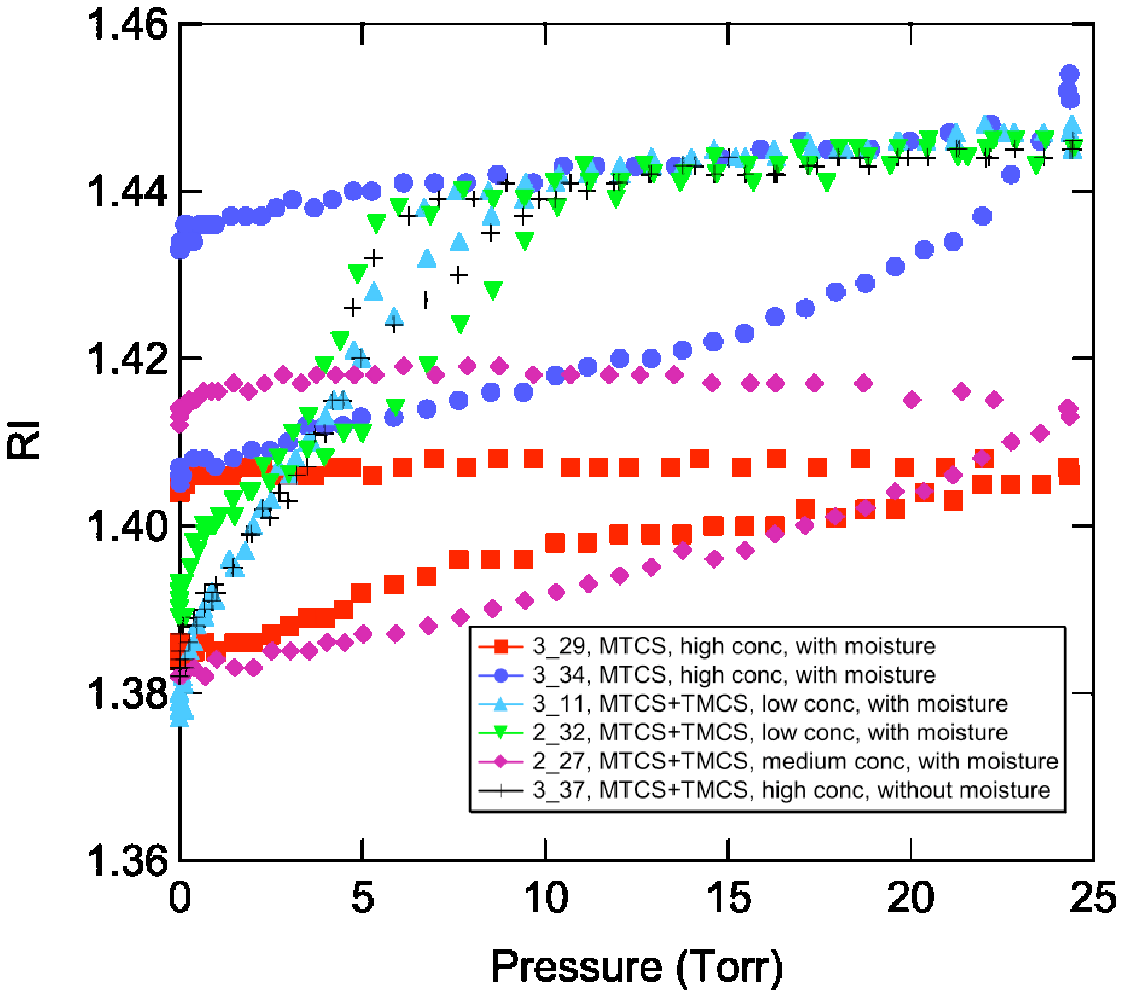
Ellipsometric Porosimetry: HMDS/scCO$_2$

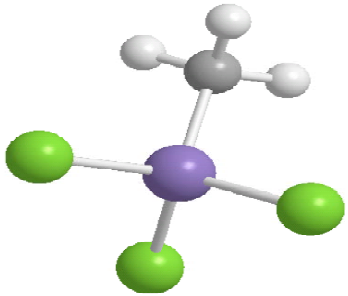




- HMDS/scCO$_2$ sample processed at 204 atm and 58C with a 2 min soak reduced open porosity, but yielded similar pore size distribution.

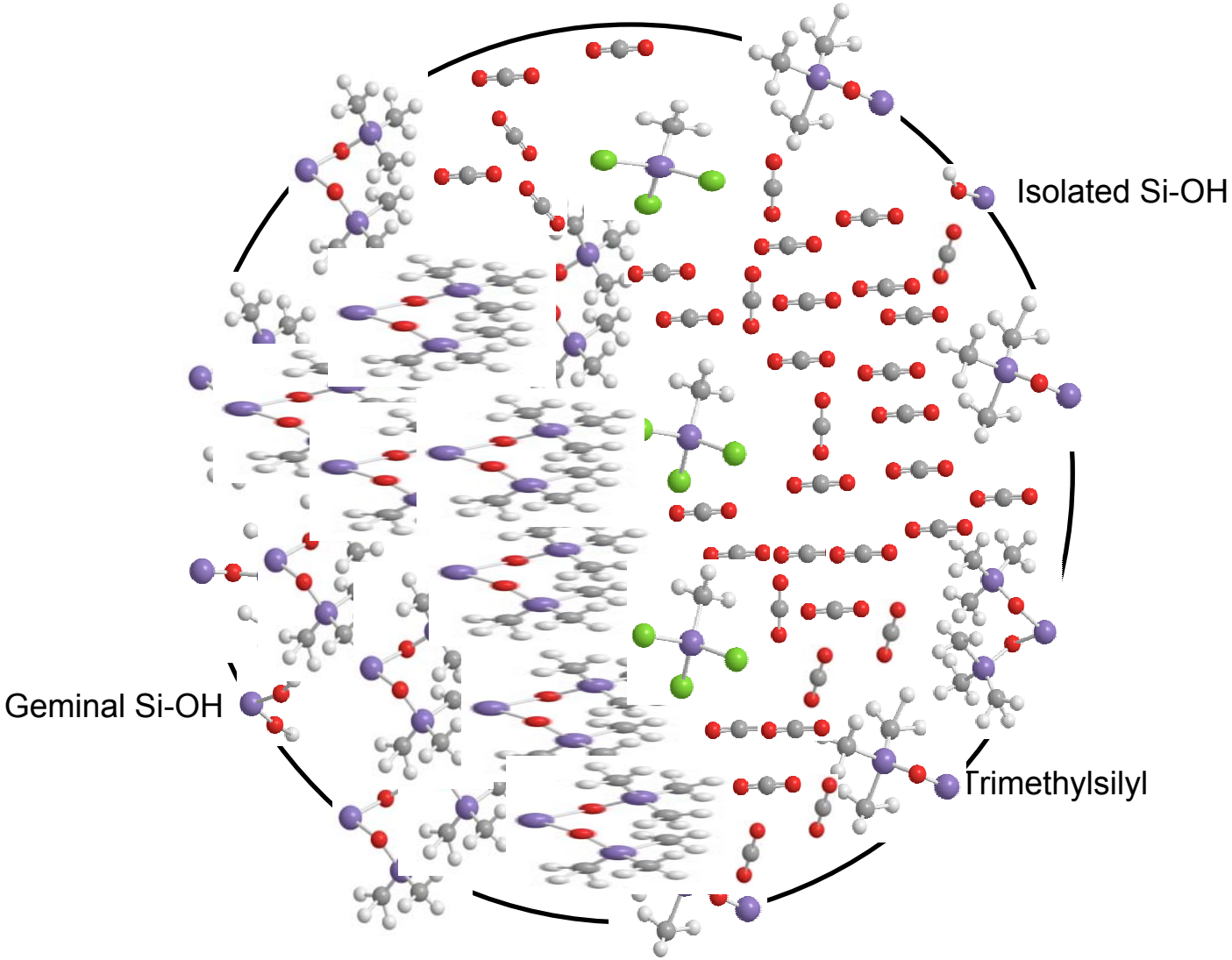
Pore Capping: Ellipsometric Porosimetry (EP)





- Pore capped after MTCS and MTCS followed by TMCS processing with moisture
- Pore not sealed after MTCS followed by TMCS processing without moisture

MTCS/scCO$_2$ Pore Repair



Conclusions

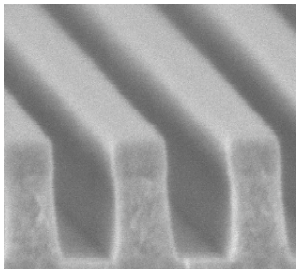
- Increased CH_3, CH_2, and Si-O-Si moieties
- Both isolated/geminal SiO-H and H-bonded SiO-H reacted except for MTCS
- Recovery of hydrophobicity with all silylation chemicals studied
- Both ellipsometry and contact angle results show that TMBS, TMIS, DMDCS, and MTCS exhibit higher reactivity than TMCS
- Restoration of dielectric constant with HMDS, TMCS, TMBS, TMIS, DMDCS, BDMCS, ODMCS, DDMCS, and ODDMCS
- Pores capped after MTCS + TMCS + moisture process based on EP
- Longer time needed for liquid silylation than supercritical silylation

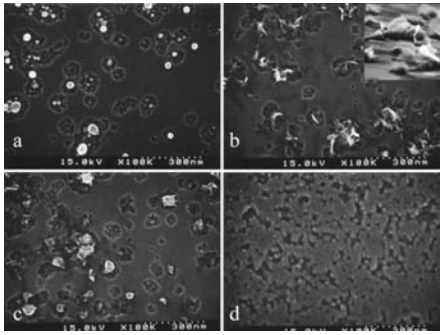
Future Work

- Chemistries
- Patterned p-MSQ films
- Low-*k* materials: microporous vs mesoporous
- Delivery methods

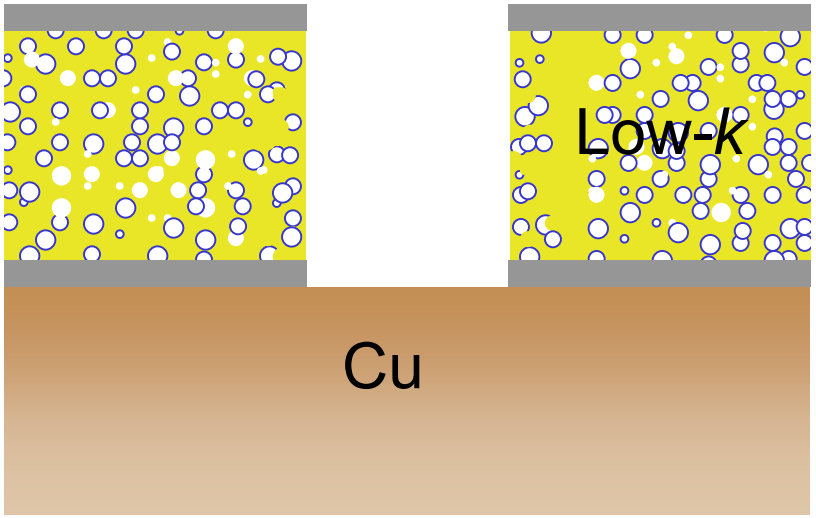
Cu processing in $scCO_2$

- Applications
  - **Cu etching**
  - Cu contamination removal
  - Cu deposition





- Maintain device structure
  - Critical dimensions
  - Etching profile
  - Remove Cu oxides without removing Cu

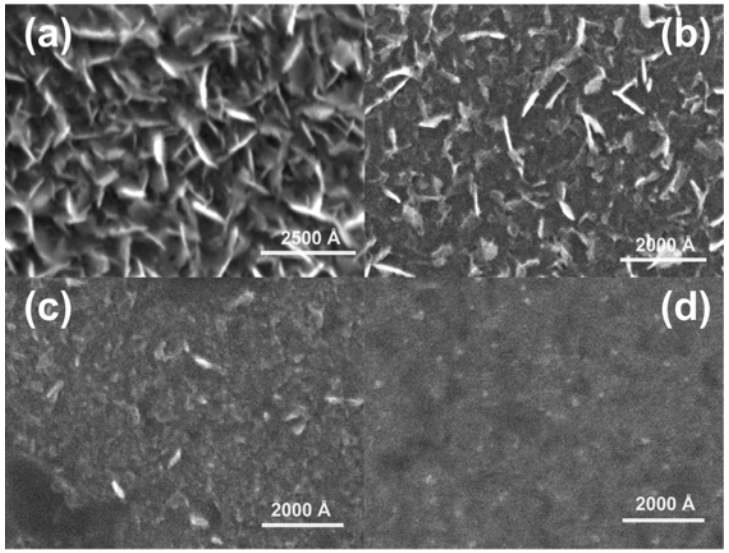


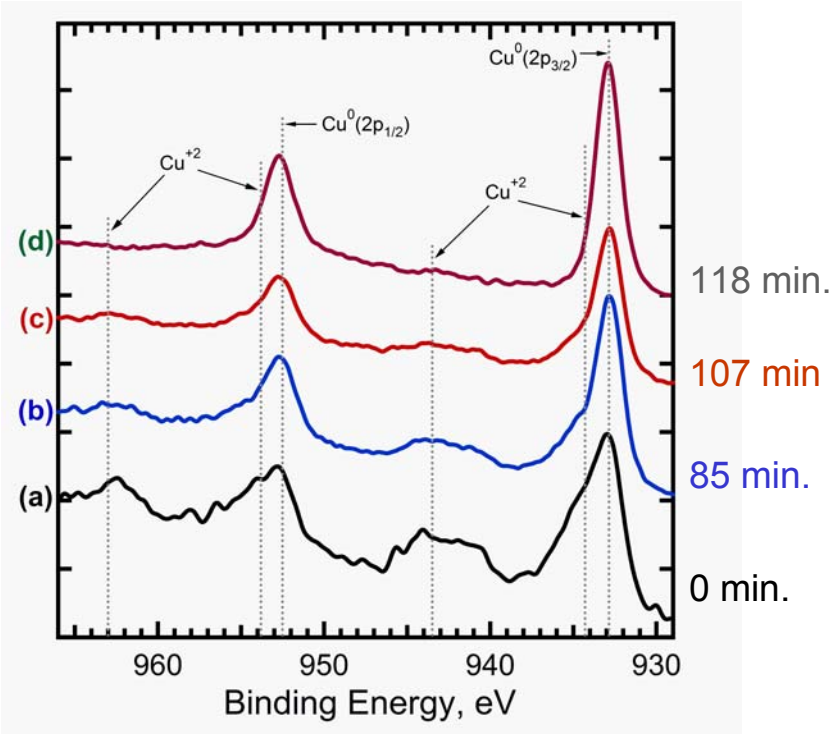
- Materials compatibility
  - low-*k* film
  - Cu interconnects
  - TiN or TaN diff. barriers

- $scCO_2$ integration
  - Inert to low-k dielectrics, metals
  - Penetrate small features
  - Hydrophobic

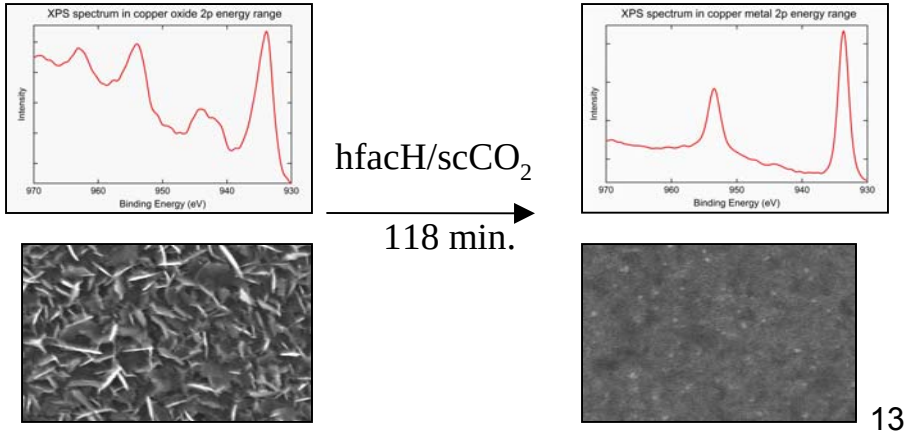
- Processing
  - Low Temperatures (< 100 °C)
  - High Pressures (> 70 atm)
  - Cosolvents/additives

XPS and SEM Analysis





- Exposure to hfacH in $scCO_2$
- CuO on surface is etched away
- Etching rates calculated as function of:
- temperature
- concentration
- additives



Conclusions

- Cu films can be etched using dissolved chelators in $scCO_2$
- Reaction conditions are tightly controlled using custom apparatus
- Etching reaction exhibits Arrhenius temperature dependence
- Reaction order indicates surface inhibition
- Etching rates increase with increasing temperature and concentration of hfacH

Future Work

- Additives/catalysts
- Explore near-critical region
- Other etching chemicals
- Delivery methods

Technology Goals

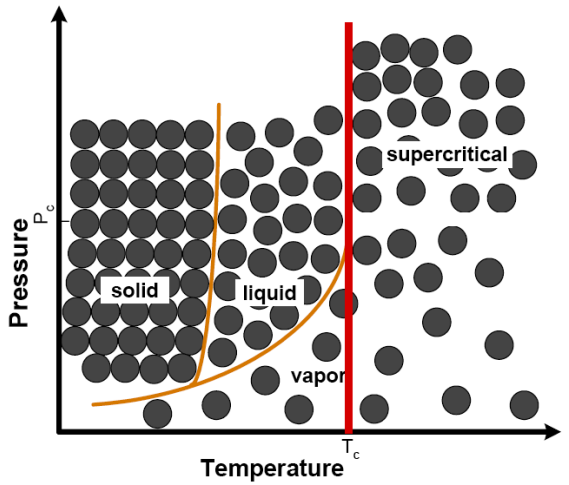
MPU Interconnect Technology Requirements (Table 81b ITRS 2004 update)

Year of production	Technology Node (nm)	MPU/ASIC 1/2 Pitch (nm)	No. of Metal Levels
2010	hp45	54	12
2013	hp32	38	12
2016	hp22	27	14

- Requires **etching, cleaning, and filling** high aspect ratio, sub-50 nm structures.
- Repeated 3-6 times per wafer.
- Increase in complexity of integration because of new material sets and novel structures .

Advanced Cleaning Technology Options

- Liquids
  - Surfactants
  - Etchants
  - Chelators



- Supercritical CO_2
  - Low tension surface
    - Wet any material
    - Penetrate sub-50 nm features
  - Tune solvent strength and function with additives
    - Etchants
    - Chelators

Acknowledgements

- NSF/SRC EBSM Engineering Research Center
  (EEC-9528813/2001-MC-425)

- Sematech
  - Eric Busch (Low-*k* Unit Process Development Program Manager, AMD Assignee)
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  - Frank Weber (Interconnect Division, Infineon Assignee)
  - Todd Rhoad, Process Engineer
  - Brian White, Project Engineer

- Texas Instruments (TI-SRC Custom Research)
  - Phil Matz

- IMEC
  - Toan Le Quoc