Reducing Water and Energy Usage in Patterned Wafer Rinsing

Jun Yan[1], Davoud Zamani[1], Vedhas Pandit[2], Xu Zhang[2], Omid Mahdavi[1]
Bert Vermeire[2] and Farhang Shadman[1]

[1] University of Arizona
[2] Arizona State University

Co-Sponsored by:
Water Sustainability Program (WSP) at UA,
Freescale, and Samsung Electronics

Objective and Approach

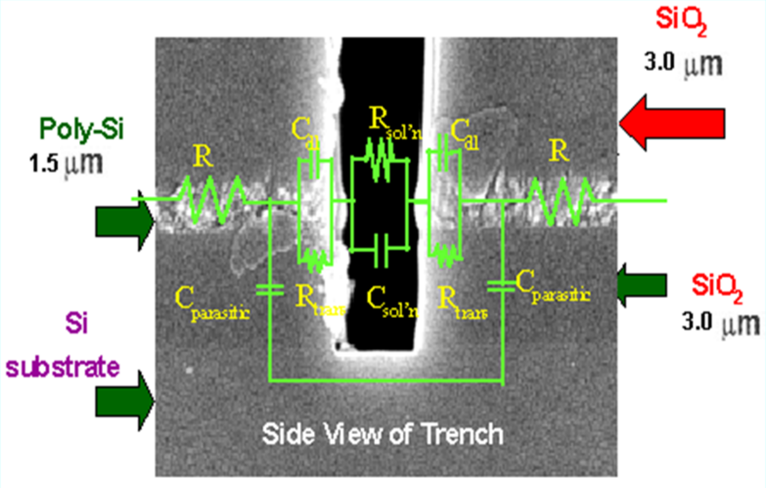
Objective:

- **Investigate the fundamentals of cleaning, rinsing, and drying of micro- and nano-structures; develop new technologies (hardware, process models, and process recipes) to reduce water, chemicals, and energy usage during these processes.**

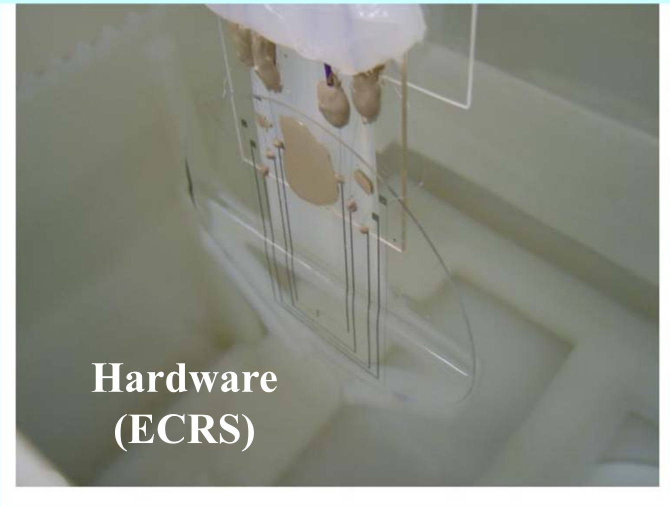
Method of Approach:

- **Apply the novel ECRS metrology method for in-situ and real-time monitoring of the dynamics of batch and single-wafer surface preparation.**
- **Combine metrology with process modeling to identify the controlling steps (bottlenecks) in the cleaning, rinsing, and drying of small structures.**

Background: In-situ Metrology (ECRS)



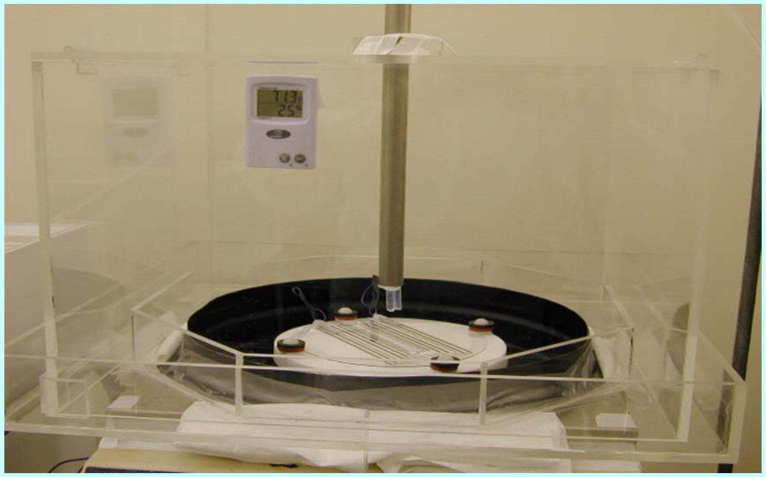
Solution (pH)	UPW (pH=7)	HCl(pH=6)	HCl(pH=5)
Resistivity (MΩ)	18	2.3	0.23
Resolution (ppt)	5	30	400



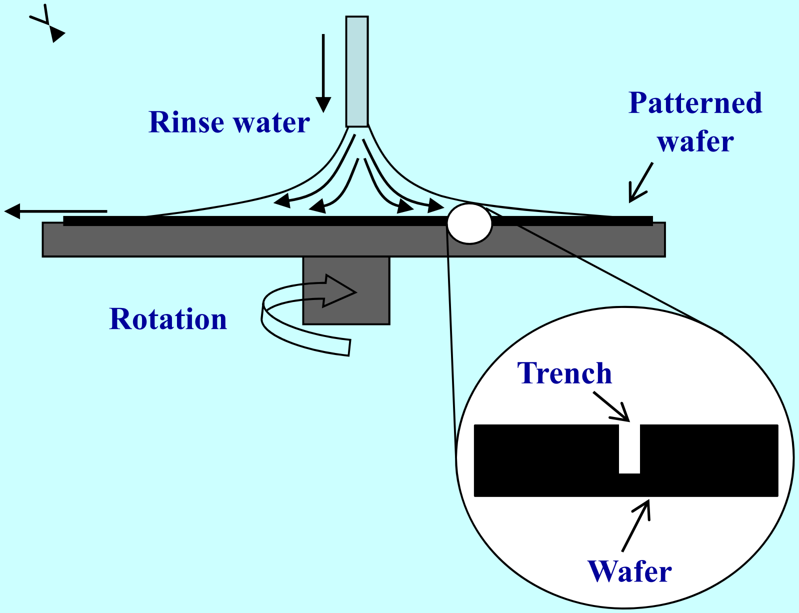
Key Features

- **Real Time**
- **In-situ**
- **Online**
- **High Sensitivity**
- **Non-destructive**
- **Quick Response**

Application of ECRS to Single Wafer Rinsing and Drying



Spin Rinse Testbed



- **A single wafer tool equipped with ECRS is designed and set up.**
- **Combination of experiments and process model is used to study the effect of various process parameters.**

Mathematical Analysis of Spin Rinsing of Patterned Wafer

- Convection
- Surface Charge
- Diffusion
- Surface reaction
- Ionic transport
- Electric field

Multi-component species transport equations :

$$\frac{\partial C_i}{\partial t} = \nabla \cdot (D_i \nabla C_i + z_i F \mu_i C_i \nabla \varphi)$$

Surface adsorption and desorption:

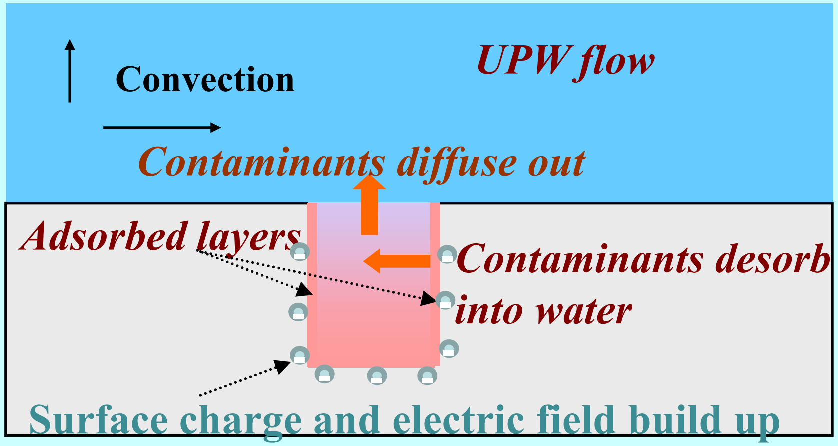
$$\frac{\partial C_{S2}}{\partial t} = k_{a2} C_2 (S_{02} - C_{S2}) - k_{d2} C_{S2}$$

Poisson equation: $\nabla^2 \varphi = -\frac{\rho}{\varepsilon}$

where charge density: $\rho = F \sum_i z_i C_i$

Ohm's law: $\vec{J} = \sigma \vec{E}$ $\qquad \nabla \times \vec{E} = 0$

where electrical conductivity: $\sigma = \sum_i \lambda_i C_i$



Convection

UPW flow

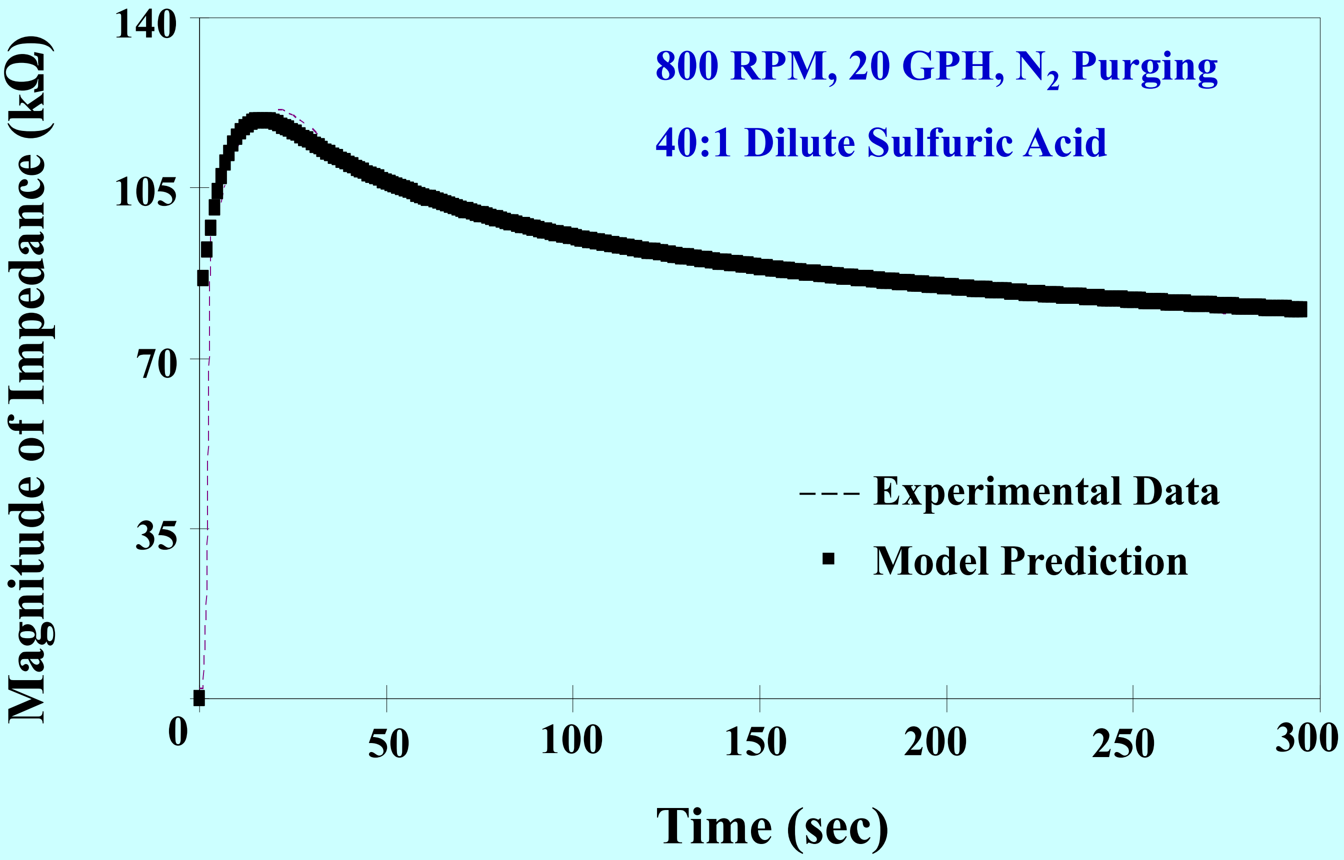
Contaminants diffuse out

Adsorbed layers

Contaminants desorb into water

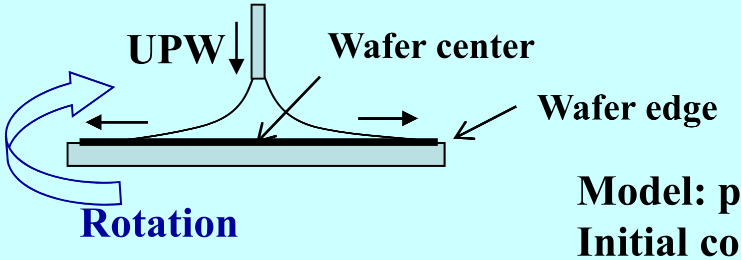
Surface charge and electric field build up

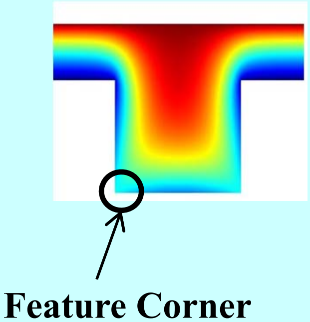
Validation of Process Simulation



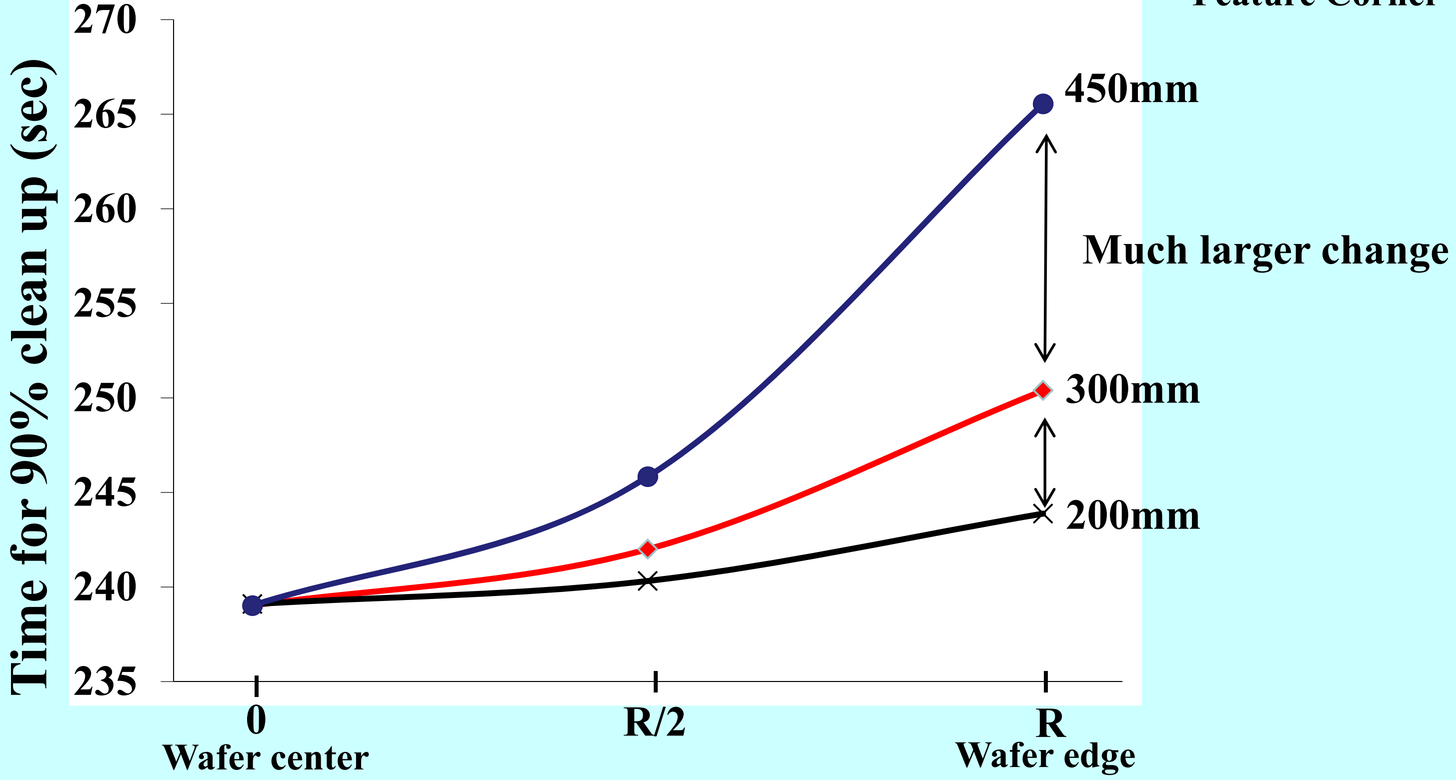
Simulation results are in good agreement with the experimental data

Effect of Wafer Size and Feature Location in Single-Wafer Spin Rinsing



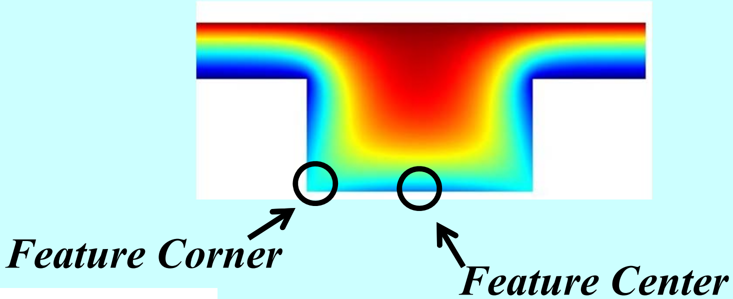


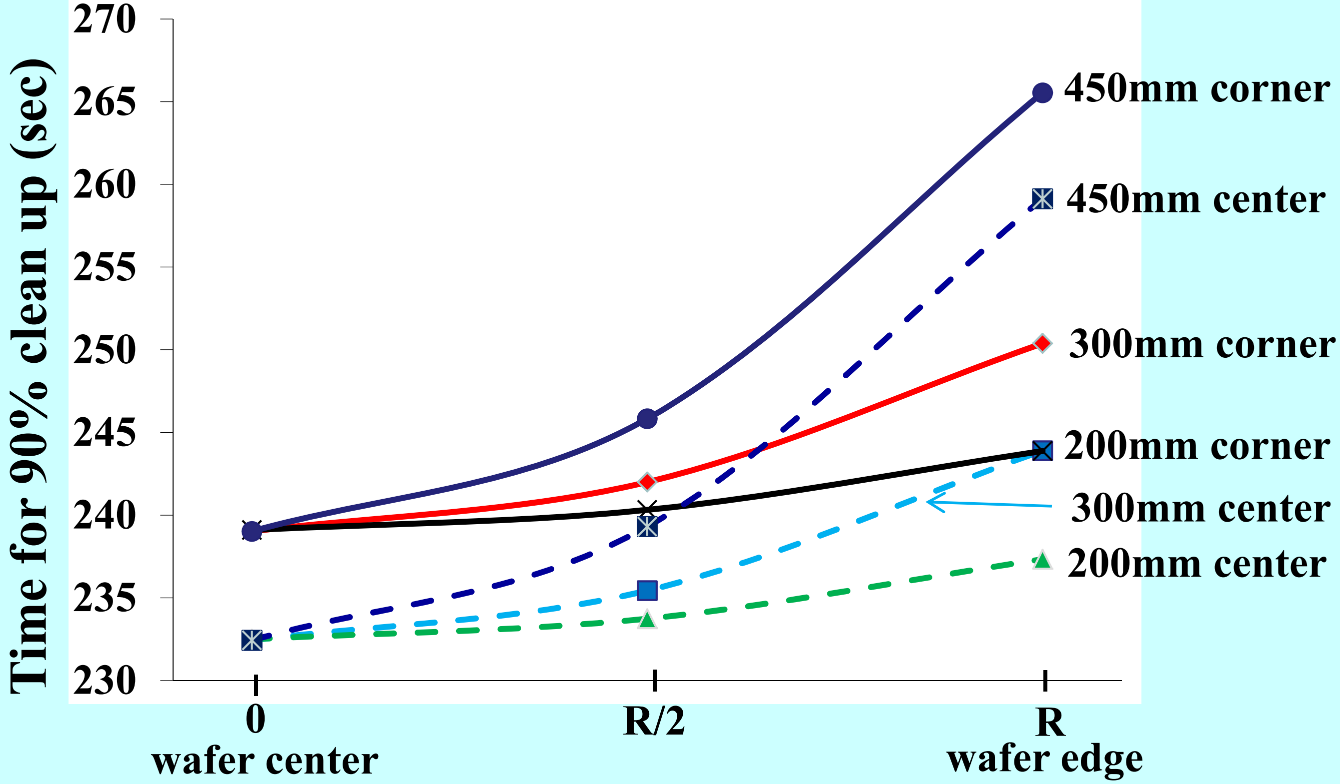
Model: post-etch removal of F$^-$ from HfO_2 surface
Initial concentration: 0.058 mM
Initial surface concentration: 4.21×10^{13} atoms/cm^2



Localized Cleaning Bottlenecks in Single-Wafer Spin Rinsing

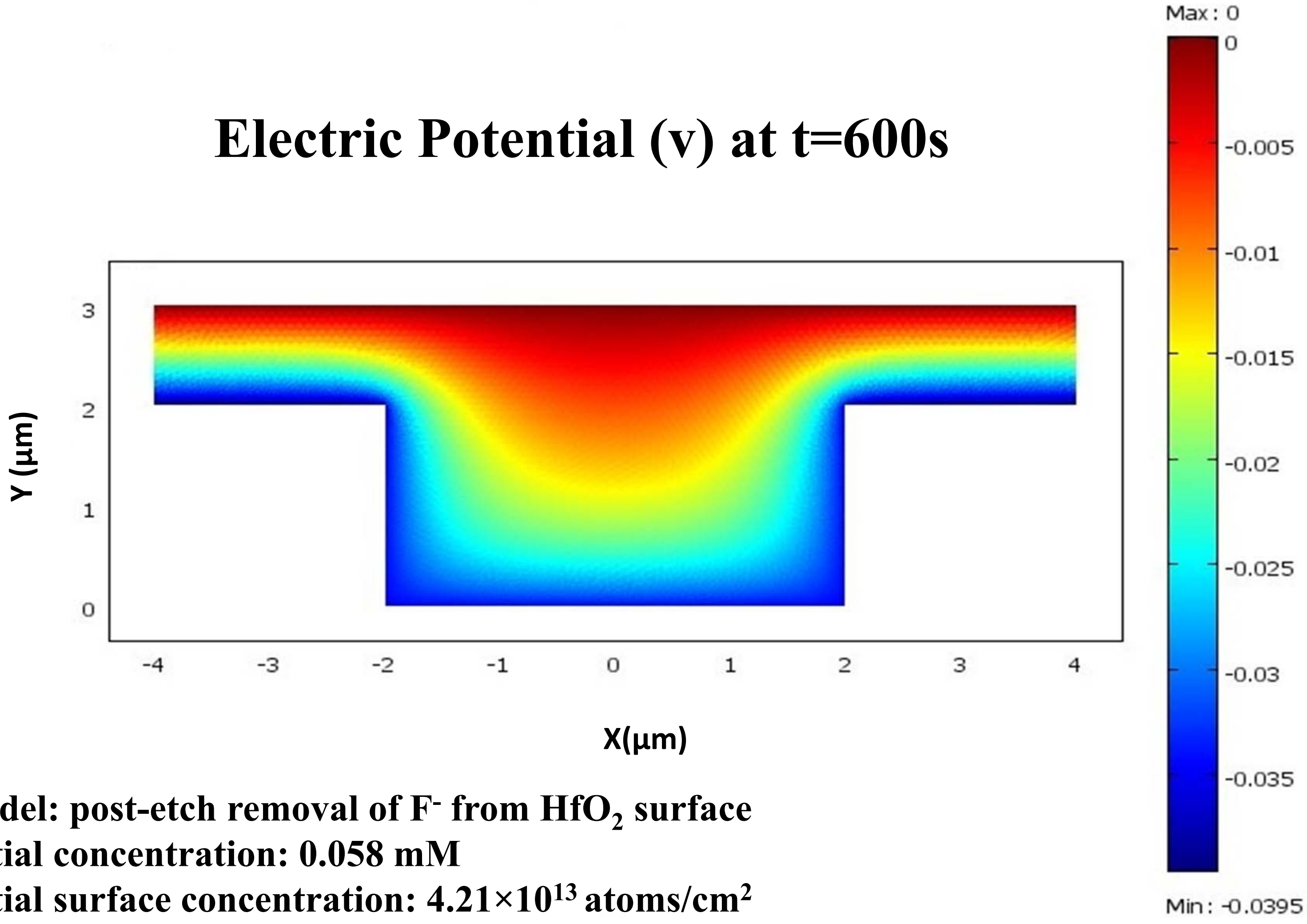
Model: post-etch removal of F^- from HfO_2 surface
Initial concentration: 0.058 mM
Initial surface concentration: 4.21×10^{13} atoms/cm^2





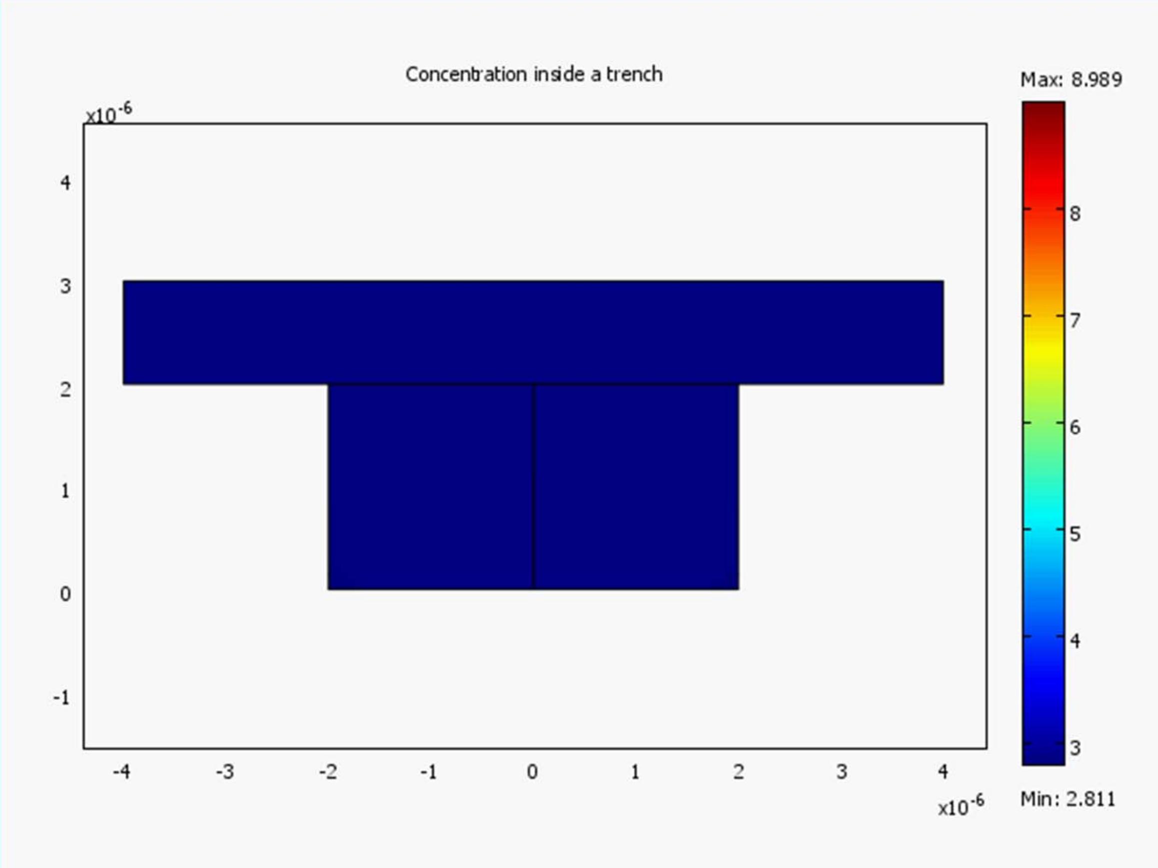
SRC/SEMATECH Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

Electrical Potential Distribution in Features During Single-Wafer Spin Rinsing



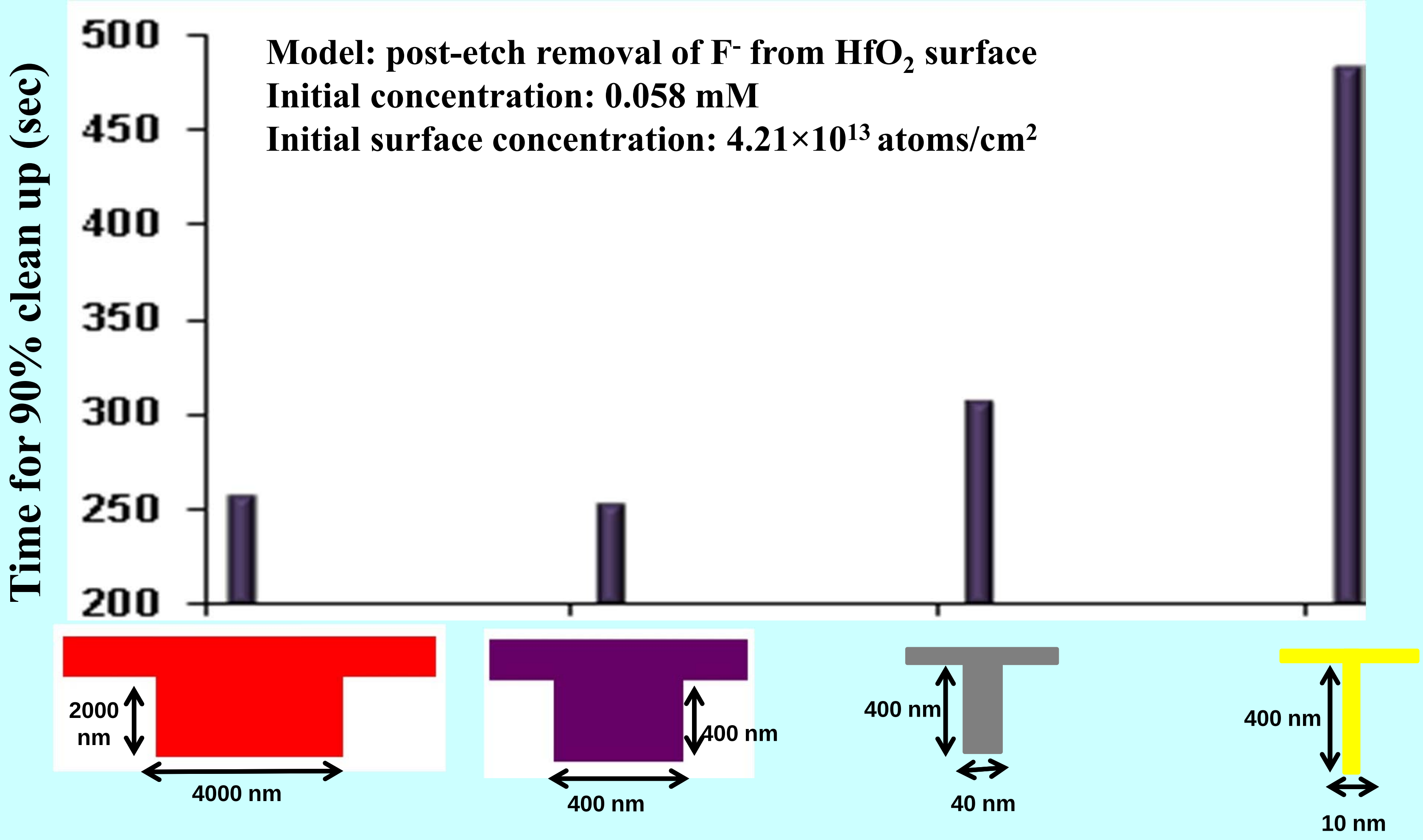
Model: post-etch removal of F^- from HfO_2 surface
Initial concentration: 0.058 mM
Initial surface concentration: 4.21×10^{13} atoms/cm^2

Dynamic Simulation of F^- Inside a Trench During Single-Wafer Spin Rinsing



Model: post-etch removal of F^- from HfO_2 surface
Initial concentration: 0.058 mM
Initial surface concentration: 4.21×10^{13} atoms/cm^2

Effect of Feature Size in Single-Wafer Spin Rinsing

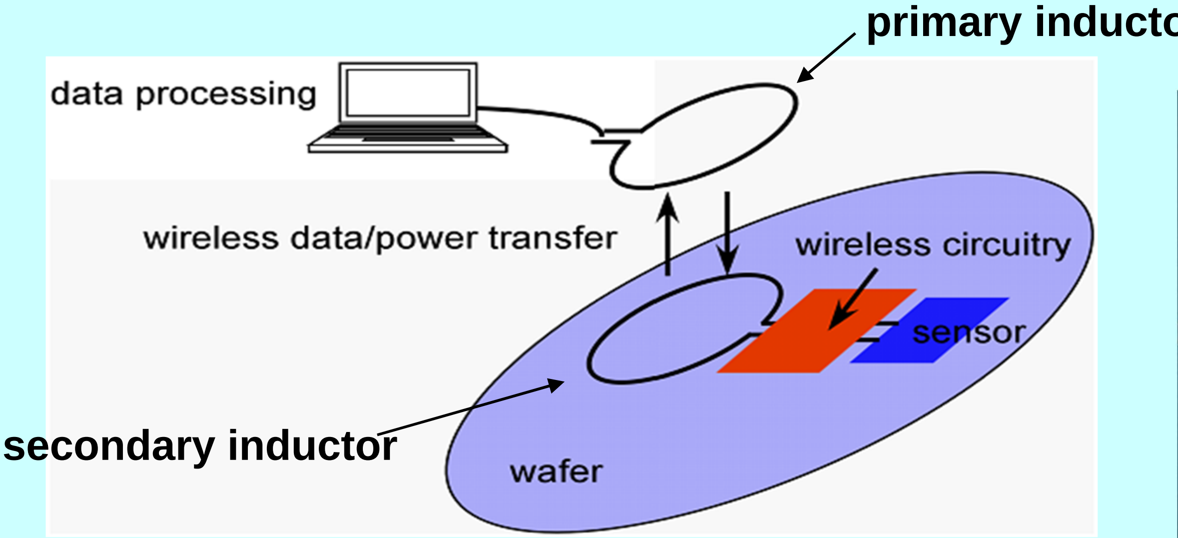


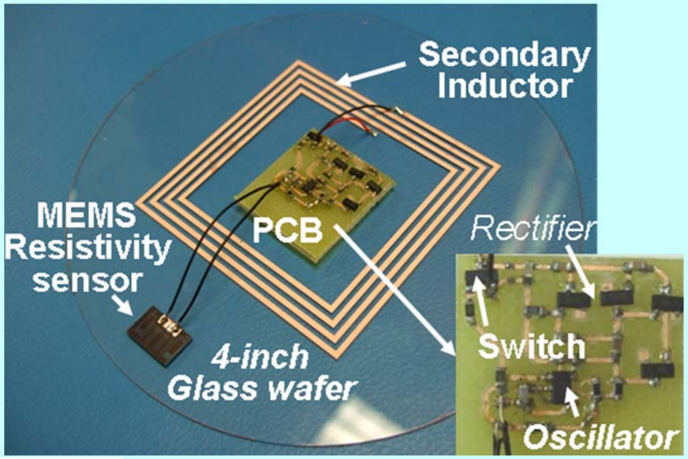
Model: post-etch removal of F^- from HfO_2 surface
Initial concentration: 0.058 mM
Initial surface concentration: 4.21×10^{13} atoms/cm^2

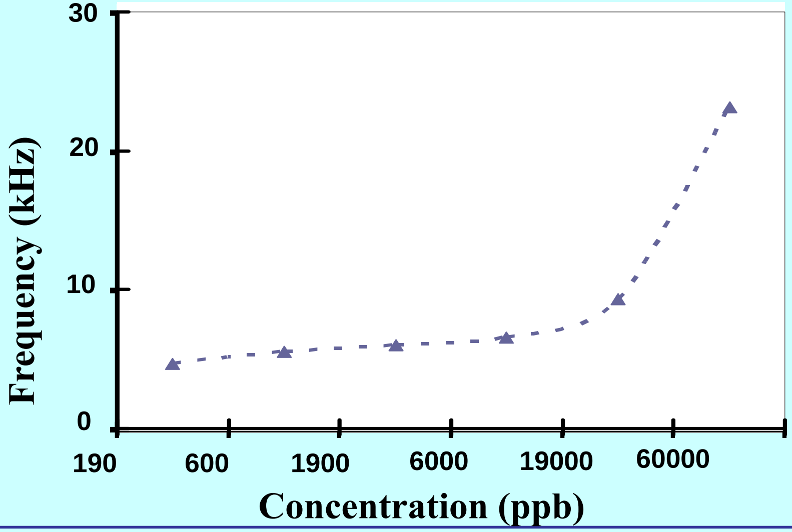
SRC/SEMATECH Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

Remote Measurement of ECRS Impedance

Inductive coupling wireless ECRS

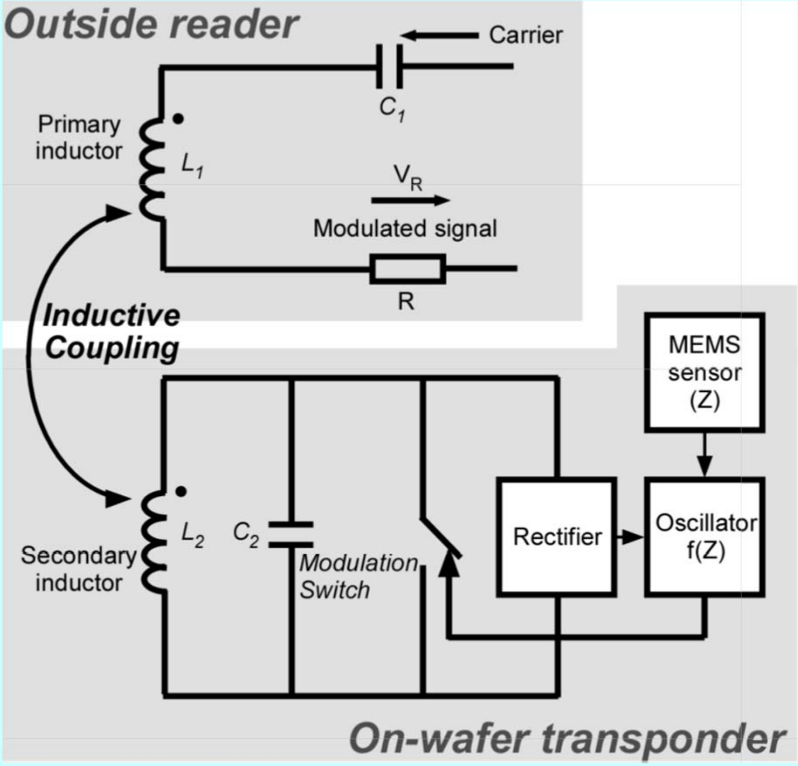






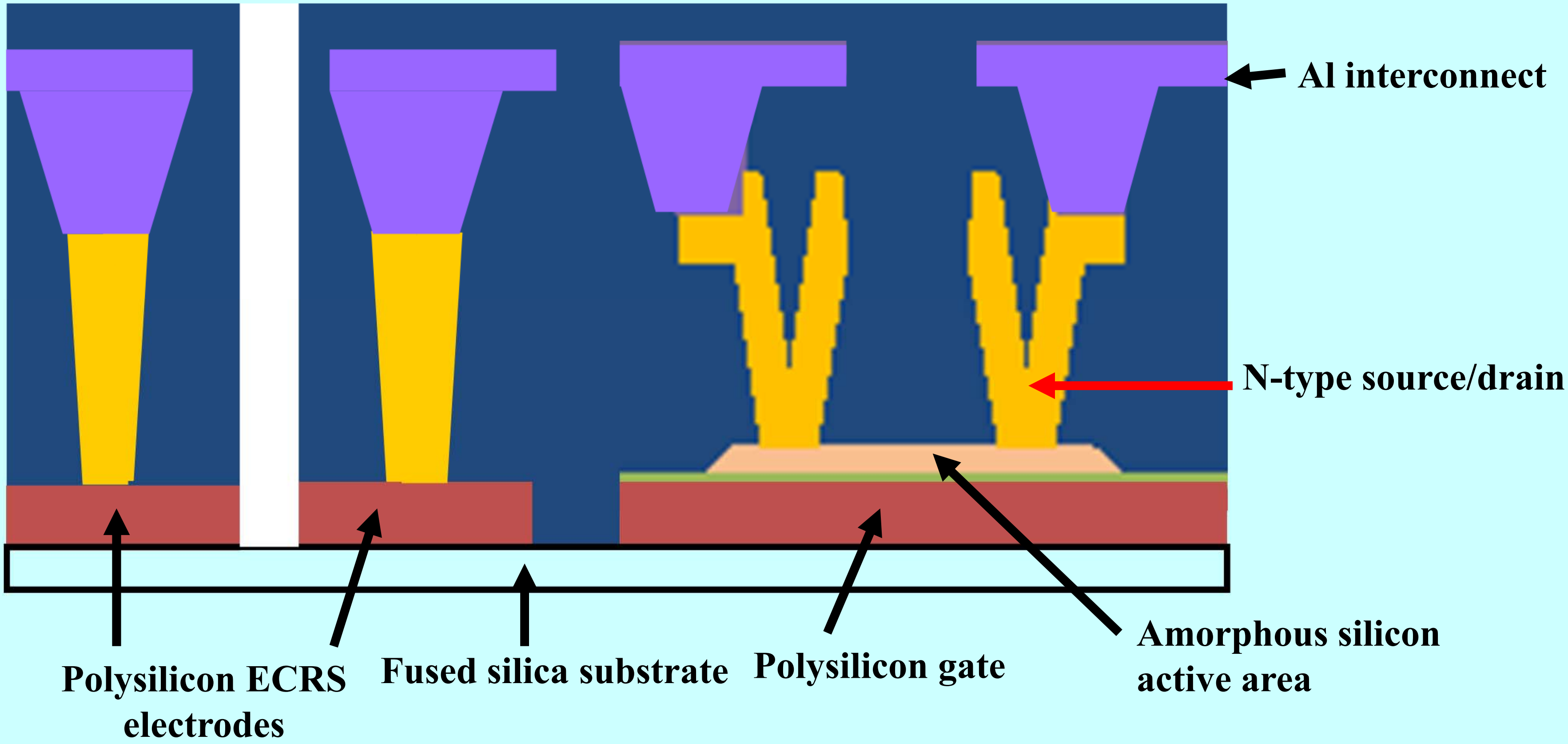
Integrated Wireless ECRS

Technology Requirements



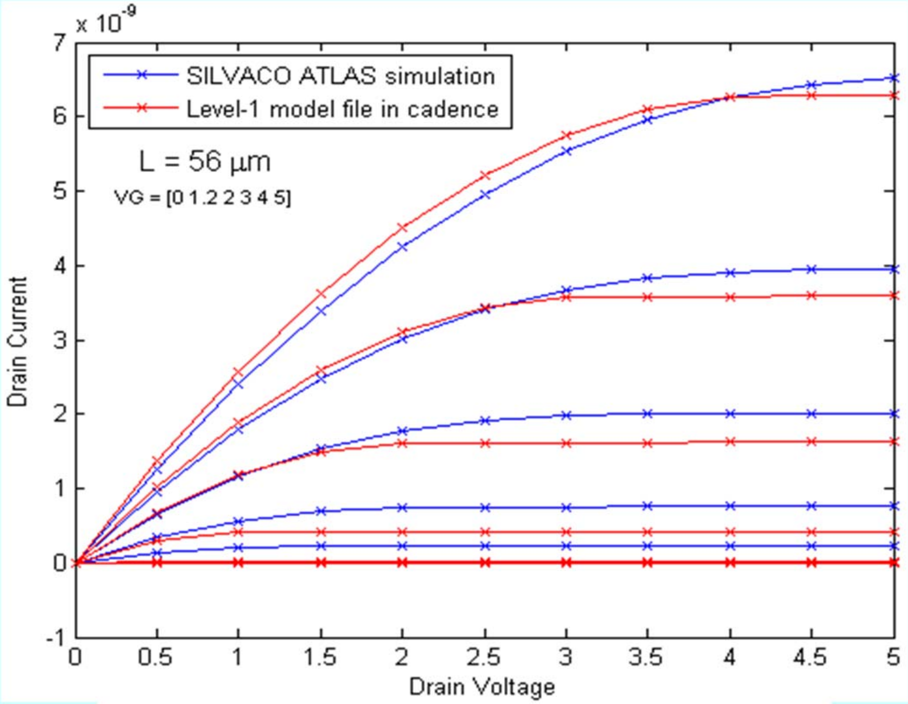
- Compatibility with sensor manufacturing and performance
- Form factor (wafer size and thickness)
- Compatible with processing environment (cleaning tools and chemicals)
- Low cost
- Low power

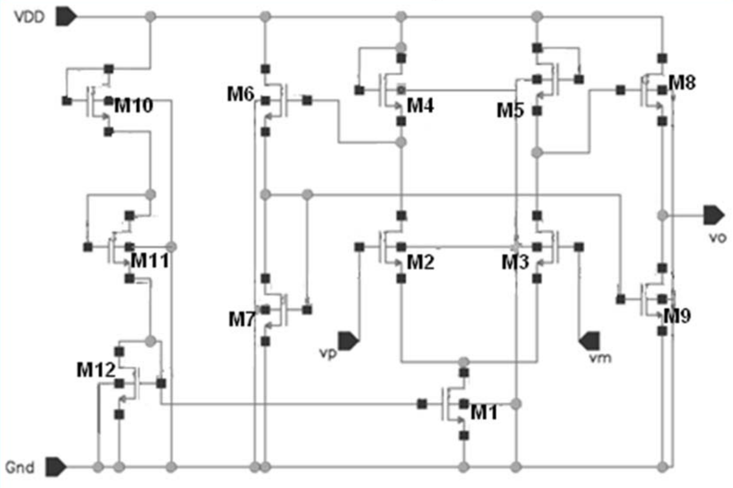
Amorphous Silicon FD-SOI nMOS and ECRS fabricated on Same Substrate



Development Flow

- Device simulations
- Transistor Spice model development
- Basic circuit design (power regulation, oscillator)
- Test-mask design
- Fab and test





Summary

- Applied ECRS to post-etch rinsing of high-k structures; the effects of key process parameters, including the speed of rotation, flow rate, water temperature, feature size, and wafer size were investigated.
- Determined the bottleneck of the rinse process and methods to detect the rinse end point. This is critical in minimizing the usage of water and energy required for rinse.
- A concept for the wireless version of ECRS is developed based on RFID technology. The prototype, using inductive coupling technology, has been designed and fabricated.
- Wireless ECRS tests proved successful transmission of both power and signal.
- Fully integrated ECRS has been designed.

Publications and Presentations

- K. Dhane, J. Han, J. Yan, O. Mahdavi, D. Zamani, B. Vermeire, and F. Shadman, "Dynamics of Cleaning and Rinsing of Micro and Nano Structures in Single-Wafer Cleaning Tools," IEEE Transactions on Semiconductor Manufacturing, 24 (1), 125, 2011
- X. Zhang, J. Yan, B. Vermeire, F. Shadman, and J. Chae, "Passive Wireless Monitoring of Wafer Cleanliness During Rinsing of Semiconductor Wafers," IEEE Sensors Journal, 10 (6), 1048, 2010.
- J. Yan, D. Zamani, O. Mahdavi, and F. Shadman "Application of a novel on-line metrology technique to reduce water and energy usage during surface preparation of patterned wafers in single-wafer tools" Submitted to TECHCON 2011, Austin , Texas
- Jun Yan, "Water Usage Reduction and Water Reuse in Semiconductor manufacturing", the Second International Congress on Sustainability Science and Engineering, Water Re-Use Workshop, January 14, 2011, Tucson, Arizona, USA (Invited Presentation)

Industrial Interactions and Technology Transfer

- **Interactions with Freescale Semiconductor (Hsi-An Kwong, Andrew Hebda, Steve Schauer , Wei Liu, and Marie Burnham) for high-efficiency rinse recipe development and demonstration.**
- **Interactions with ASM America(Shawn Thomas and Tracy Irving) for high-efficiency rinse recipe development and demonstration**