ERC Annual Meeting
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Academia / Industry Partnership to Enhance Research in Energy & Sustainability for next generation High Volume Nano Manufacturing

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Acknowledgements: Josh Walden, Gopal Rao, Prof Farhang Shadman

Summary

➢ ERC's Success Story

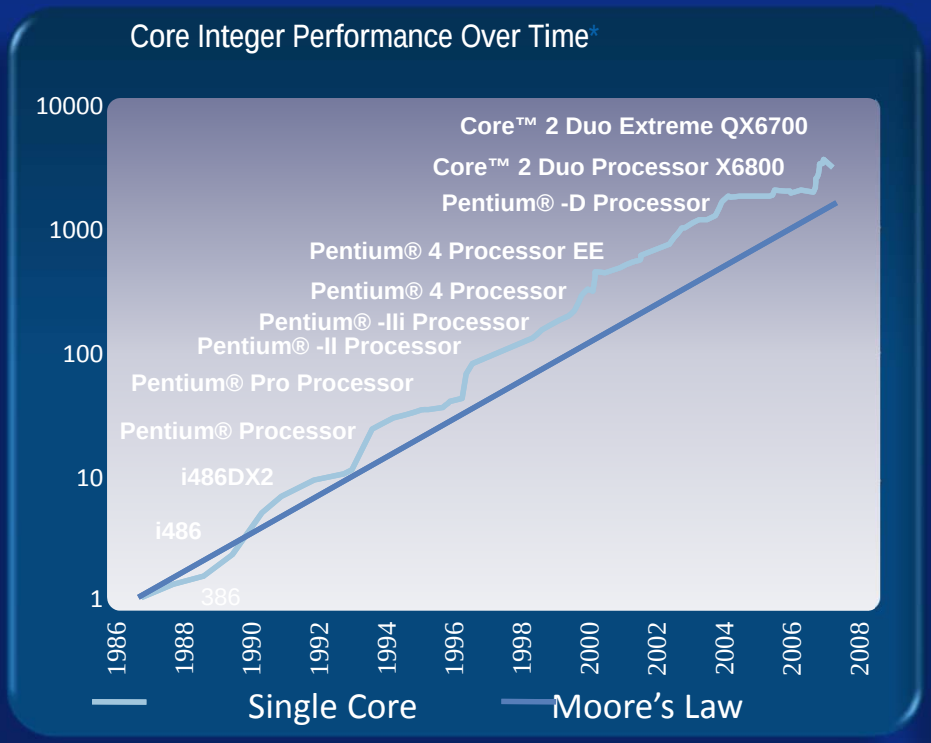
- ERC has been a pioneer in initiating research that is helping make Semiconductor manufacturing more environmentally friendly
- ERC/Intel Customized Research Program has been a win-win relationship
  - Excellent quality of research
  - Dedicated PIs and Students (Some of them have are now working in Intel)
  - Joint partnership enabled successful implementation of research results

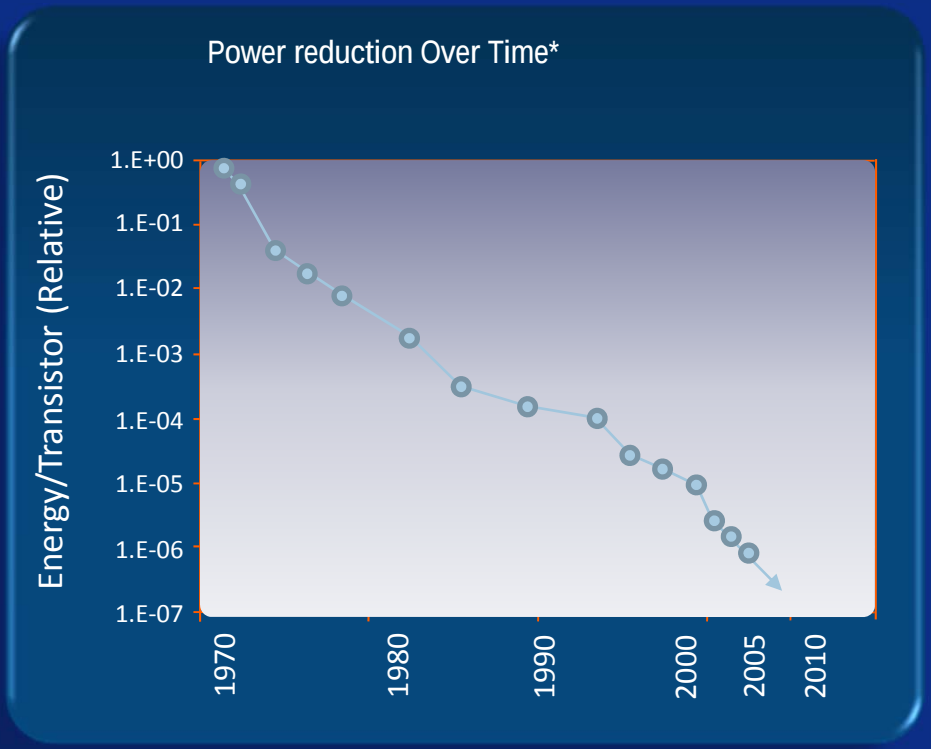
➢ Big Challenges / Big Rewards in Energy & Sustainability

- Major transitions (technologies and regulations) in the Semi industry are driving R&D in Energy & Sustainability
- Focused effort needed to address many challenges
- Enable the US to establish its manufacturing & environmental leadership
- ERC is the right place to facilitate this effort

Recommendation:
ERC/Intel Steering Committee (Chairs: Farhang Shadman/Gopal Rao) to establish an Energy & Sustainability research roadmap that is comprehensive and enables Industry/Academia collaboration.

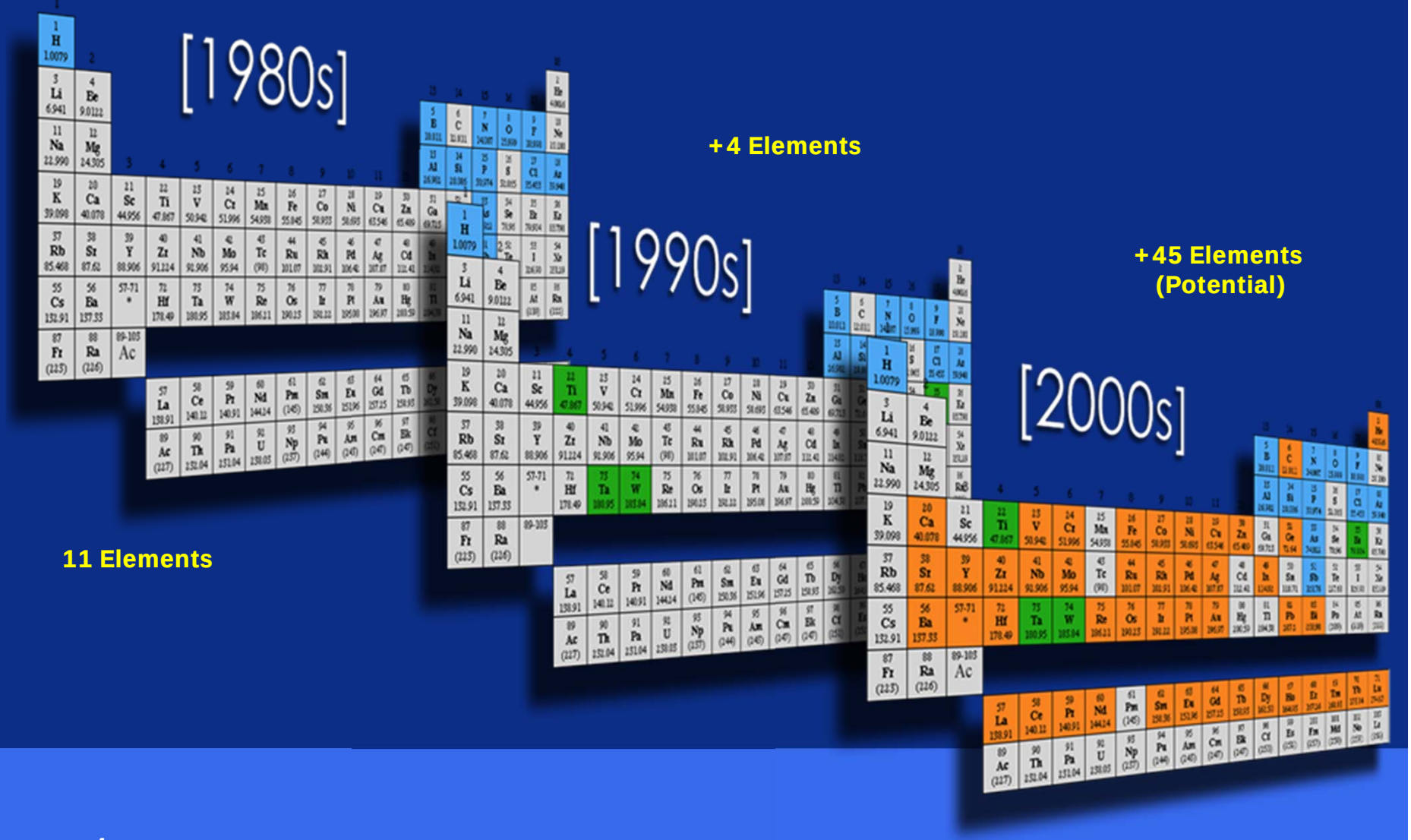
Moore's Law pushes performance and power reduction



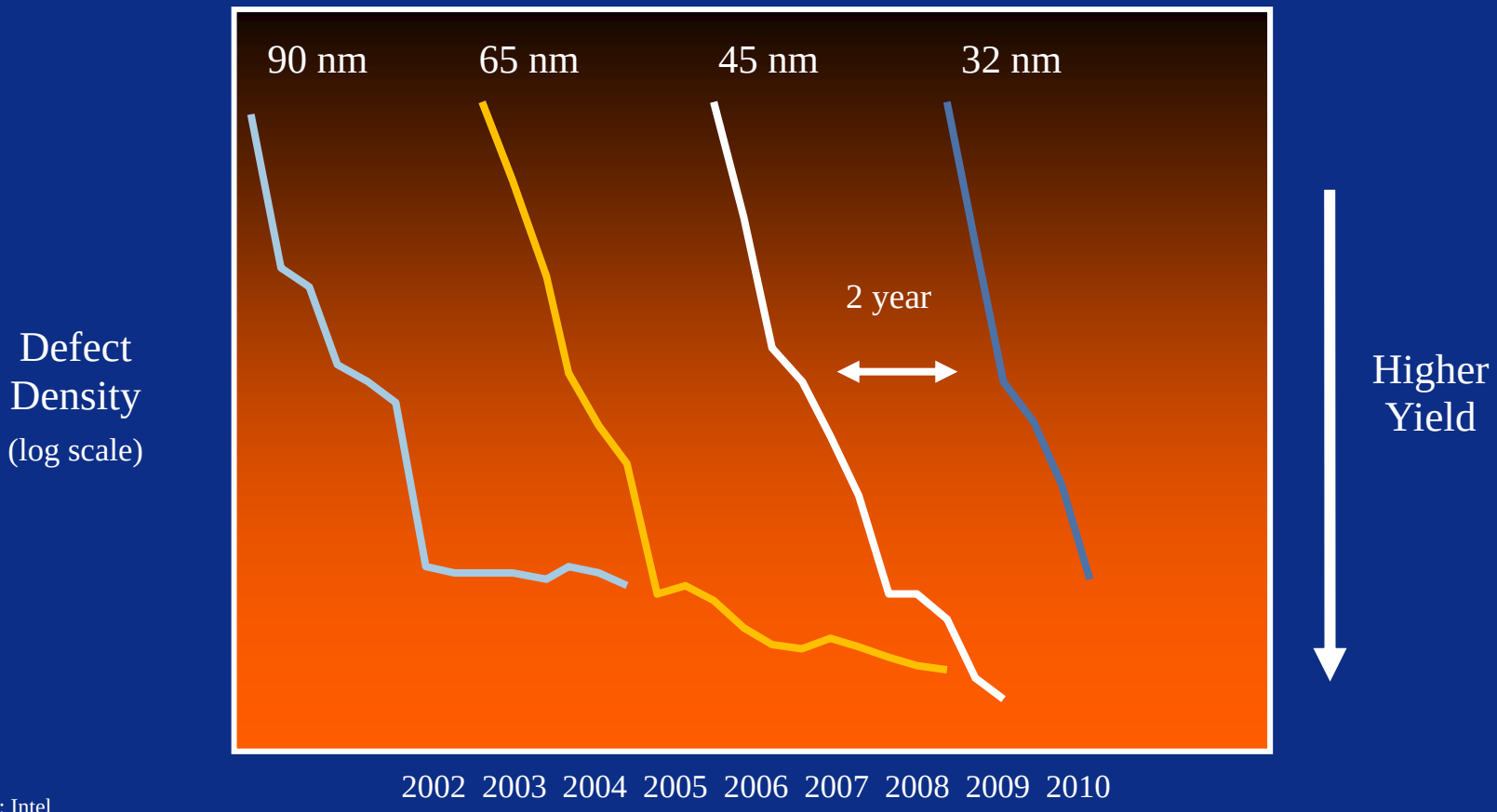


Each transistor in Intel's newest 45 nanometer processors uses 1/7000th of the power compared to our earliest transistors. If automobile fuel efficiency had improved at the same rate, today's cars would get ~100,000 miles per gallon.

Si Technology:
Exponentially Increasing Complexity



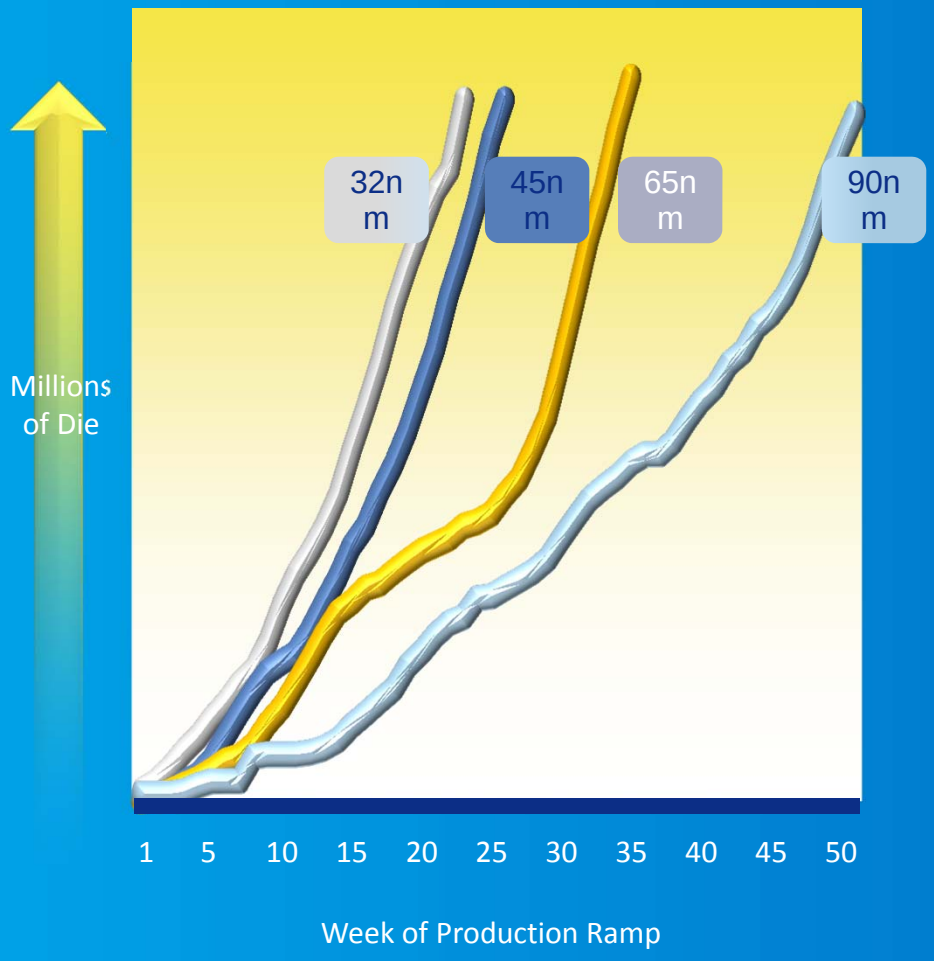
Technology innovation on a reliable and predictable timeline



Source: Intel

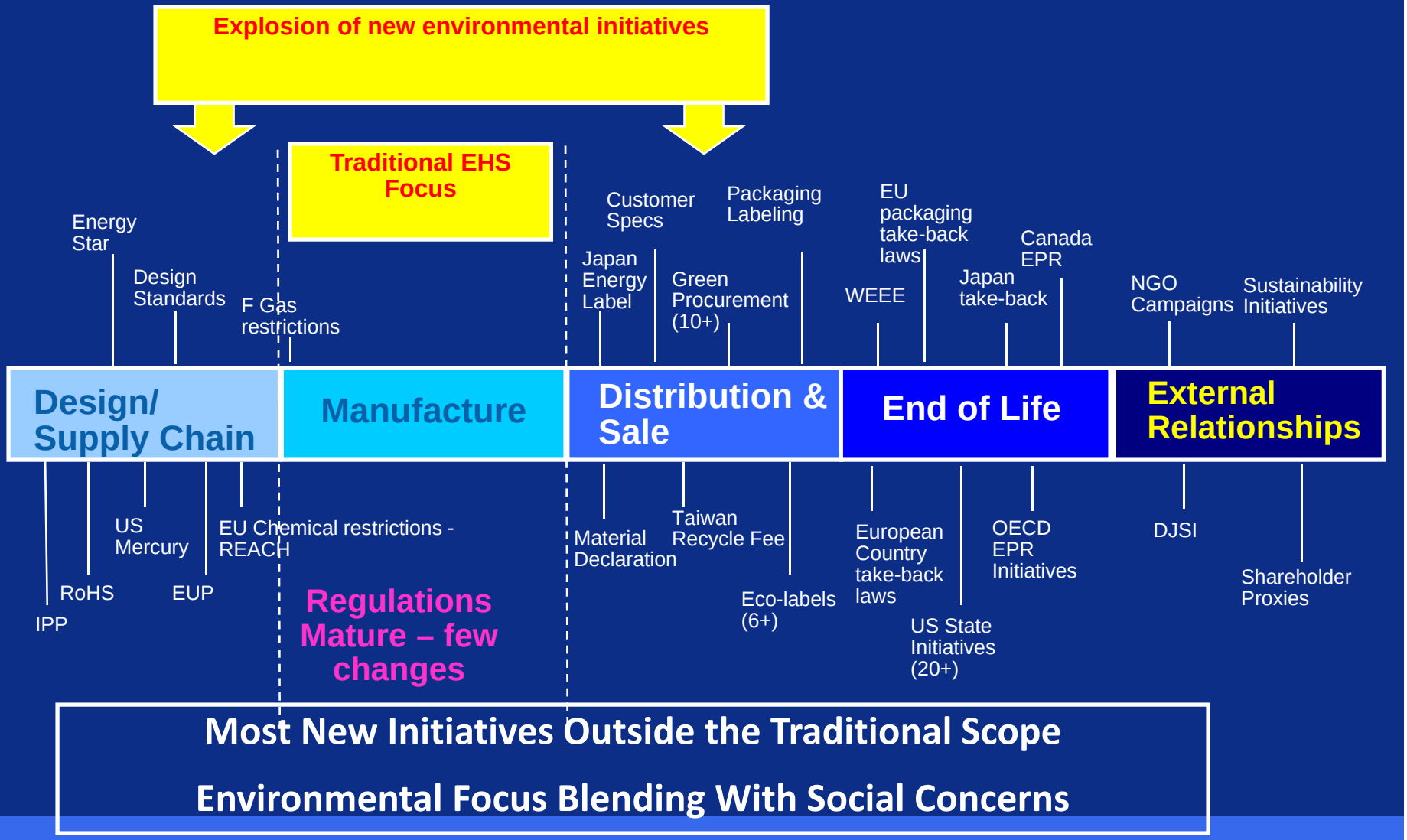
Continually improving complex technologies requires extraordinary collaboration

Faster Ramps with Each Generation



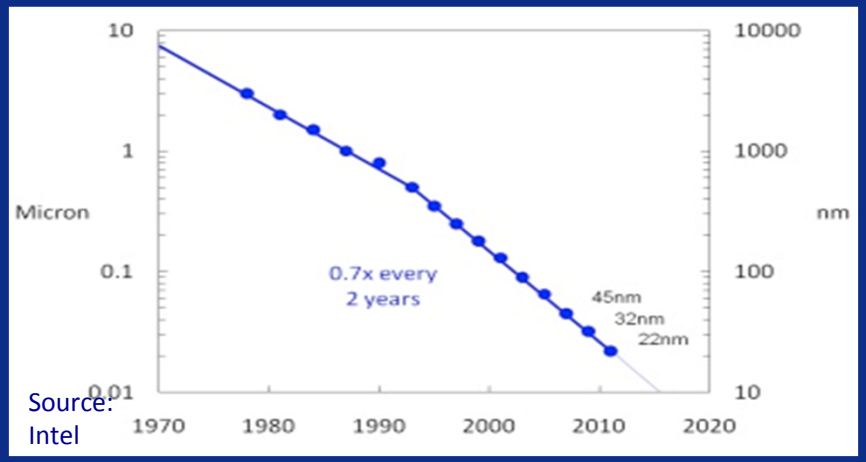
>50%
Reduction In Time to Ramp from 90nm to 32nm

Mega-Trend: Moving Beyond the Traditional Focus



Major Transitions in Semiconductor Technology

Drivers for Research in Energy/Natural Resource Conservation



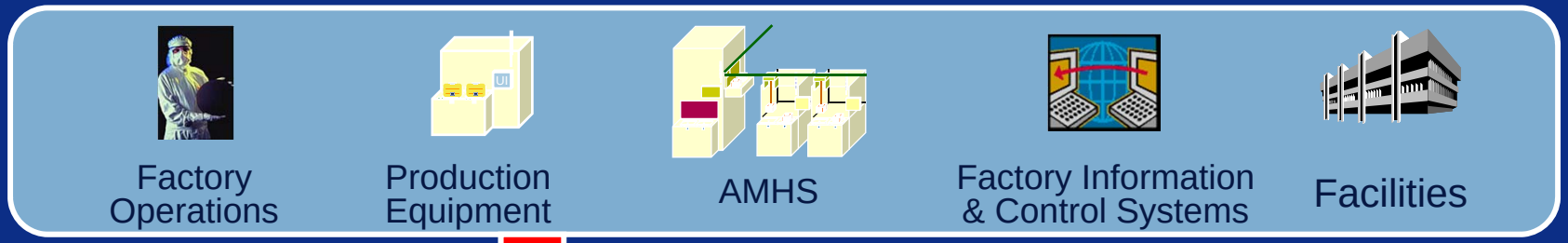
Moore's Law: Transistor dimensions scale to improve performance, reduce power and reduce cost per transistor

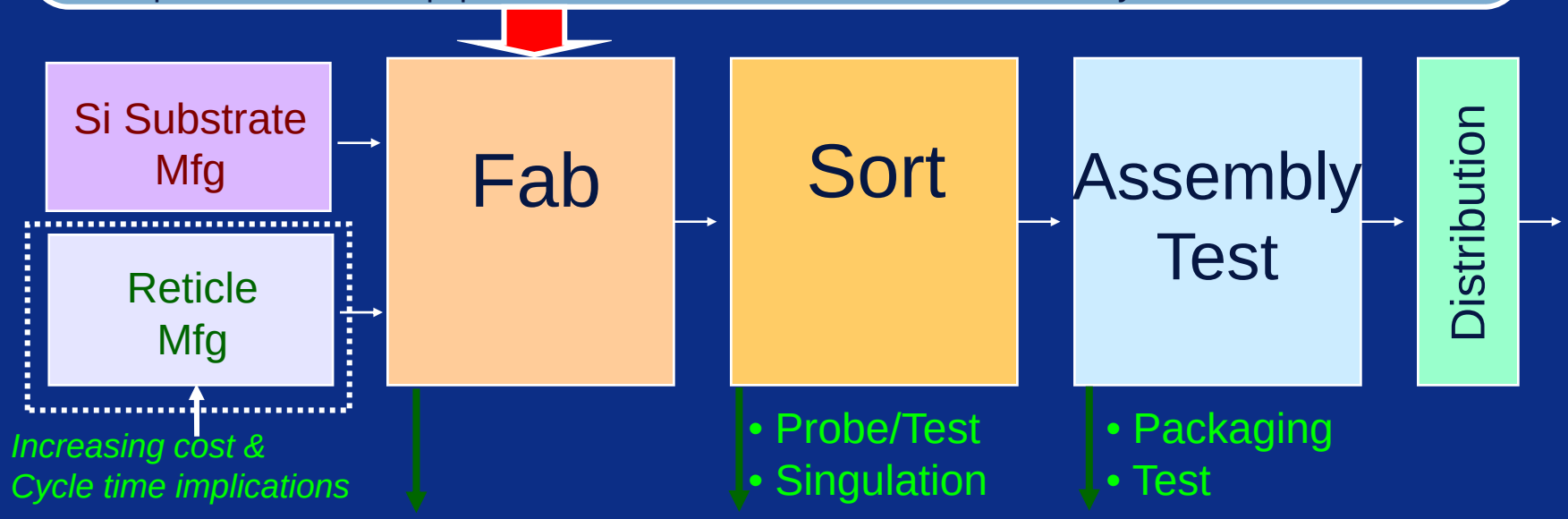
- Device Technology
  - Scaling
  - Beyond CMOS
- New Materials
  - Carbon Nanotubes/wires
- Wafer Size: 300mm to 450mm
  - New Equipment/Systems/Automation/Facilities
- Lithography: EUV
  - New Litho process technology
  - New Equipment/Mask/Systems
- New Regulations

Need Academia/Industry Partnership to Study Energy & Natural Resource Conservation

								New Fabs	**Green Fabs**
								Scaling	**Factory Ops/Yield /Quality**
							New Materials	**EHS Impact / New Regulations**	
						Major Si/Tool Changes	**Energy Management Challenge**		
Current HVM Base	**Diffusion**	**Deposition**	**Etch**	**Litho**	**Cleans**	**AMHS**	**Implant**	**Facilities**	**Data Center**

Factory Scope and Drivers





Factory is driven by Cost, Quality, Productivity, and Speed

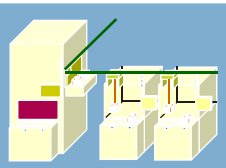
- Reduce factory capital and operating costs per function
- Faster delivery of new and volume products to the end customer
- Efficient/Effective volume/mix production, high reliability, & high equipment reuse
- Enable rapid process technology shrinks and wafer size changes

Energy Conservation Efforts in Wafer Manufacturing will impact positively the entire supply chain

Energy Distribution in a Fab

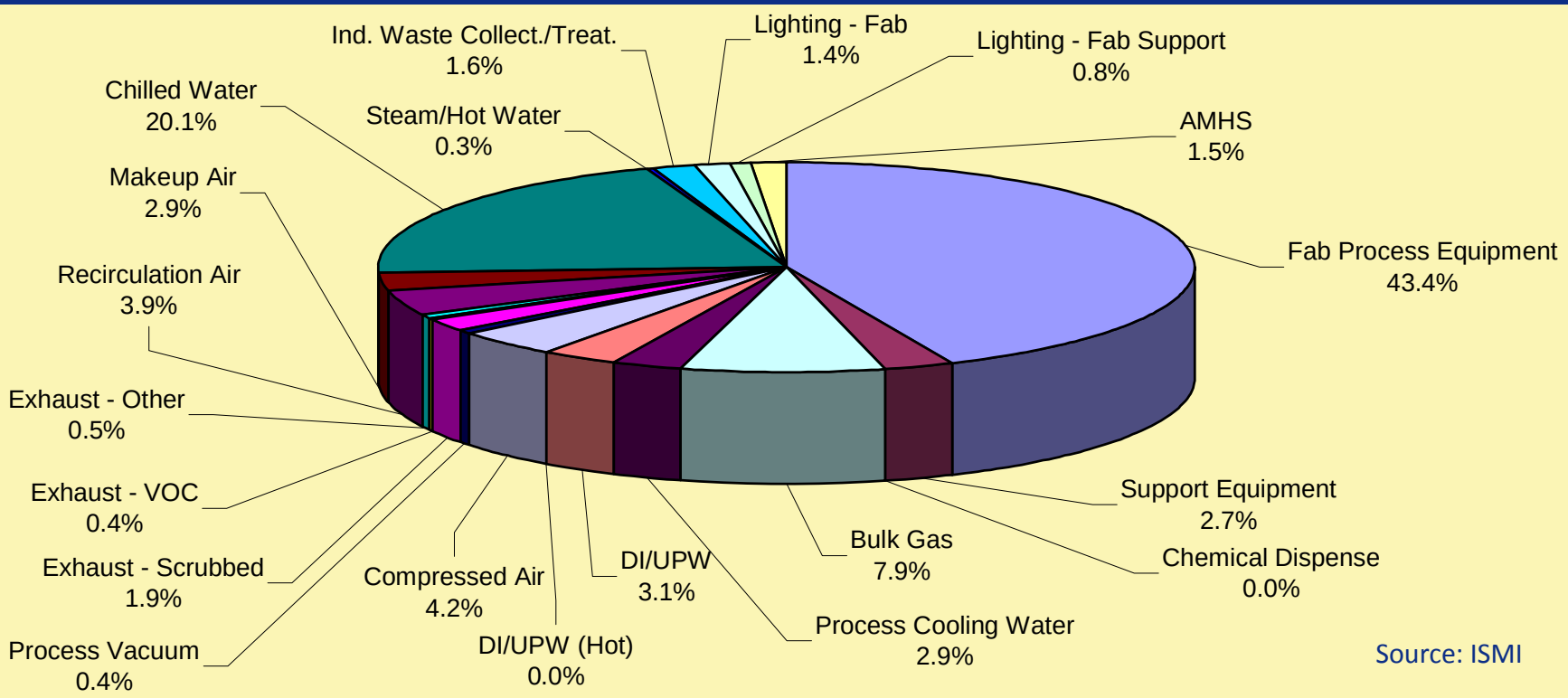

Factory Operations


Production Equipment


AMHS


Factory Information & Control Systems


Facilities



Intel's 2011 Vision and Global Strategy

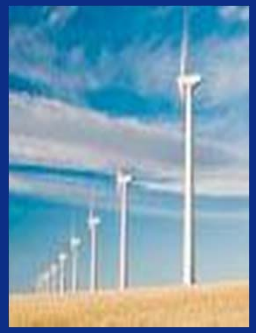
In the coming decade, we will create and extend computing technology to connect and enrich the lives of every person on earth.

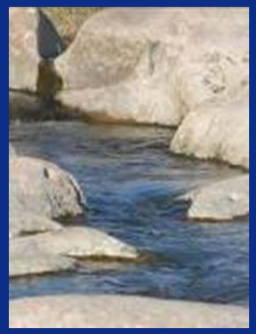
We will build these experiences by innovating around three pillars of computing: energy efficient performance, security, and connectivity.

We will also care for our people, the planet and inspire the next generation of innovators.

Our Sustainability Strategy:
Develop technology solutions to address major global problems while reducing our environmental impact

2012 Intel Environmental Goals





Reduce absolute global-warming gas footprint by 20% by 2012 from 2007 levels.

Reduce energy consumption per chip 5% per year from 2007 through 2012.

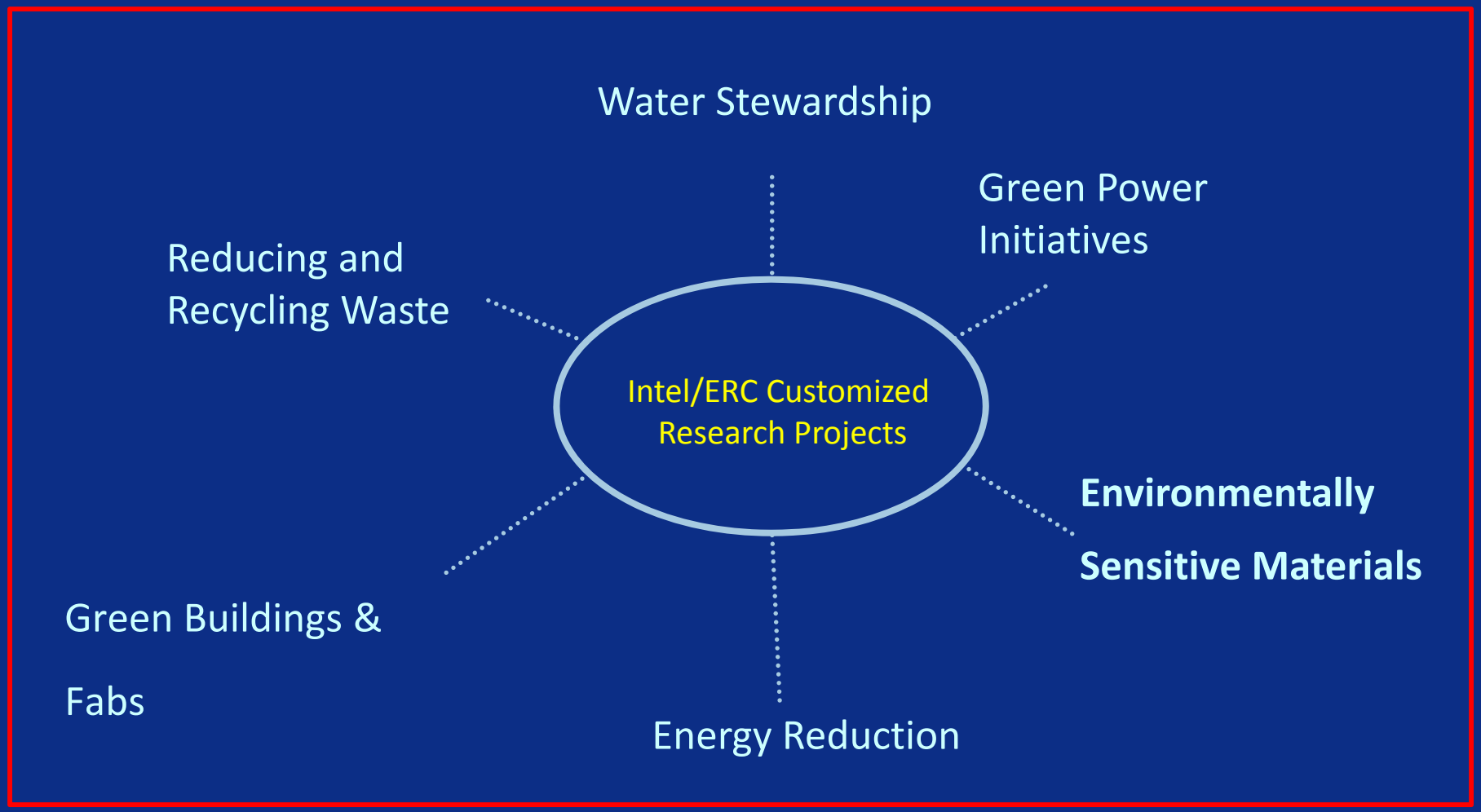
Achieve engineering and design milestones to ensure that Intel products keep the energy-efficiency lead in the market for our next two product generations.

Reduce water use per chip[1] by 2012 from 2007 levels.

Reduce generation of chemical waste per chip by 10% by 2012 from 2007 levels.

Recycle 80% of chemical and solid waste generated per year.

Scope of Work: Big Challenge / Big Reward



Potential Beneficiaries of Academia/Industry Research

Solar Panel Manufacturing

Flat Panel Display Manufacturing

Photonics

State & US Economic Development

Suppliers

Semiconductor Manufacturing

Device Makers

INTERNATIONAL SEMATECH ISMI MANUFACTURING INITIATIVE ESH Technology Center

Energy Research

Smart Buildings & Factories

C Footprint

Industry/University/Gov Partnership in C Footprint reduction

SRC Semiconductor Research Corporation Pioneers in Collaborative Research®

Industry/University Partnership in Energy & Natural Resource Management

Academic Research Student Programs

Conclusions

- Academia/Industry partnership is vital for enabling U.S. leadership
- Investing in smart energy and sustainability research will help sustain and grow US semiconductor manufacturing while ultimately reducing the carbon impact of the industry.
- ERC is a very successful consortium and is a key player in Energy and Sustainability research – need to have a robust Energy & Sustaining Roadmap

Goal: Review the Energy & Sustainability Research Roadmap at the 2012 ERC Annual Meeting