Lowering the Environmental Impact of High-k and Metal Gate-Stack Surface Preparation Processes

(*Task Number: 425.028)*

PIs:

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- **Omid Mahdavi, Micro/Nano Fabrication Center, University of Arizona**

Graduate Students:

- **Kedar Dhane, graduated; currently with Intel**
- **Gaurav Thareja, Electrical Engineering, Stanford University**
- **Davoud Zamani, Chemical Engineering, University of Arizona**

Cost Share (other than core ERC funding):

- **$50k from Stanford CIS**
- **$20k from WSP**

Objectives

- Development of a wet etch method to minimize fluoride consumption during etching of hafnium based high-k materials
- Significant reduction of water and energy usage during rinse
- Validation of low-resource usage processes using metal-high-k device fabrication and electrical characterization.

Subtasks 1 and 2

- **A wet etch method to reduce fluoride consumption during etching of high-k**
- **Reduction of water and energy usage for rinse after high-k etch**

ESH Metrics and Impact

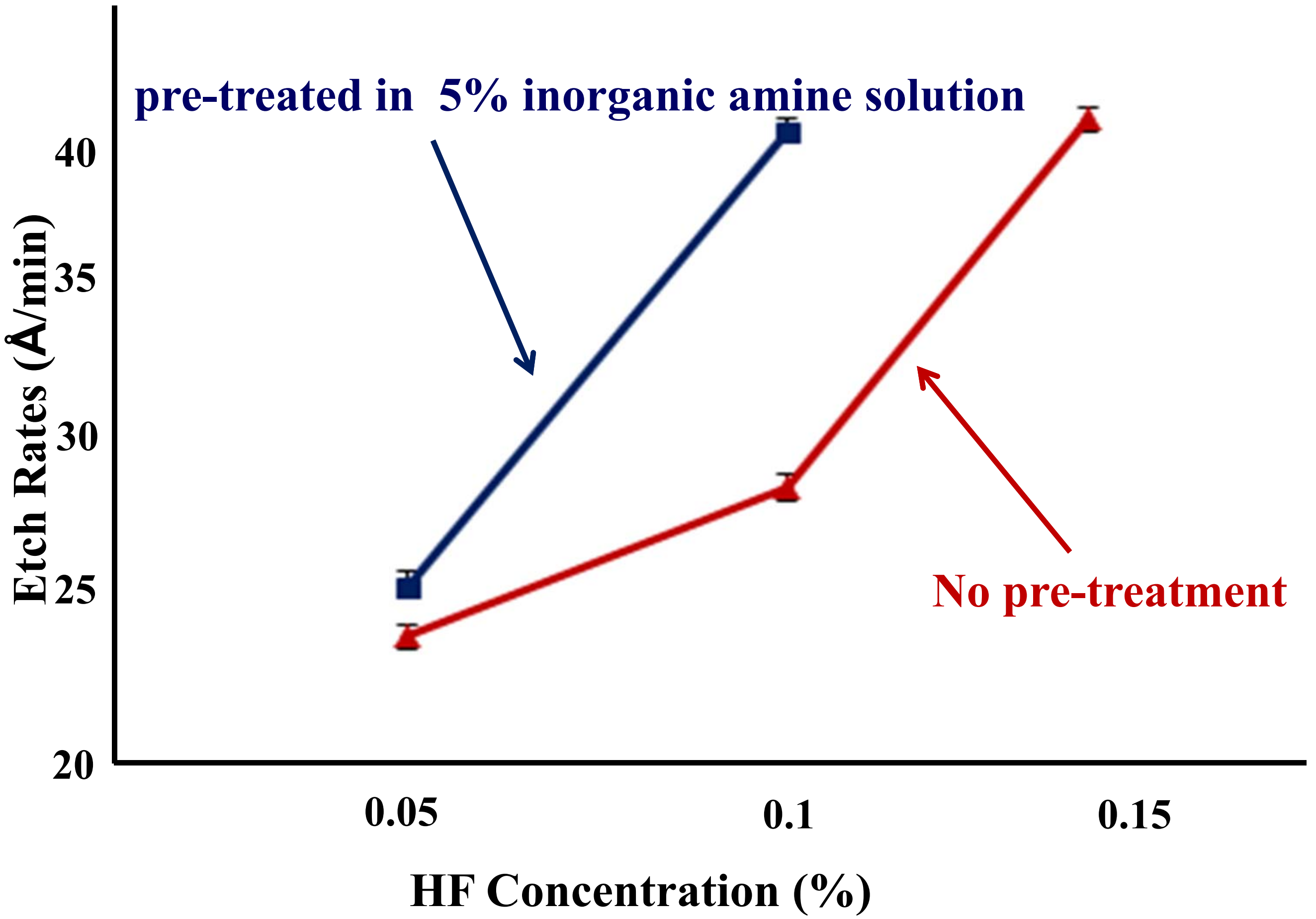
- **Reduction in the usage of HF; reduce the ESH impact of etch chemistries for hafnium based high-k materials**
- **Significant reduction in water usage during rinse**
- **Significant reduction in energy usage during rinse**
- **Reduction of rinse time leading to increase in throughput and decrease in resource usage**

Subtask 1: Lowering HF Usage
Method of Approach

Pre-treatments to enhance the etch rate of hafnium silicate in dilute HF:

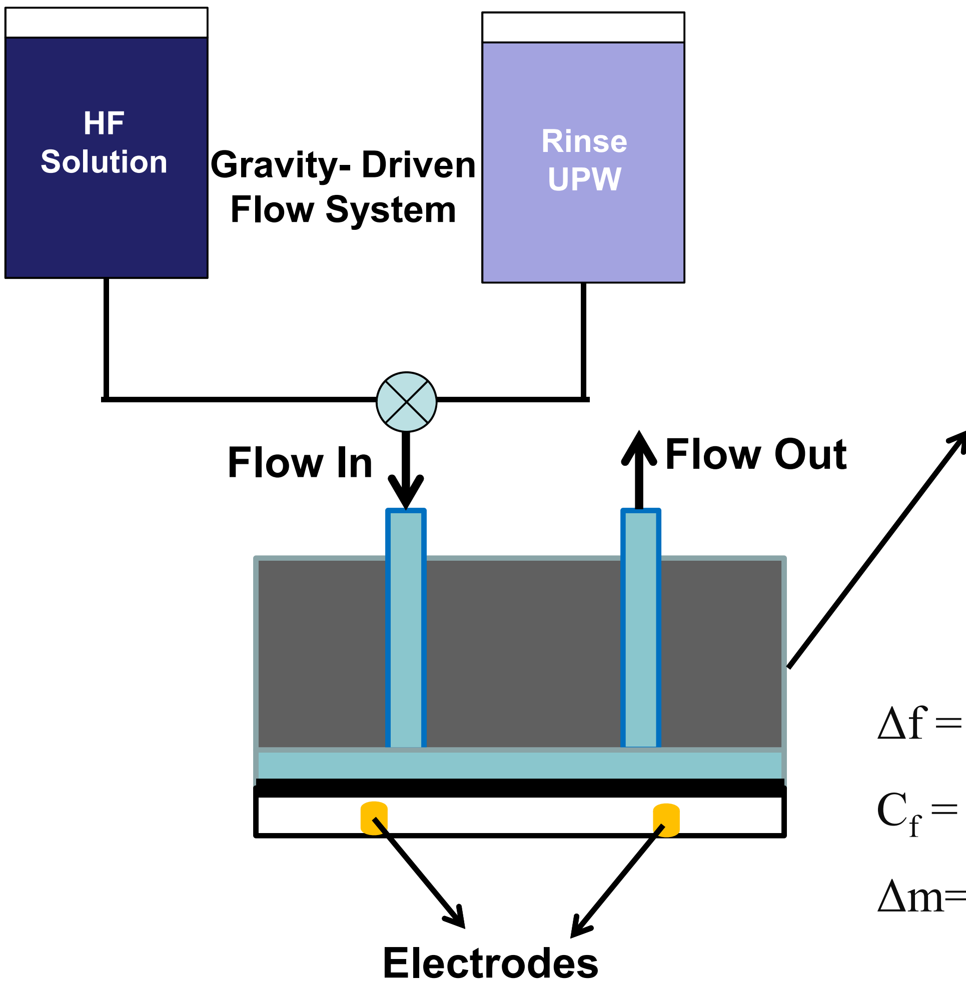
- **Pre-reduction treatment in gas mixtures, CO/CO_2, CO/N_2, and H_2/N_2**
- **Pre-treatment in aqueous inorganic amine solution**

ESH Gain in Etching of Hafnium Silicate



Reductive pretreatment of hafnium silicate ($HfSi_{0.74}O_{3.42}$) in 5% inorganic amine solution improves the etch rate in 1:500 $HF:H_2O$

Subtask 2: Reducing the Water and Energy Usage
Experimental Setup



High-k coated Quartz Crystal

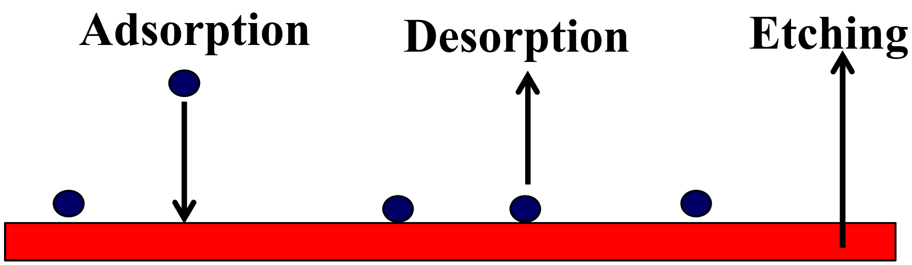
$$\Delta f = -C_f \Delta m$$

Δf = Observed frequency change in Hz,

C_f = Sensitivity factor of the crystal

Δm= Change in mass per unit area, in $\mu g/cm^2$

Process Model for DHF Interaction with High-k



k_a: Adsorption Rate Coefficient

k_d: Desorption Rate Coefficient

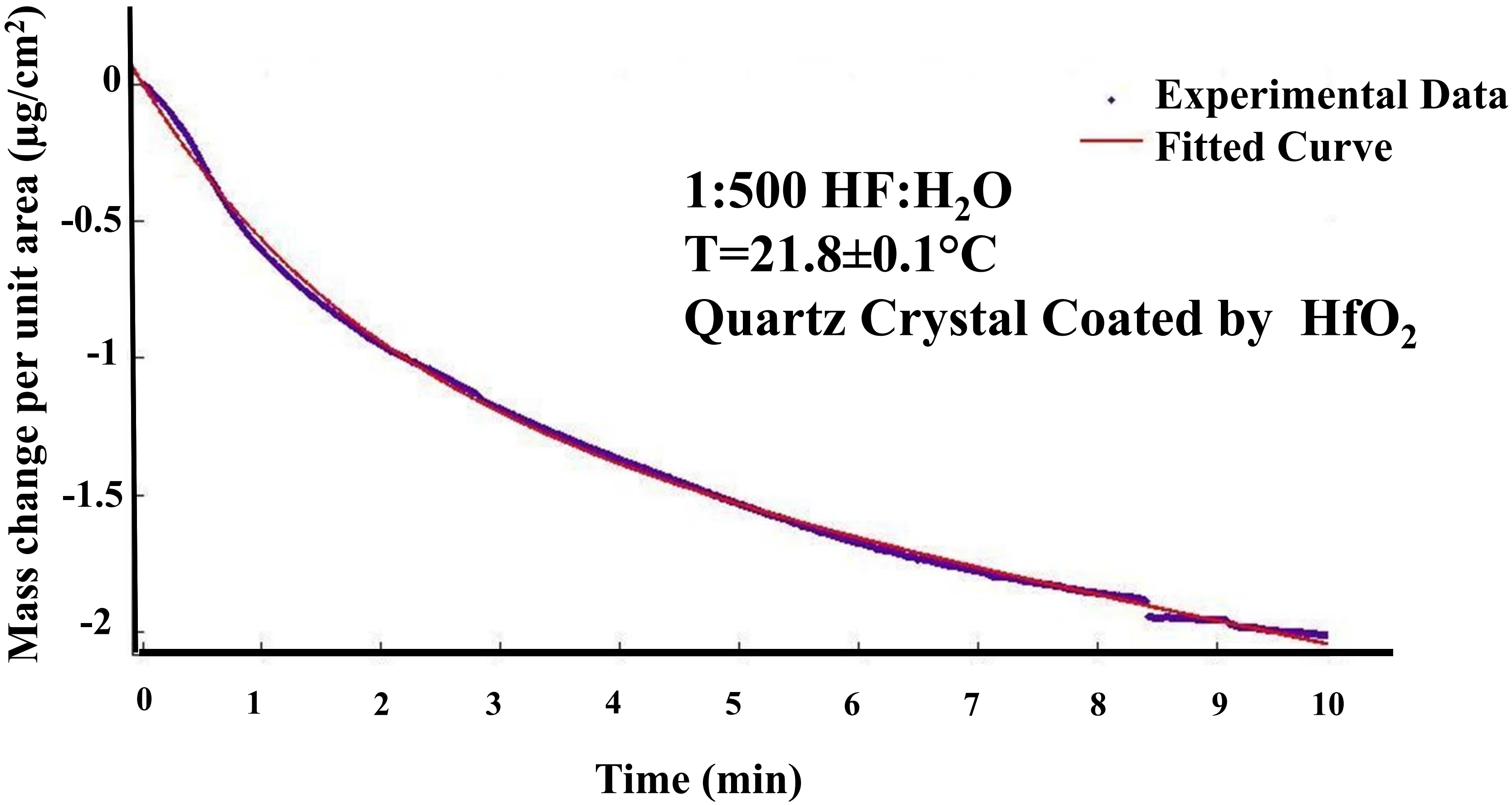
k_e: Etching Rate Coefficient

$$\frac{dC_s}{dt} = \underbrace{k_a C_b (S_0 - C_s)}_{\text{adsorption rate of } F^-} - \underbrace{k_d (C_s)}_{\text{desorption rate of } F^-}$$

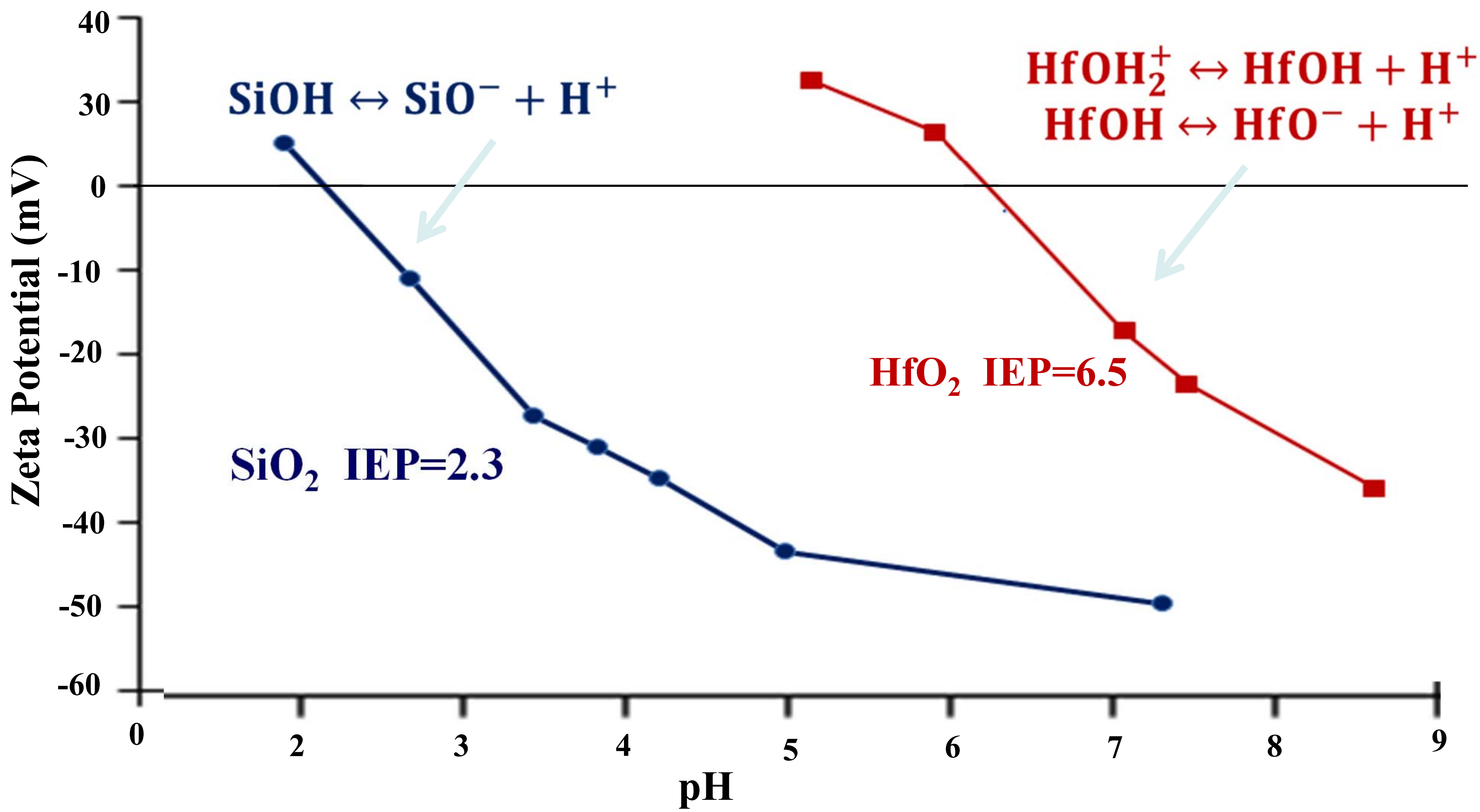
$$\underbrace{-\frac{1}{A}\frac{dM}{dt}}_{\text{rate of mass change}} = -(MW_{F^-})\frac{dC_s}{dt} + \underbrace{(MW_{HfO_2}) \times k_e C_b (S_0 - C_s)}_{\text{etching rate of } HfO_2}$$

Analysis of the Experimental Data

Adsorption Rate Coefficient: 133 (lit/mol.s)
Desorption Rate Coefficient : 0.001 (1/s)
Etching Rate Coefficient : 1407 (lit/mol.s)



Effect of Surface Charge on Rinsing of HfO_2



HfO_2 surface in UPW is more positive than SiO_2 surface. Therefore, removal of negative ionic species from HfO_2 by rinse will be more difficult.

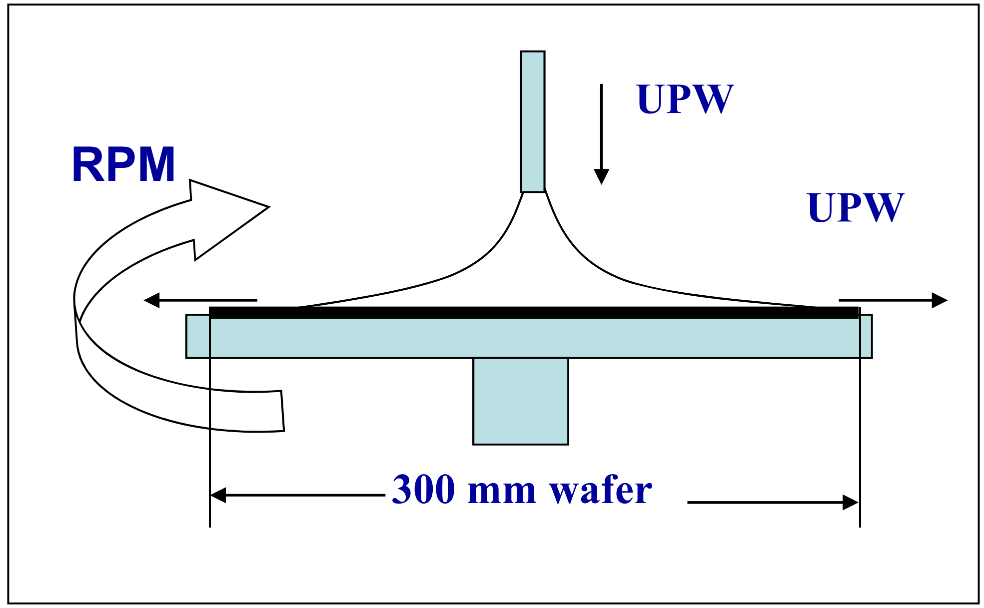
Analysis of Rinse Process in Single-Wafer Tools

Surface adsorption and desorption

$$\frac{\partial Cs}{\partial t} = K_a C_2 (S_0 - C_S) - K_d C_S$$

Poisson equation $\nabla^2 \varphi = -\frac{\rho}{\varepsilon}$

where charge density $\rho = F \sum_i z_i C_i$



Process Model Schematic

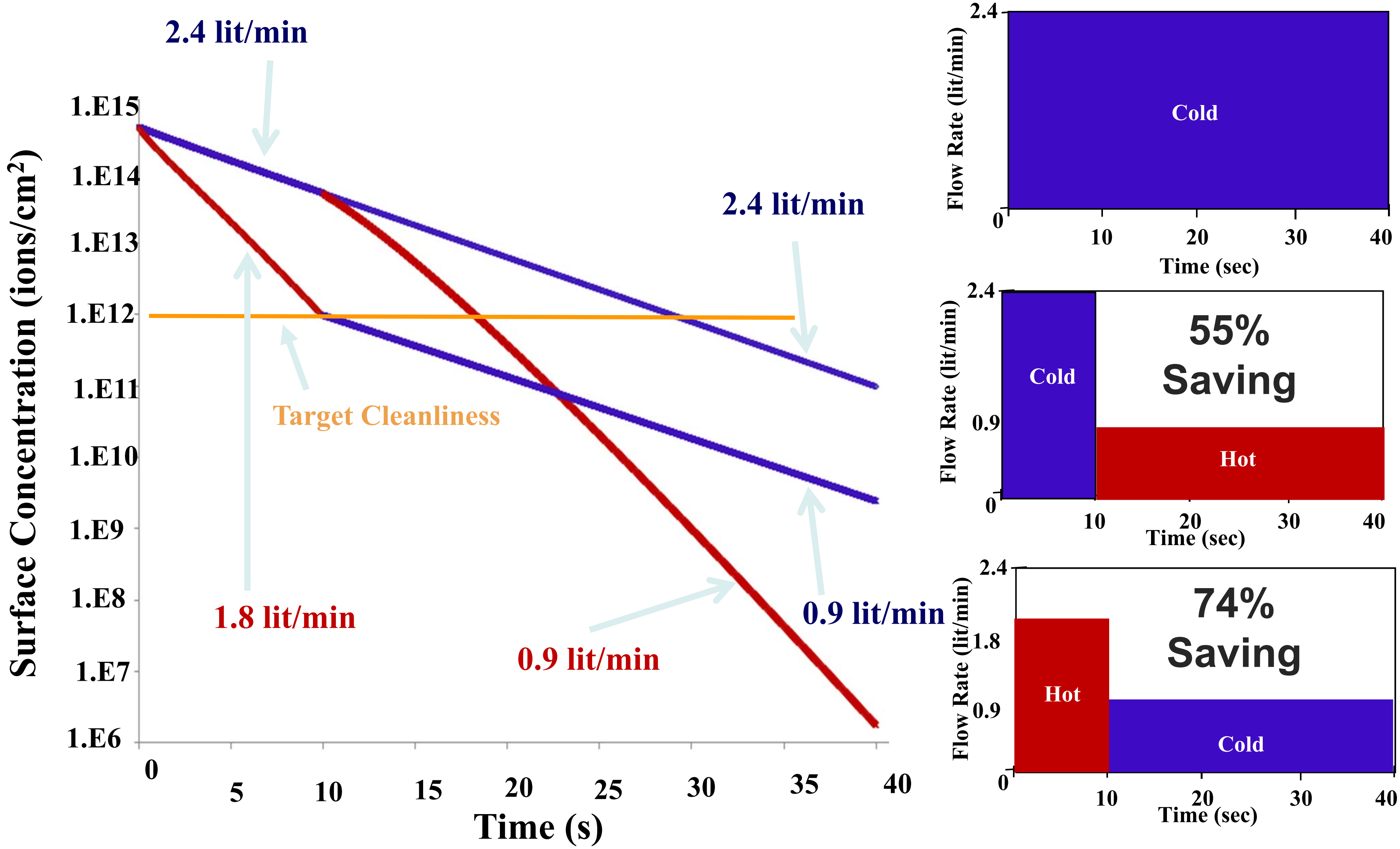
Multi-component species transport equations

$$\frac{\partial C_i}{\partial t} = \nabla \cdot (D_i \nabla C_i + z_i F \mu_i C_i \nabla \varphi) - u \nabla C_i$$

$$h = 0.782\left(\frac{Q\mu}{\rho\omega^2 r^2}\right)^{1/3} \qquad u_r = \frac{\rho\omega^2 r h^2 (1 - (1 - \frac{z}{h})^2)}{2\mu}$$

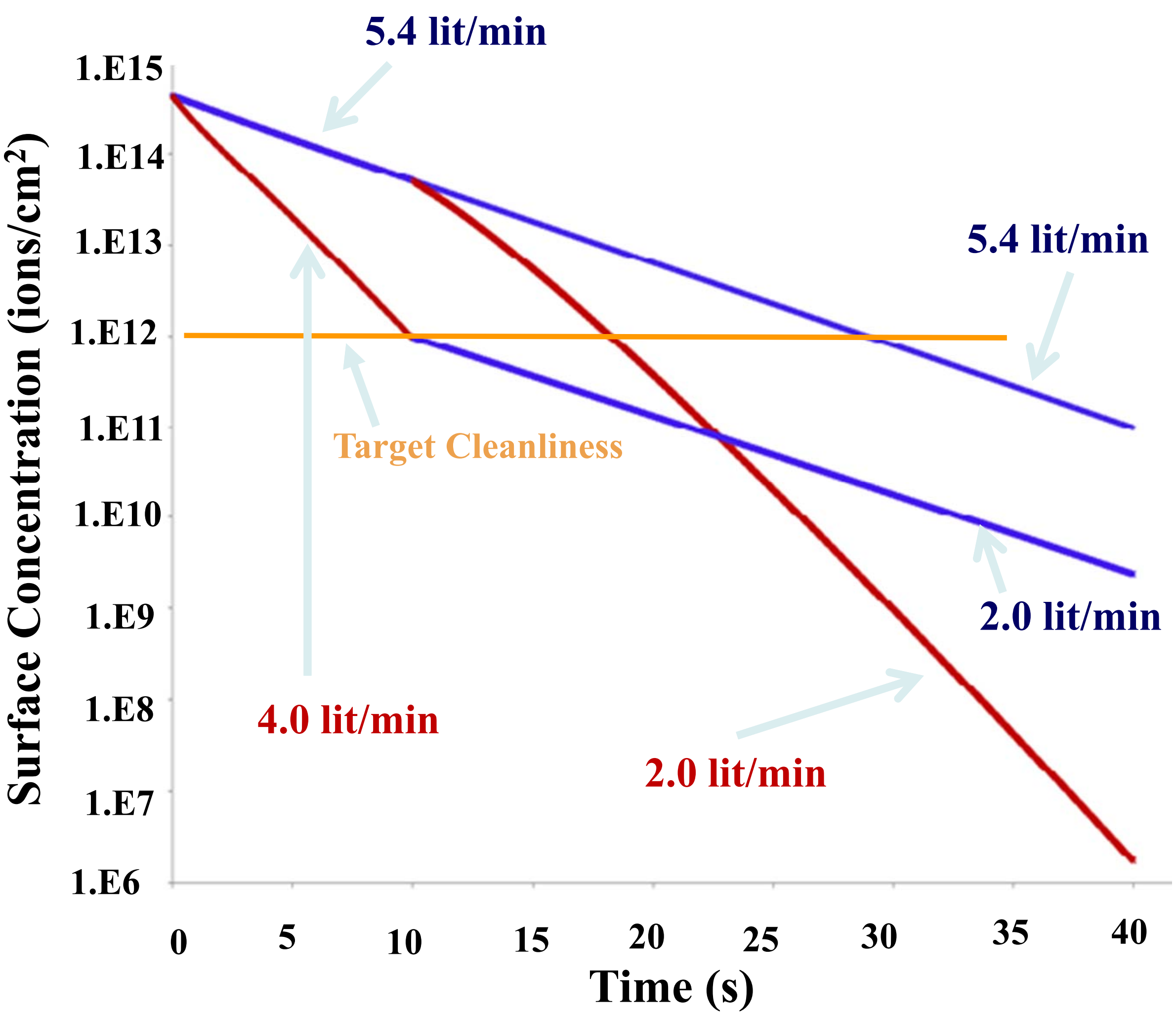
Low Water/Energy Single-Wafer Spin Rinsing

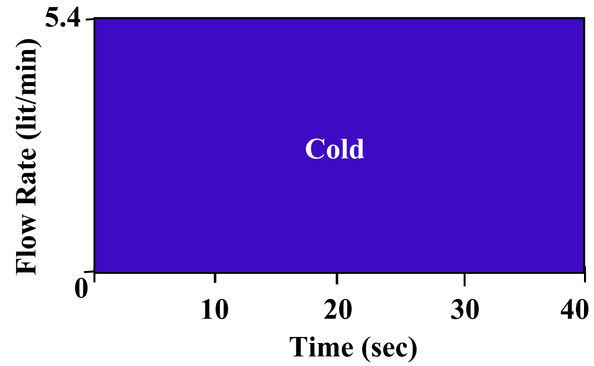
Wafer size: 300 mm; 800 rpm

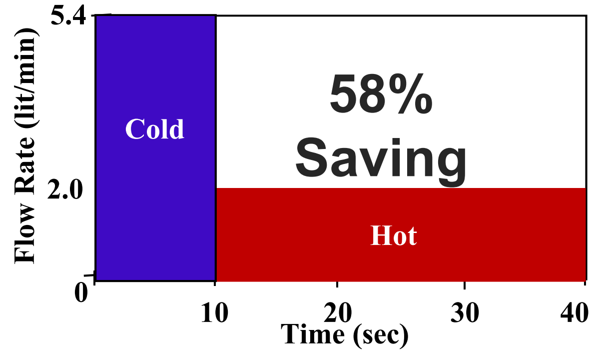


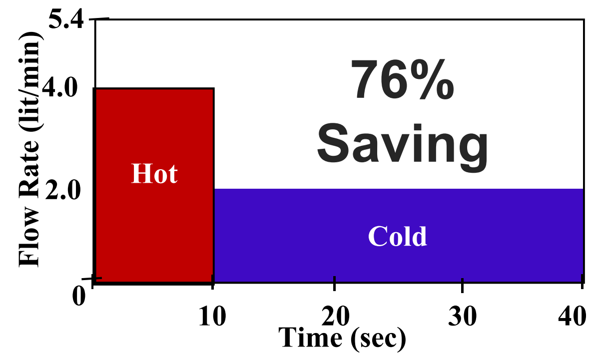
Low Water/Energy Single-Wafer Spin Rinsing

Wafer size: 450 mm; 800 rpm









Summary

- **Pre-treatment of hafnium silicate with an inorganic amine solution enhances its etch rate in dilute HF solutions; this would allow lower HF concentration and lower overall HF usage for etching, without compromising the etch rate.**
- **A comprehensive method for analyzing the rinse process in single-wafer spin tools is developed; application to high-k rinsing shows significant ESH gain by using the proposed staged rinse process.**

Publications and Presentations

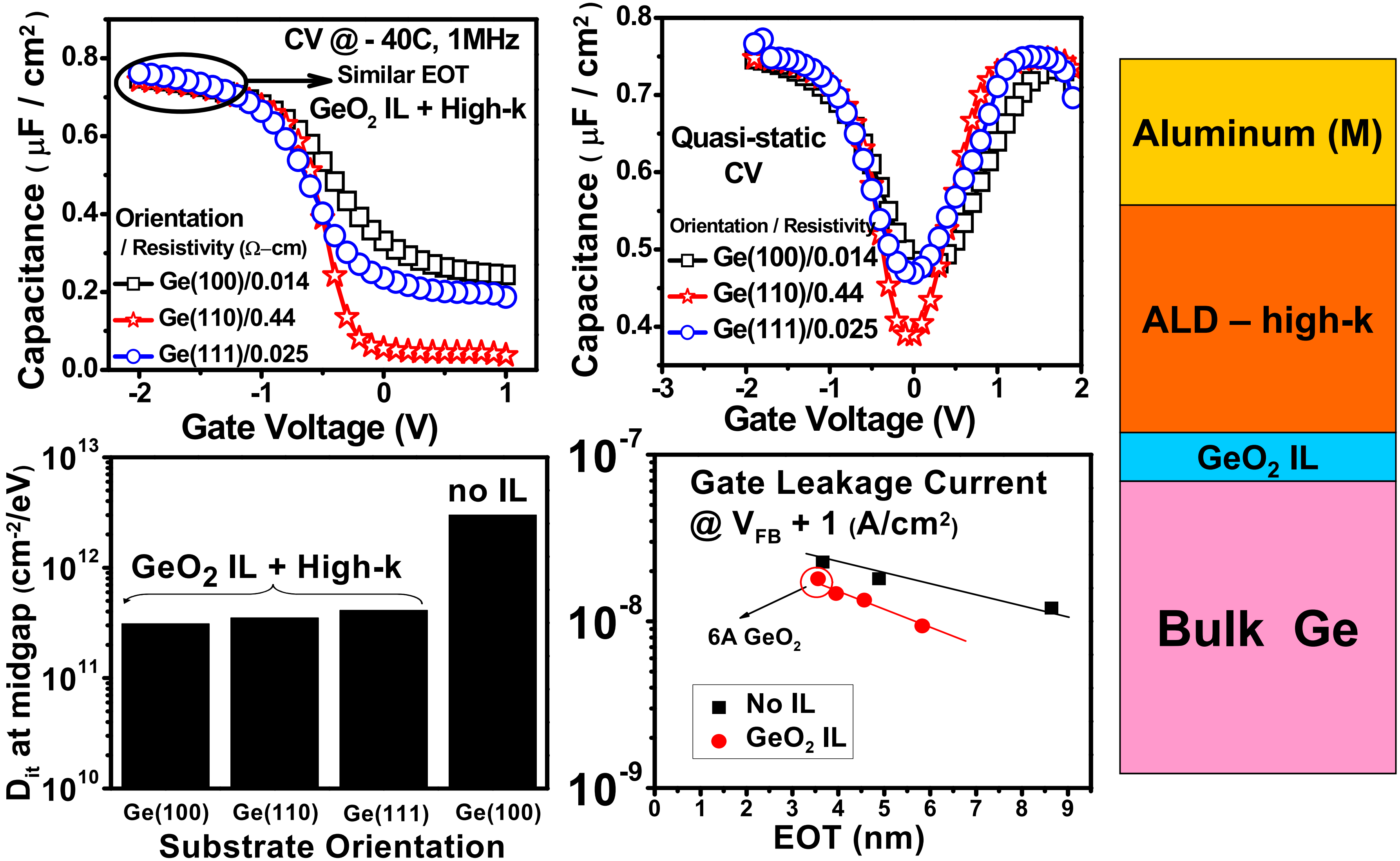
- X. Zhang, J. Yan, B. Vermeire, F. Shadman, and J. Chae, "Passive Wireless Monitoring of Wafer Cleanliness During Rinsing of Semiconductor Wafers," IEEE Sensors Journal, 10 (6), 1048, 2010.
- K. Dhane, J. Han, J. Yan, O. Mahdavi, D. Zamani, B. Vermeire, and F. Shadman, "Dynamics of Cleaning and Rinsing of Micro and Nano Structures in Single-Wafer Cleaning Tools," IEEE Transactions on Semiconductor Manufacturing, 24 (1), 125, 2011
- Jun Yan, "Water Usage Reduction and Water Reuse in Semiconductor manufacturing", the Second International Congress on Sustainability Science and Engineering, Water Re-Use Workshop, January 14, 2011, Tucson, Arizona, USA (Invited Presentation)
- D. Zamani, J. Yan, M. Keswani, O. Mahdavi, S. Raghavan, F. Shadman, "Environmentally Friendly Chemicals for Patterning of Hafnium Based Oxides and Silicates and Cleaning and Rinsing in Single-Wafer Cleaning Tools" Submitted to TECHCON 2011, Austin , Texas
- D. Zamani, J. Yan, M. Keswani, O. Mahdavi, S. Raghavan, F. Shadman, "Environmentally Friendly Chemicals for Patterning of Hafnium Based Oxides and Silicates and Cleaning and Rinsing in Single-Wafer Cleaning Tools" Submitted to SESHA 2011, Scottsdale, Arizona
- D. Zamani, J. Yan, M. Keswani, S. Raghavan, F. Shadman, "Adsorption - Desorption of Diluted Hydrofluoric Acid on Hafnium Oxide Quartz Crystal in Flow Mode" In Preparation for Submission to Electrochemical and Solid-State Letters.

Industrial Interactions and Technology Transfer

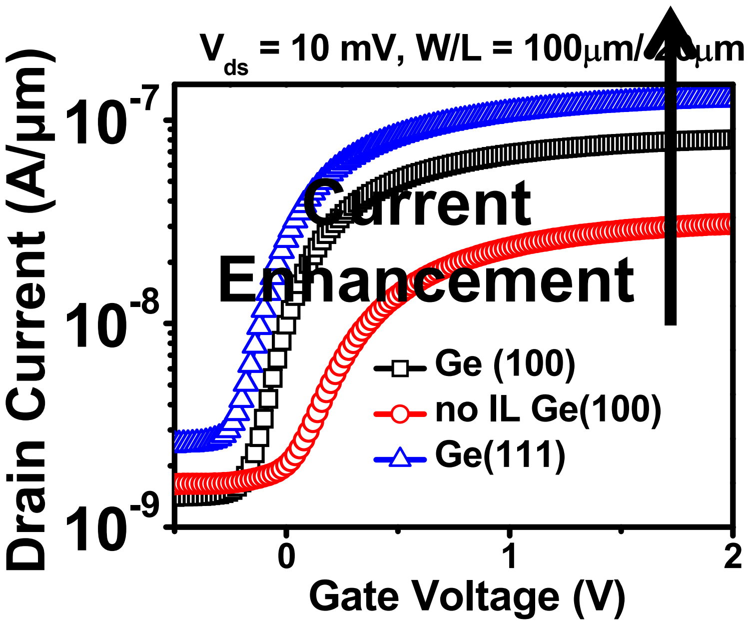
- **Interactions with ASM (Eric Shero and Eric Liu) for preparation of high-k wafers**
- **Interactions with Sematech (Joel Barnett) for high-k etching and cleaning development.**

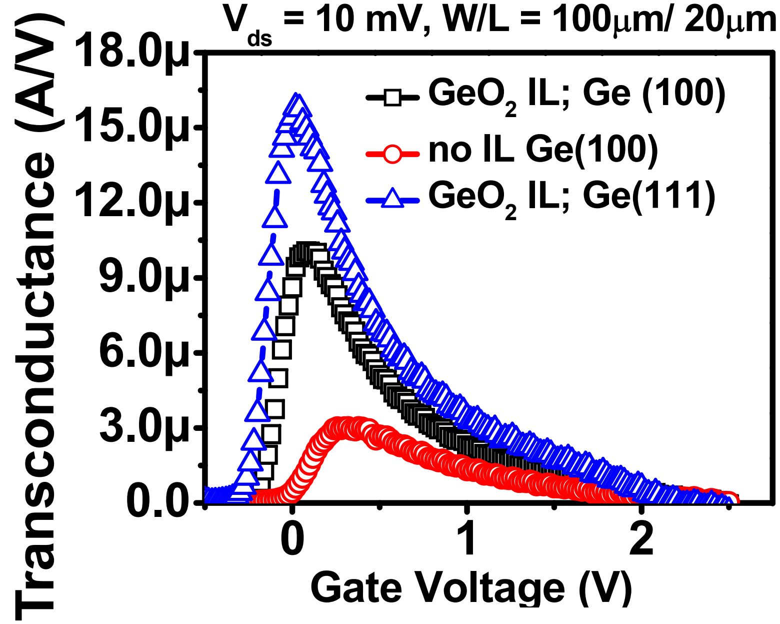
Subtask 3: Test Structure

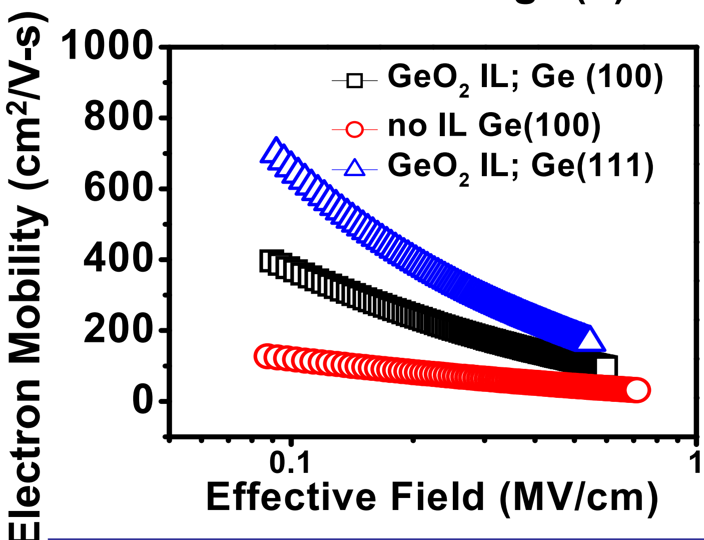
GeO_2 : Growth Rate, D_{it}, Scalability



Drive Current, Mobility Enhancement



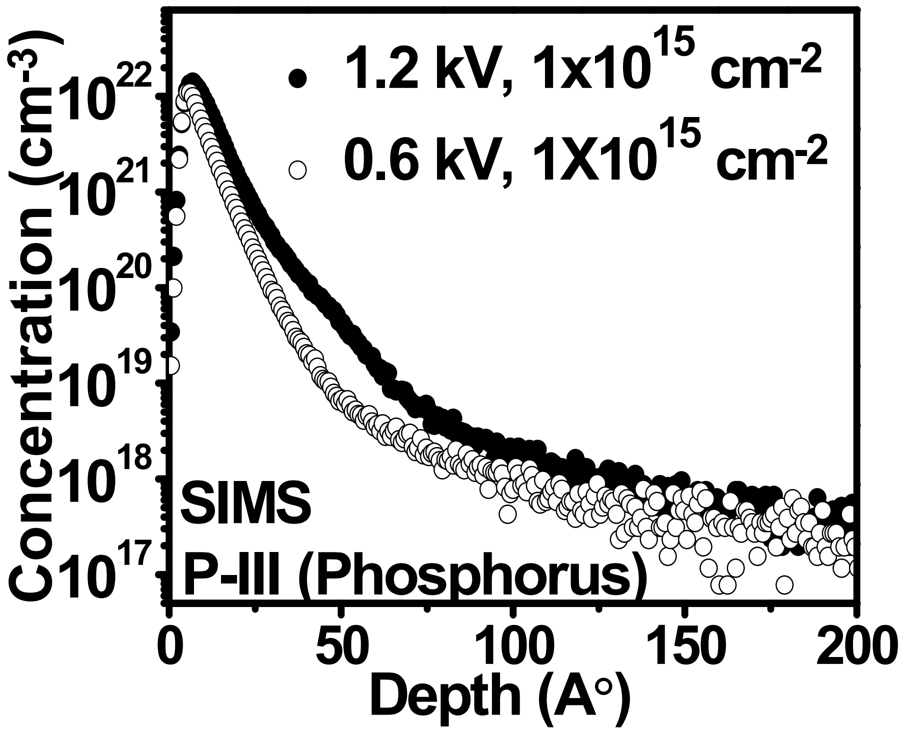


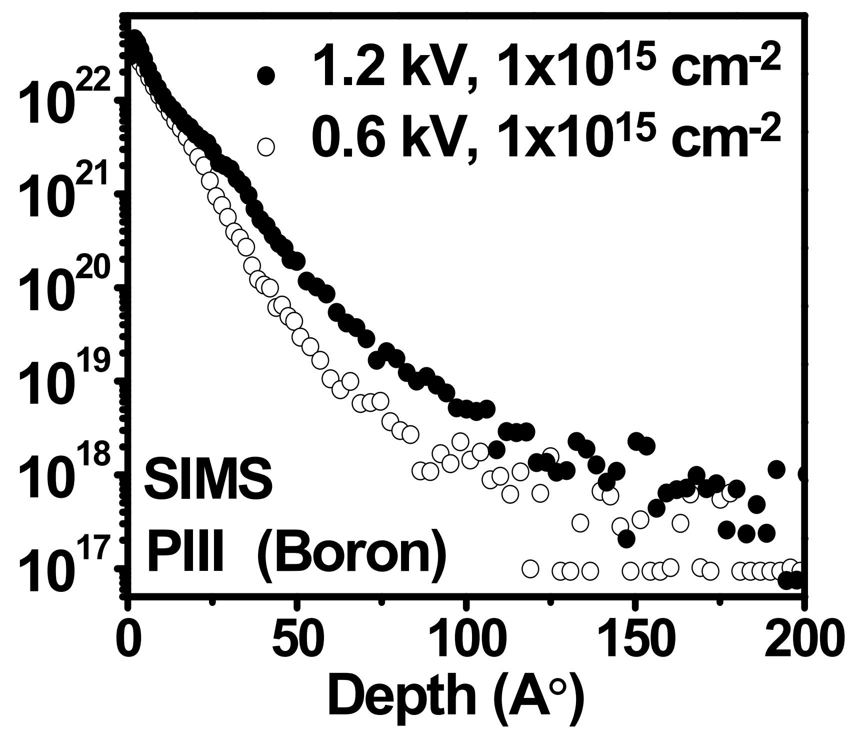


Ge(111) has higher mobility – lower m*

Samples without GeO_2 – poor mobility - interface/coulomb scattering

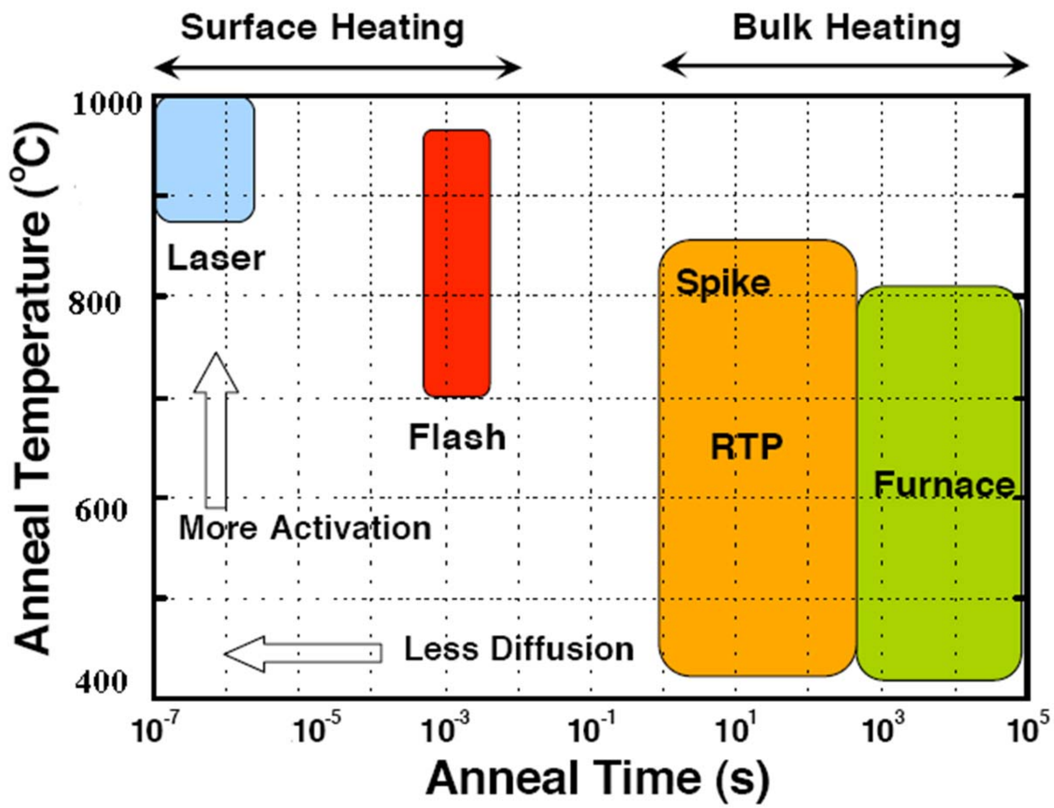
Plasma Doping in Ge





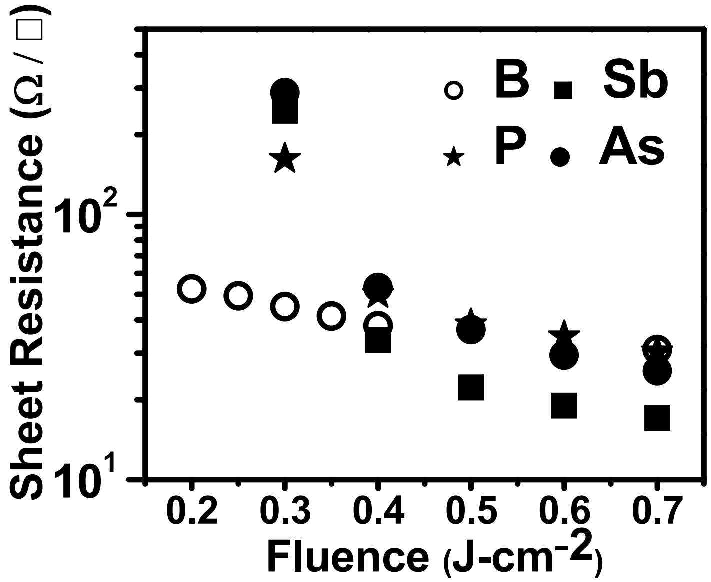
- X_j < 10nm @ 5 x 10^{18} cm^{-3}
- Shallower junctions possible
  - Scaling the voltage
  - Using arsenic species

Dopant Activation for USJ in Ge



- Laser Thermal Processing (LTP)
  - High dopant activation
  - Reduced diffusion
  - Implantation damage annihilation (Melt – Regrowth)

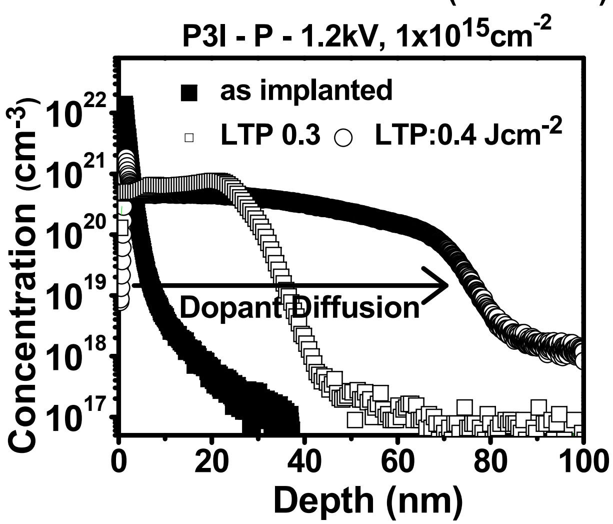
Sheet Resistance & SIMS

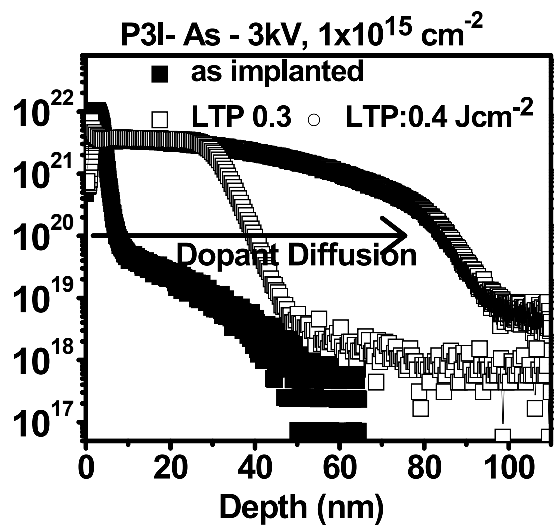


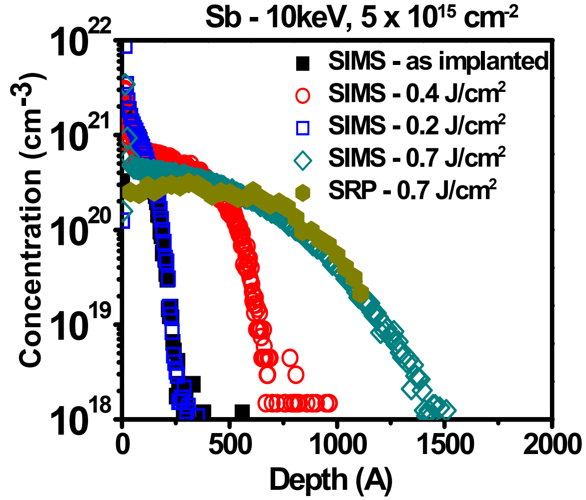
Laser Fluence ↑

Dopant diffusion ↑

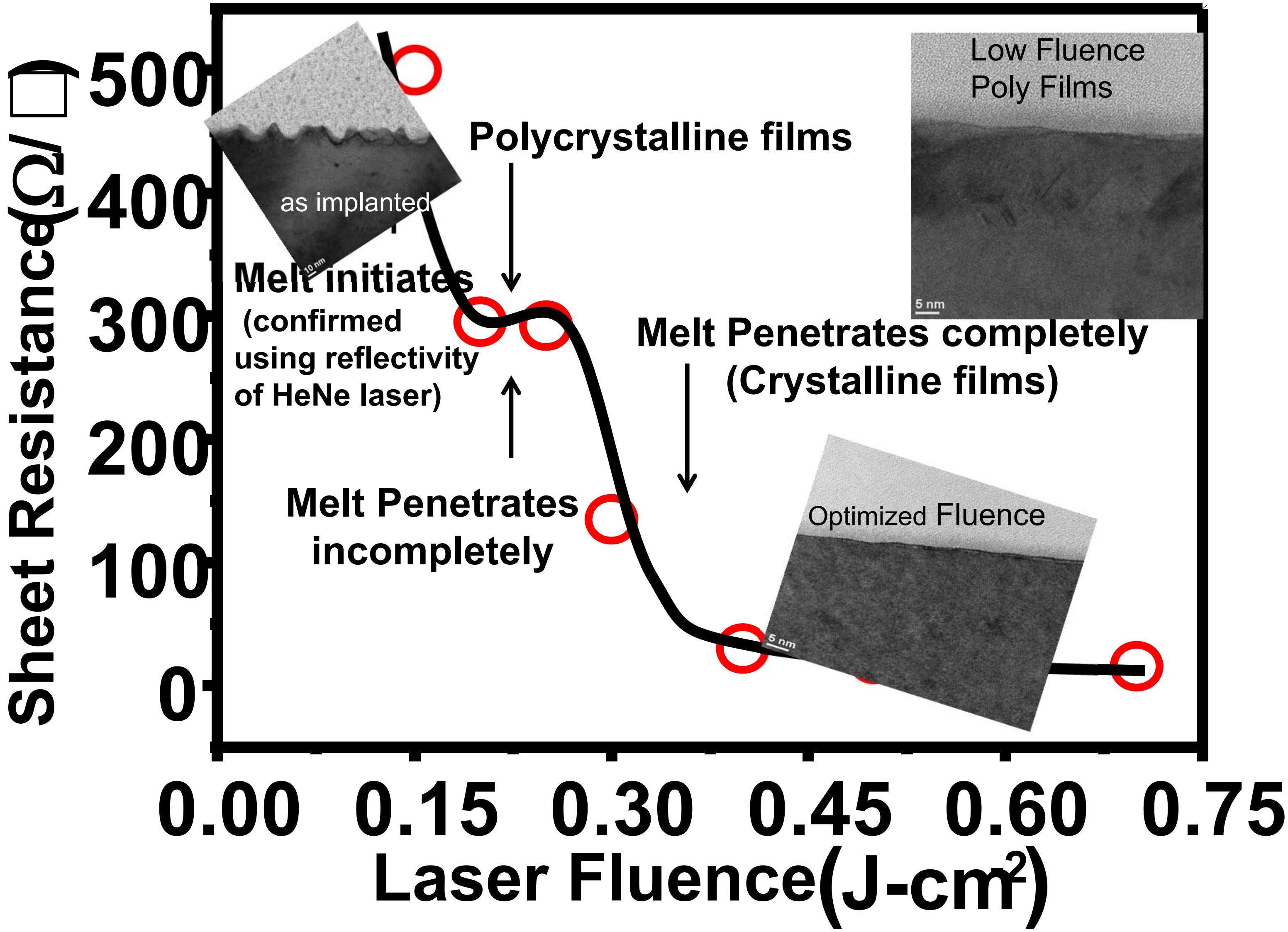
Sheet Resistance ↓



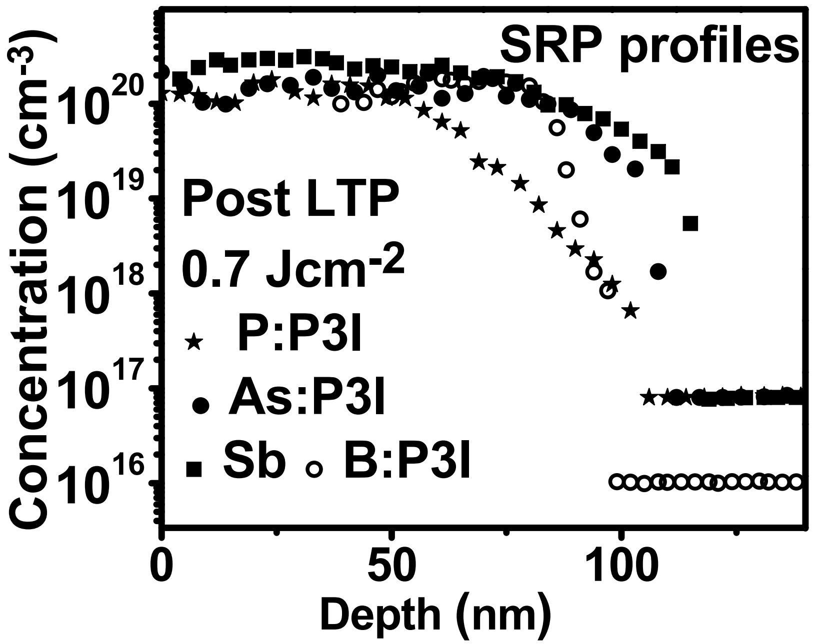




Sheet Resistance and TEM



Dopant Activation using LTP

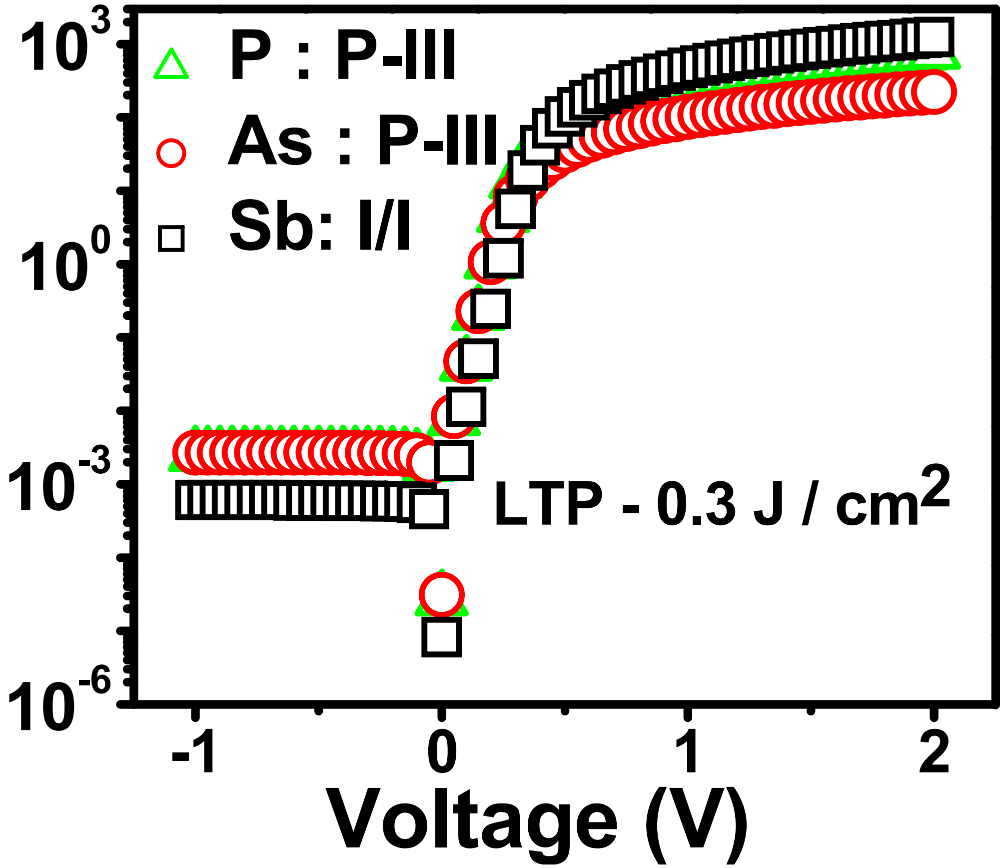


Annealing Technique	Dopant	Electrical Activation (cm^{-3})
Furnace Anneal[1]	P	8×10^{18}
Rapid Thermal Anneal (RTA)[2]	P / As / Sb / B	2×10^{19} / 8×10^{18} 8×10^{18}/ 1×10^{20}
Flash Anneal[3]	P	6×10^{19}
In-situ doping[4]	P	1×10^{19}
This Work (LTP)	P/ As / Sb / B	> 1×10^{20}

Dopant Activation > 1×10^{20} cm^{-3}

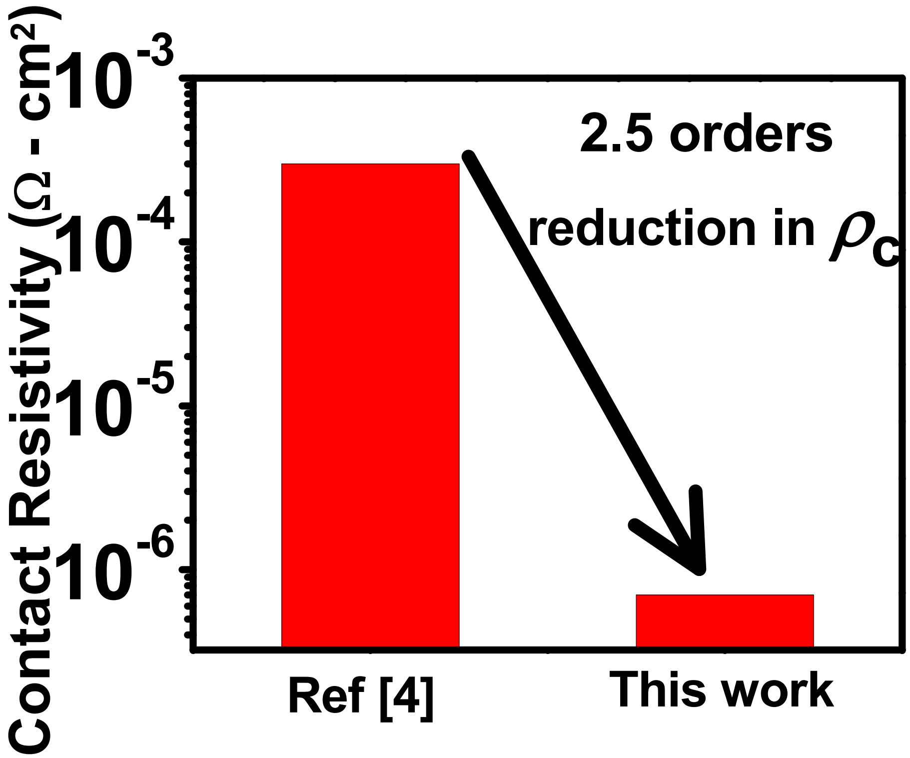
[1] D.Kuzum, et al., IEDM, 2009, 453, [2] C.O.Chui, et al. APL, 83, 3275, 2003,
[3] C. Wundisch, et al. 95, 252107, 2009, [4]H.-Y. Yu, et al. 685, IEDM 2009

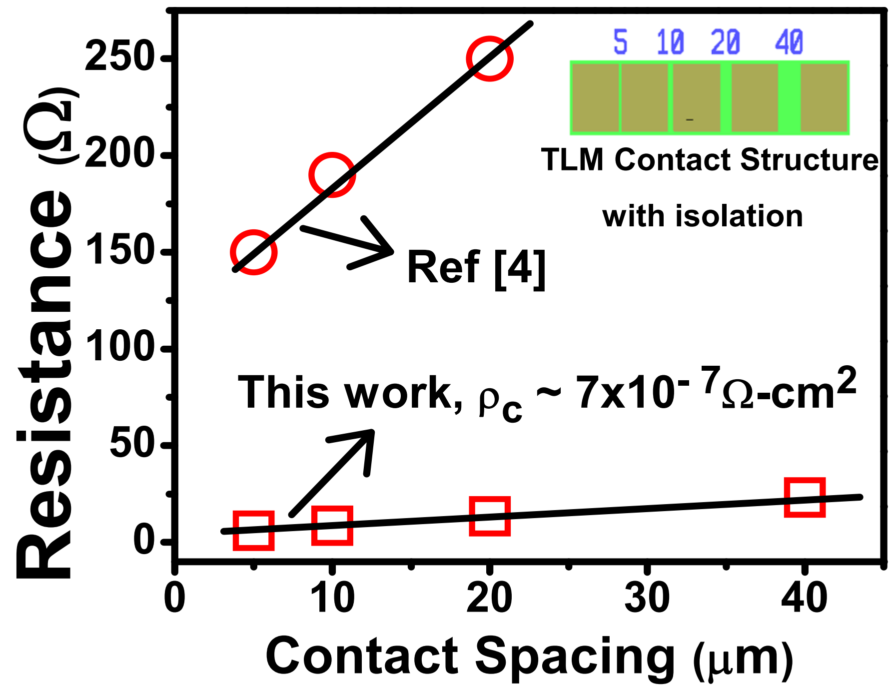
High Performance N^+/P Ge Diodes



$I_{on} / I_{off} > 1 \times 10^5$, $\eta < 1.2$

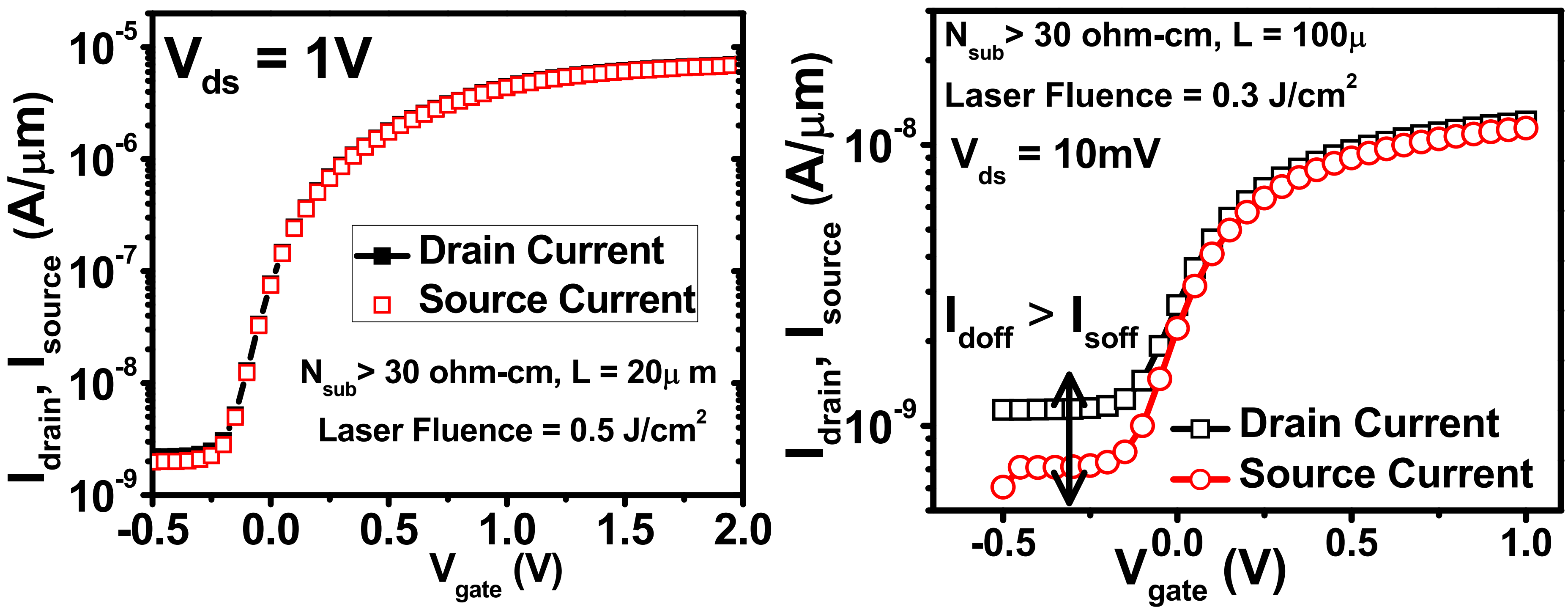
Contact Resistivity (ρ_c) & Benchmark





Significant reduction in Metal / N$^+$ Ge ρ_c of 7 x 10^{-7} Ω-cm^2

MOSFET results



Unoptimized laser fluence causes discrepancy between I_{drain} and I_{source} due to high diode leakage

Contributions

- First demonstration of
  - High dopant activation (> $1x10^{20}$ cm^{-3}) using Sb dopants (n-type) in Ge
    - Well behaved n^+/p diodes (I_{on}/I_{off} > $1x10^5$, η < 1.2) and MOSFETs.
    - Lowest contact resistivity for metal(Ti/Al)-n^+ Ge contacts ($7x10^{-7}$ Ω-cm^2)
  - Ultra Shallow Junctions (X_j < 10nm) for Ge
  - Scalable GeO_2 Interfacial Layers (IL) (sub -1nm) for Ge MOS with performance enhancement for Ge NMOSFET
  - Substrate orientation independent growth rate and D_{it} for GeO_2 engineered using SPA oxide

Publications and Presentations

- **G. Thareja, J. Liang, S. Chopra, B. Adams, N. Patil, A. Nainani, E. Tasyurek, S.-L. Cheng, Y. Kim, S. Moffatt, R. Brennan, J. McVittie, T. Kamins, H-S.P. Wong, K. Saraswat and Y. Nishi, "High Performance Germanium N-MOSFET with Antimony Dopant Activation Beyond 1 x 10^{20} cm^{-3} ", IEDM, December 6, 2010**
- **Masaharu Kobayashi, Gaurav Thareja, Masato Ishibashi, Yun Sun, Peter Griffin, Jim McVittie, Piero Pianetta, Krishna Saraswat, Yoshio Nishi, "Radical oxidation of germanium for interface gate dielectric GeO_2 formation in metal-insulator-semiconductor gate stack,"** ***Journal of Applied Physics*****, 106, 104117, 2009.**

Industrial Interactions and Technology Transfer

- **Collaborative interactions with Initiative for Nanoscale Materials and Processes, INMP, at Stanford which is supported by 7 semiconductor and semiconductor equipment manufacturing companies.**