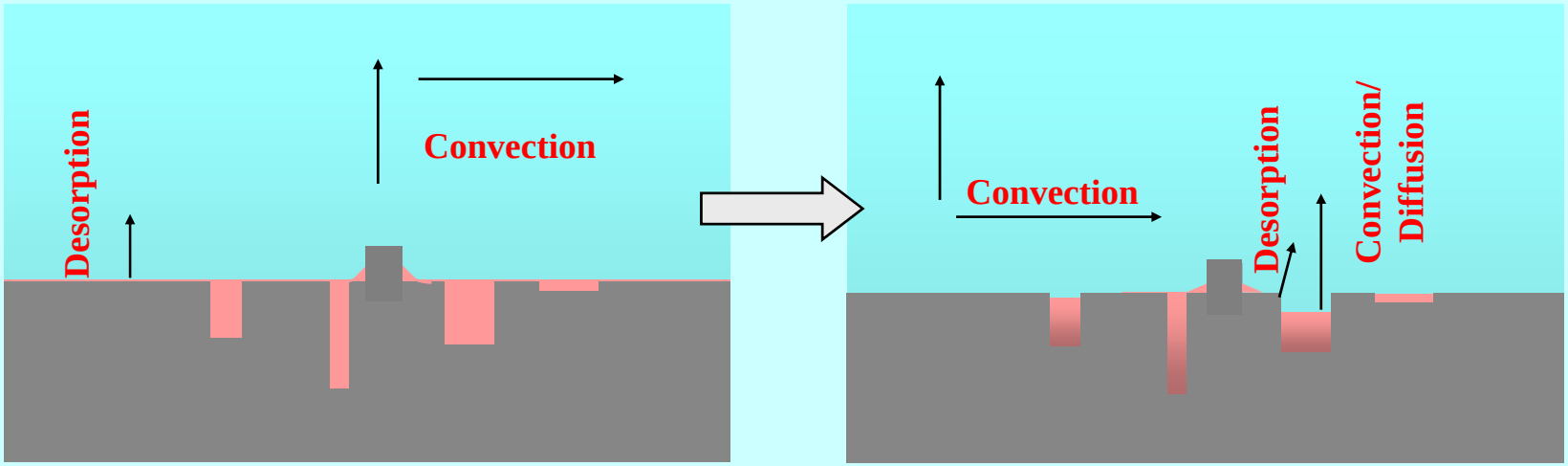
ESH Challenges in Surface Preparation of Large Wafers and Small (Nano) Features

Effect on Water and Energy Usage During Rinsing and Drying

SRC/Sematech Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

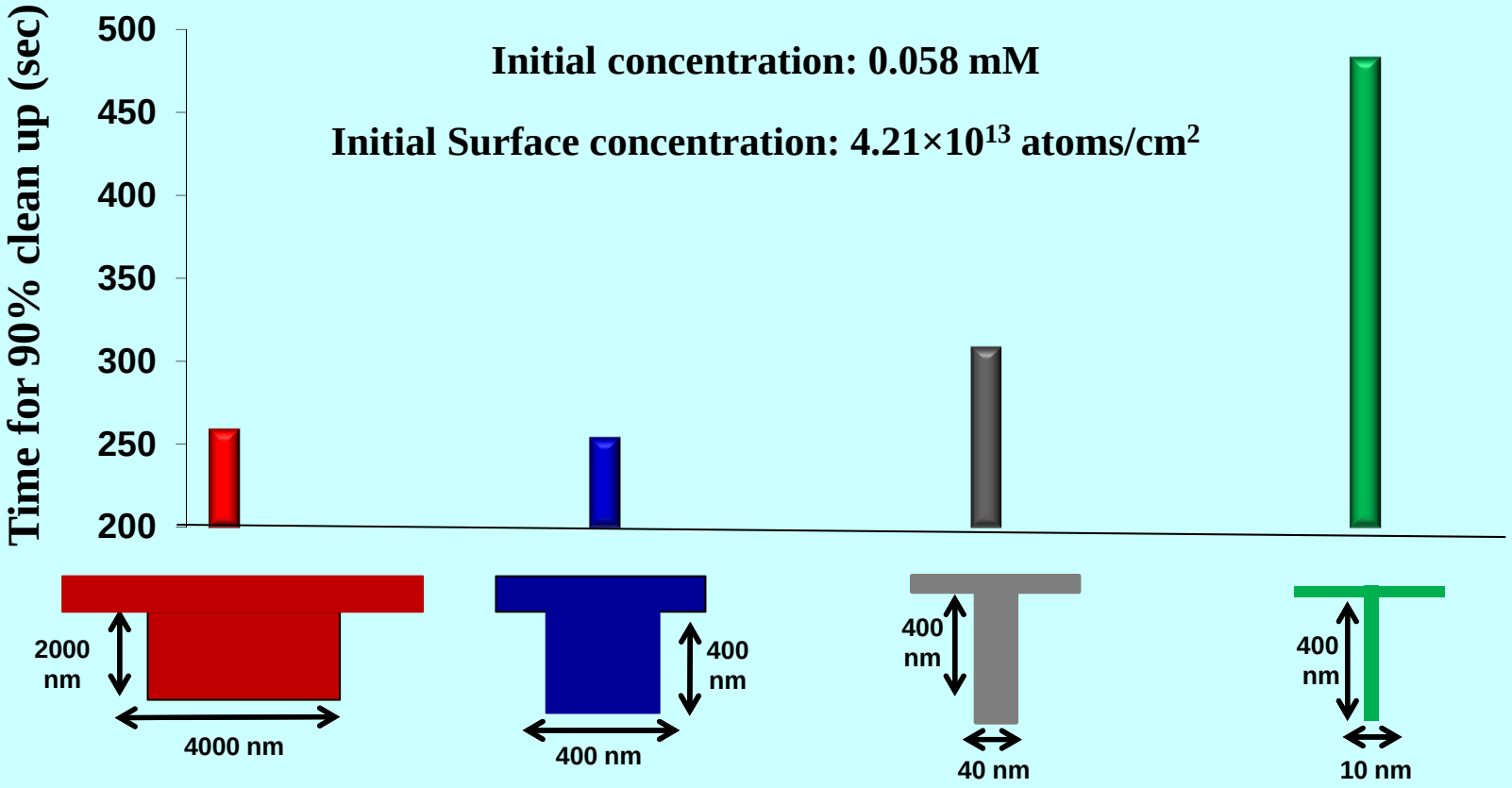
Cleaning of Nano-Structures



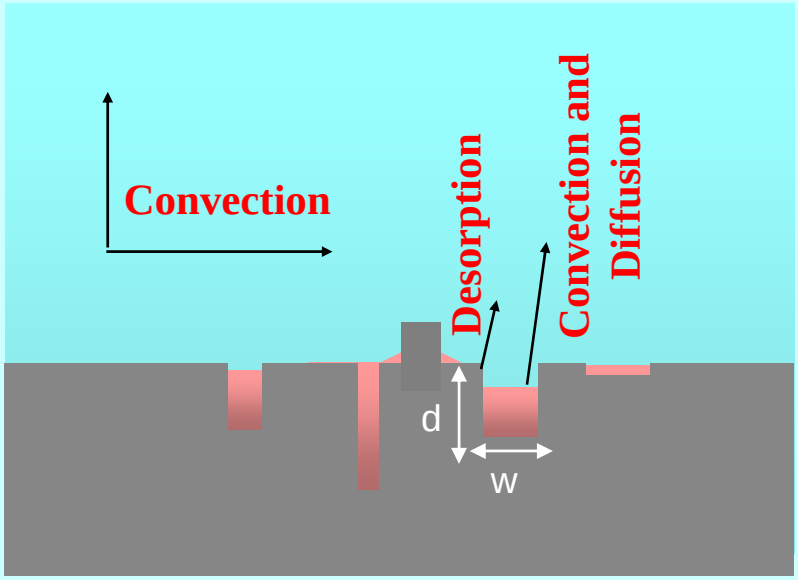
Mechanism	Time Scale	Flow Effect
Boundary Diffusion	$d^2/D \sim 10$ s	Indirect, mild
Convection	$d/u \sim 1\text{-}3$ s	Direct, strong
Desorption	$1/k_d \sim 0 - 10^5$ s	No effect

Single-Wafer Spin Cleaning and Rinsing

Effect of Feature Size



Issues in Cleaning of Nano-Structures

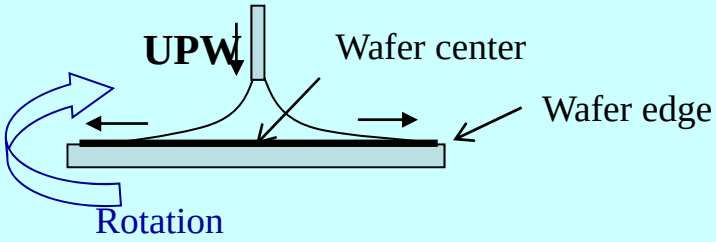


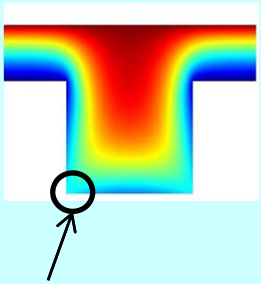
Estimates

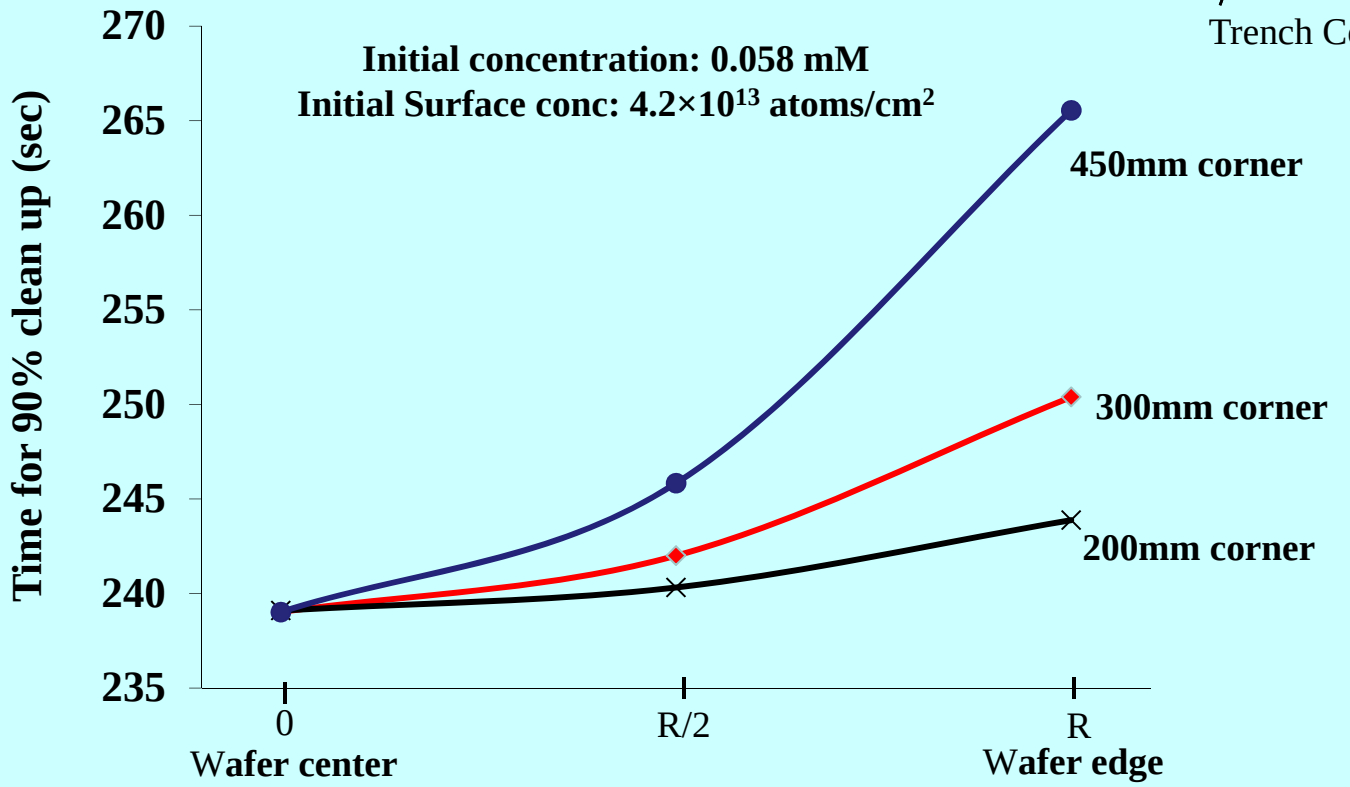
- **Feature depth: d**
- **Feature width: w**
- **Aspect ratio: a = d/w**
- **Just by diffusion alone: the required cleaning/rinsing/drying time is proportional to d^2 and inversely related to w.**
- **Adding surface charge effect, will further increase the cleaning/rinsing/drying time significantly.**
- **Resource usage is at least proportion to the cleaning/rinsing/drying time.**

Single-Wafer Spin Cleaning and Rinsing

Effect of Feature Location and Wafer Size







Some Surface Preparation R/D Needs

- **Same amount of water or energy per wafer (ITRS guidelines) may be very difficult to meet as feature size decreases into deep nano-range; innovative technologies are needed.**
- **Determine the bottleneck (slow and rate-controlling step) of the process; find ways to speed that up the controlling step (focus on removing the bottleneck) to reduce the processing time.**
- **Lower the extent of overkill (cushion) currently used; that requires real-time and on-line metrology and process control.**
- **Rinsing and drying are complex processes to be monitored, controlled, and optimized.**