Task ID: 425.022
Task Title: Environmentally-Friendly Cleaning of New Materials and Structures for Future Micro- and Nano-Electronics Manufacturing
Deliverable: Report on the application of the cleaning model for data analysis and final test plans on the potential cleaning recipes and procedures

Abstract:
We successfully demonstrated Schottky barrier height modulation in metal/Ge Schottky junction by inserting an ultrathin interfacial SiN layer which was deposited on top of germanium surfaces cleaned and passivated by using the process which was previously reported. The SiN layer suppressed strong Fermi level pinning in metal/Ge junction, which resulted in effective control of the Schottky barrier height. We systematically investigated its physics, for the first time, and almost zero Schottky barrier height was successfully obtained for electrons. We applied this technology to metal source/drain Ge NMOSFET and achieved low source/drain resistance as device level characterizations of germanium surface cleaning and passivation research.

Technical Results and Data:

Experimental:
Non-silicon channel material, especially Ge, is one of the key technology boosters to enhance device performance. There are demonstrations of superior performance in Ge PMOSFETs to Si. Ge NMOSFETs are, however, still not superior to Si. A major obstacle for Ge NMOSFETs is the large source/drain (S/D) resistance due to poor dopant incorporation into Ge. Although metal S/D is a possible candidate to reduce S/D resistance, strong surface Fermi level pinning of Ge results in high Schottky barrier height for electrons with typical germanides, such as NiGe, TiGe, CoGe. To mitigate this problem, reduction of the barrier height is necessary to achieve low S/D resistance in Ge NMOSFETs. In this study, SiN is deposited by our sputter system after Ge surface clean and passivation by using HCl treatment as reported in the previous period, and metal/SiN/Ge Schottky diode is fabricated for a variety of metal with different work function values. After the fabrication of capacitor structure, we have measured electrical characteristics and analyzed the results for estimation of contact resistance and barrier height for ech combination of metal-n-Ge structures.

Fig. 1 shows *contact resistance change* for Al/SiN/n-Ge Schottky diode as a function of different t_{SiN} in which the barrier height is successfully modulated with t_{SiN}. Fig. 2 clearly shows that the Fermi level depinning is achieved, and there are clear correlation between metal work function and Schottky barrier height when optimized thickness of silicon nitride layer is inserted between metal and germanium. This is the first observation for Ge-metal contact characteristics.

Future study:
We will fabricate GeCMOS by using this innovative structure to fully suppressed Fermi level pinning, and see how this would imply for device characteristics. As the first step, we fabricate nMOSFET for full investigation in terms of Id-Vg, Id-Vd, series resistance, contact resistance for source and drain to channel, and transport properties which will guide us whether this approach can be used in manufacturing of Ge based CMOS integrated circuits with reduce process steps with reduced consumables.

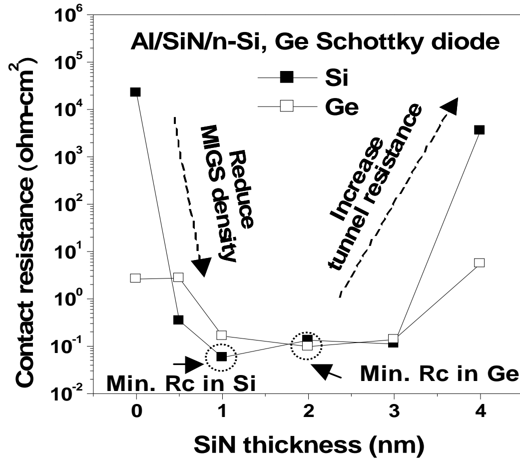

Figure. 1 R_c in Al/SiN/Si, Ge as a function of t_{SiN}.

R_c is minimum at optimal t_{SiN}=2nm for Ge due to

the balance between two mechanisms.

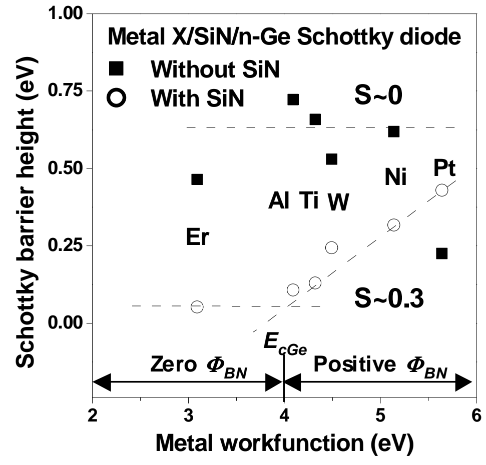

Figure 2 Barrier height as a function of metal work function