

Task ID : 425.026

Task Title : Low-ESH-Impact Gate Stack Fabrication by Selective Surface Chemistry

Deliverable: Report on the development of low ESH impact surface passivation processes to suppress defect formation and Fermi level pinning

Abstract:

A significantly higher electron mobility compared to silicon makes III-V compound semiconductors potential candidate materials for high speed, low power devices. The lack of good quality oxides on these surfaces, however, has limited their use in microelectronics. Recent advances in depositing high-k films on silicon using atomic layer deposition (ALD) could expand the use of III-V materials in high volume manufacturing. It has been demonstrated that an ALD process produces a self cleaning effect depending on the precursor, deposition conditions, and surface pre-treatment [1,2,3]. Surface preparation prior to ALD to remove native oxides and to passivate or activate III-V atoms ensures that the best possible interfaces will be made and improves reliability.

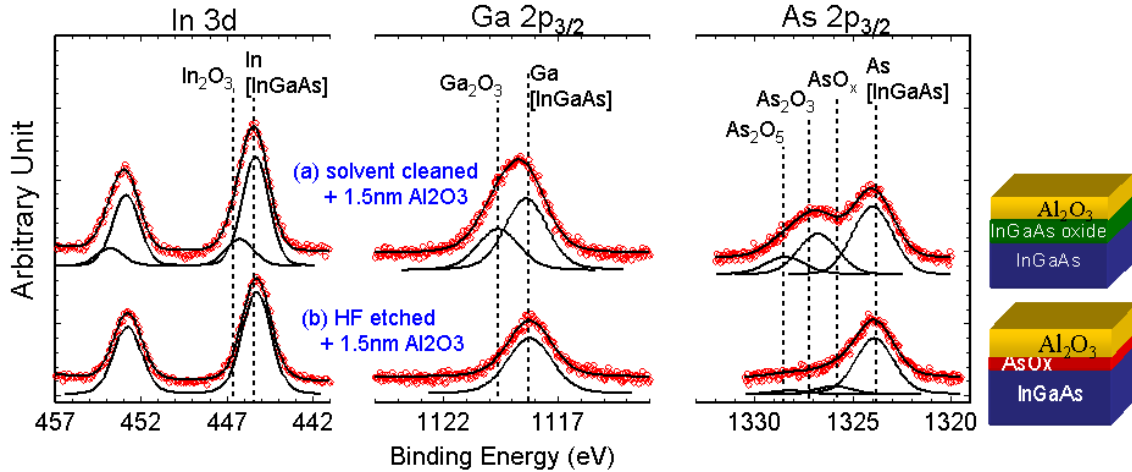
Technical Results:

This report examines high-k/III-V interface formation by aqueous HF pre-treatment and ALD  $\text{Al}_2\text{O}_3$ . Since aqueous HF processes are a standard clean for Si technology, the development of HF-based processes on III-V surfaces would minimize the changes needed to incorporate a new material set into existing fabs. Although HF is not ESH friendly, the semiconductor industry has developed the expertise necessary to use and dispose of this chemical safely. The interfacial region between the ALD  $\text{Al}_2\text{O}_3$  and III-V substrate was characterized chemically using x-ray photoelectron spectroscopy (XPS) and electrically using capacitance-voltage (C-V) and large AC signal conductance (LACS) measurements.

Epitaxial InGaAs(100) films grown on InP substrates were first degreased using standard solvent cleaning. Liquid phase HF etching was performed by immersing samples in an aqueous solution of hydrofluoric acid diluted with ultra pure water at HF (49%) to water ratios of 1:100 to 1:0 by volume at room temperature. Samples were rinsed with ultra pure water, dried with ultra pure nitrogen, and loaded into a vacuum chamber for ALD  $\text{Al}_2\text{O}_3$ . Trimethylaluminum (TMA) was chosen as the metal precursor due to its high reactivity and thermal stability, and ultra pure water vapor was used as the oxygen source. Deposition at  $170^\circ\text{C}$  produced a growth rate of  $1 \text{ \AA}/\text{cycle}$ . For interface characterization by XPS, a 1.5 nm  $\text{Al}_2\text{O}_3$  film was grown and characterized in situ. For electrical characterization, a metal-insulator-semiconductor (MIS) structure was fabricated from a 10 nm  $\text{Al}_2\text{O}_3/\text{InGaAs}$  stack.

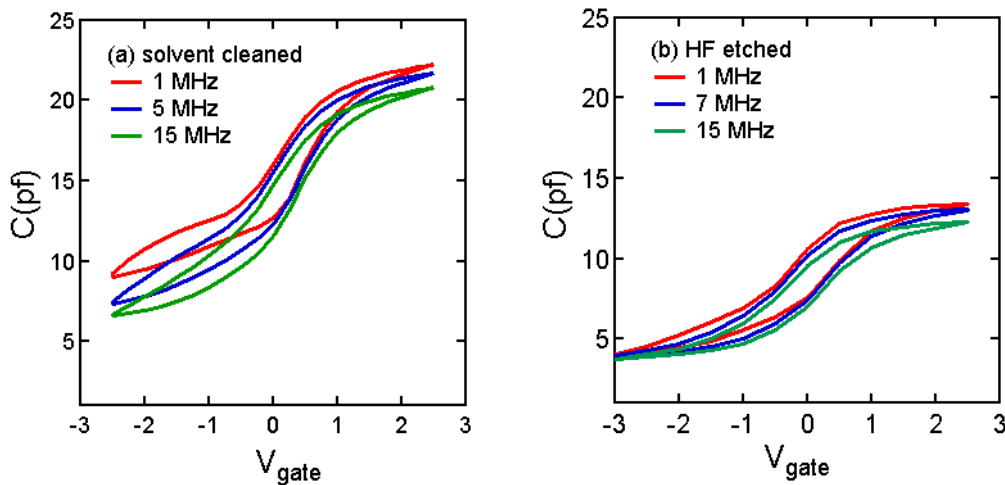
The XPS spectra in Fig. 1 show that an interfacial layer consisting of the oxides of InGaAs remained after ALD  $\text{Al}_2\text{O}_3$  on a solvent cleaned sample, while a chemically sharp interface was formed on the HF-prepared surface. Removal of the topmost native oxide layers was observed during the first 5 ALD cycles due to reaction with TMA. However, once a complete  $\text{Al}_2\text{O}_3$  layer was formed, the ALD cleaning mechanism was suppressed by  $\text{Al}_2\text{O}_3$  growth, resulting in the interfacial InGaAs oxide shown in Fig. 1(a). Aqueous HF treatment before ALD removed InGaAs native oxides and produced an As-

rich surface. The surface oxidized upon air exposure when the sample was removed from the HF solution, forming a thin  $\text{As}_2\text{O}_3$  overlayer which was mostly removed during the first ALD cycle. An interfacial layer consisting of one monolayer or less of As oxide was produced as shown in Fig. 1(b).



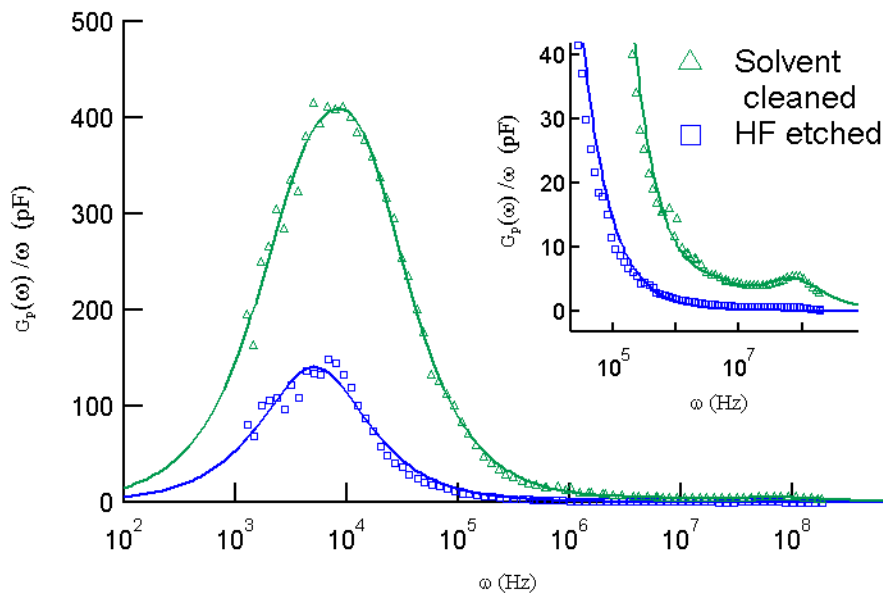
**Fig. 1.** High resolution XPS of  $\text{Al}_2\text{O}_3/\text{InGaAs}$  interface formed on solvent cleaned and aqueous HF etched surfaces.

The quality of the  $\text{Al}_2\text{O}_3/\text{InGaAs}$  interface was investigated electrically by capacitance-voltage (C-V) and a conductance technique. In a C-V measurement, the position of the Fermi-level is scanned across the bandgap, filling and emptying the defect energy levels created by dangling bonds at the surface [4]. The C-V stretch observed in Fig. 2 is an indication of surface defects. Surface defects include dangling bonds at the oxide/ $\text{InGaAs}$  interface and defects in the oxide located near the interface ( $\sim 3\text{nm}$ ) [5]. Electron-hole carriers in the semiconductor can tunnel to surface defects and recombine non-radiatively, generating heat and modifying the device biasing.



**Fig. 2.** C-V curves at 1, 5, and 15 MHz for metal-insulator semiconductor structures fabricated on an  $\text{Al}_2\text{O}_3/\text{InGaAs}$  stack prepared by solvent cleaning and aqueous HF etching.

In order to identify the source of defects at semiconductor-dielectric interfaces, a new technique based on conductance [4] was developed in our research group. A large AC signal is launched across the semiconductor-dielectric interface and the loss of e-h carriers, which represent defects, is monitored. We are just beginning to understand the chemical character of the response, but the fast defects related to dangling bonds at the semiconductor surface appear at higher frequency than the slow defects located within the oxide at the interface with the semiconductor (~3nm) [5]. The net effect of these defects manifests itself in a surface recombination velocity value. Surface recombination velocity (SRV) is a number that quantifies how fast e-h carriers are captured by defects distributed across the bandgap. The surface recombination velocity of Al<sub>2</sub>O<sub>3</sub>/InGaAs interfaces prepared by solvent cleaning was 45 cm/s. After liquid phase HF and ALD deposition, SRV decreased to less than 1 cm/s, approaching the value of an ideal interface. The major improvement is attributed to the chemically sharp Al<sub>2</sub>O<sub>3</sub>/InGaAs interface produced by the combination of HF treatment and ALD processes. The stretch in the C-V curve is related to slow bulk defects near the interface that are in the oxide.



**Fig. 3.** Large AC signal conductance curves for the same structures as in Fig. 2. The higher frequency peaks are an indication of dangling bonds at the InGaAs surface. After liquid phase removal of the oxide and ALD passivation by Al<sub>2</sub>O<sub>3</sub>, the dangling bonds are removed and defects only related to border traps inside the oxide are left.

References:

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