Task ID: 425.028

Task Title: Lowering the Environmental Impact of High-k and Metal Gate-Stack Surface Preparation Processes

Deliverable Title: Report on the test structure mask design

Abstract:

In order to characterize environmentally friendly surface preparation of high k dielectrics prior to metal gate formation, we can consider two different approaches: gate-first CMOS process and gate-last CMOS process. In the former approach, the process sequence will involve high k dielectrics deposition, metal gate material deposition, partial removal of one type of metal gate material, deposition of another metal gate material to the exposed high k dielectrics. Such partial removal of metal gate material would cause new challenge for how we can stop the removal process at exactly the surface of high k dielectrics, and how the exposed surface of high k dielectrics can maintain cleanliness before the metal deposition for the other type of MOSFET. This is truly critical in terms of controlling the interface work function of gate material which predetermine the threshold voltage of transistors. The latter process would create even more complexity. After lithographic patterning of poly silicon gate, ion implantations of source/drain dopants are made for n-channel and p-channel MOSFETs. The stability and integrity of high k materials will become significant issues to be considered. There have been a number of studies, but there have not been any systematic studies focused on thin high k dielectric film surface preparation and their sensitivity to the subsequent processes, especially for 3-dimensional device structures.

Technical Results:

In "gate-first" process, there are at least two steps in which etching of high-k is critical; one is the slight etch after metal 1 removal to prepare the surface for metal 2 deposition and the second is complete removal after patterning, with a high selectivity over SiO_2. In this project hafnium silicates and oxide films deposited on thermal oxide wafers are heat treated in reducing (gaseous) atmospheres and etched with ammoniacal solutions containing complexing agents. The possibility of galvanic corrosion between polysilicon and representative metal gate materials during high-k etching will be investigated using electrochemical techniques.

A key variable in the experiments is the ratio of polysilicon to metal. To accomplish this, test structures for corrosion studies are being created by depositing metal and polysilicon films of different thickness and patterning them to expose the sides of the films to solution. Test structures include MOS capacitors, consisting of high k before and after chemical process to investigate remaining silicate and oxide of hafnium in terms of electrical integrity of the films, implications of the processing to the film-silicon interface states in addition to physico-chemical analyses such as SIMS and XPS measurements of the film surfaces. These test structures representing high-k metal gate stack are shown in the Figure 1. While these test structures are not necessarily identical to the gate stack which will ultimately be used, they will provide sufficient insight into the dynamics to enable accurate simulation of the rinsing and drying of the many possible gate stack configurations with complex fine geometries made up of multiple materials.

Figure 1: sample AC Impedance test structure for in-situ rinse and dry monitoring for the Gate First process (left) and the Gate Last process (right). The path followed by the current between the two electrodes of the test structure is shown as a solid gray line.

Electrical test structures will be used to evaluate the effectiveness of the process steps being evaluated and to assess possible unintentional damage to the gate stack which could occur during this processing. As noted above, damage could occur to the dielectric layer itself, to the underlying junctions, to the polysilicon cap layer or to the metal gate at various times during the processing. MOS structures will be used to assess damage to the high-k dielectric. Junction diodes will be used to evaluate the impact on underlying diffusion regions and resistors will be used to assess potential corrosion on the poly and metal layers.

A large number of electrical test structures have been designed and a set of mask layers prepared. This set will allow a comprehensive evaluation of a large number of critical parameters that could be impacted by the gate stack processing. For example, the MOSCAP test structure is used to evaluate the gate dielectric. It has been laid out in various sizes as shown in Figure 2, and is used to extract the following post-processing electrical properties:

a. Capacitance of the MOS stack
b. Fixed charge in the high-k dielectric
c. High-k-semiconductor interface trap density
d. Gate leakage
e. Gate breakdown voltage

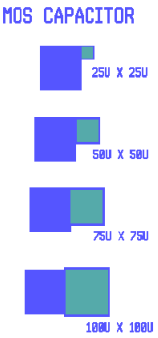

Figure 2: MOS Capacitor sample layouts

As indicated in the sample layout, square shaped MOSCAPs (25μ, 50μ, 75μ, 100μ) are included in the mask. The contact aligner mask sets that have been designed for the test structure fabrication flow are active window pattern, metal gate etch, and source-drain junction lift-off. Similar test patterns and masks have been designed for MOSFETs (to study mobility, for example), junctions (to study leakage, for example) and resistors using the four-point probe technique (to study corrosion, for example).

Additionally, joint work has started with ASM. Samples of high k material deposited using Atomic Layer Deposition have been prepared for this project. A new experimental set up is under study using a Quartz Crystal Microbalance to measure residual contaminants on the layers. This setup will be used for studying the parameters of low-water rinse process.