Lowering the Environmental Impact of High-k and Metal Gate-Stack Surface Preparation Processes

(Task Number: 425.028)

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- $50k from Stanford CIS

Objectives

- Development of non-fluoride based etch chemistries for hafnium based high-k materials
- Elimination of galvanic corrosion between metal gate and polysilicon during wet etching
- Significant reduction of water and energy (hot water) usage during rinse
- Determination of chemical and electrical characterization methodology for surface preparation of high k dielectric films.
- Validation of low resource-usage processes using Metal - high-k device fabrication and electrical characterization

ESH Metrics and Impact

- **Reduction in the usage of HF and HCl; development of environmentally friendly, non-fluoride based etch chemistries for hafnium-based high-k materials**
- **Significant reduction in water usage during rinse**
- **Significant reduction in energy (hot water) usage during rinse**
- **Reduction of rinse time leading to increase in throughput and decrease in resource usage**

Subtask 1: Environmentally Friendly Chemical Systems for Patterning Silicates and Hafnium Oxide

BACKGROUND

- **In the formation of high k- metal gate structures by the "gate first" process, etching of high k material after 'P-metal' removal to prepare the surface for 'N- metal' deposition is required. Additionally, selective etching of high k material with respect to SiO_2 is also needed**
- **Currently used chemical system for etching Hf based high-k materials is dilute HF containing HCl; however, these high k materials become very difficult to etch when subjected to a thermal treatment**
- **HF based systems appear to induce galvanic corrosion of polysilicon, which is in contact with metal gate materials; reducing the oxygen level of HF has been recommended to reduce corrosion**

Materials and Experimental Procedures

- **Materials**

  300 mm ALD HfO_2 wafers:
  - **Provided by ASM**
  - **Film Thickness: ~ 230 Å**

  300 mm ALD $HfSi_{0.74}O_{3.42}$ wafers:
  - **Provided by ASM**
  - **Film Thickness: ~ 240 Å**

- **Experimental Procedures:**
  - **Wafer was cleaved into 2 x 3 cm pieces for testing**
  - **Cleaned by IPA, rinsed with DI water and dried by N_2**
  - **Etch rate determined from thickness measurements made by spectroscopic ellipsometer (J. A. Woollam Co.) at 5 different locations**
  - **Heat treatment and reduction tests were conducted in a tube furnace;**

    50% N2 and 50% H2 gas mixture was used for reduction tests
  - **Dilute HF was used for baseline etch rate measurements; ammonium hydroxide was tested as an alternate etchant**

Baseline Etch Tests on ALD HfO_2 in Dilute HF Solutions

HF concentration (%)	Temperature (℃)	ER_{HfO2} (Å/min)	Selectivity $ER_{HfO2}:ER_{SiO2}$
0.01	25	1.5	4.8 : 1
0.1	25	4.1	2.2 : 1
1	25	27.6	0.5 : 1

- **Better etch selectivity of HfO_2 (with respect to SiO_2) at low concentrations of HF---trend in line with literature data for MOCVD HfO_2**

Wet Etching of ALD $HfSi_xO_y$ in Dilute HF Solutions

HF concentration (%)	Temperature (℃)	Reduced in $50\%H_2/50\%N_2$	$ER_{HfSixOy}$ (Å/min)	Selectivity $ER_{HfSixOy}:ER_{SiO2}$
0.01	25	No	2.2	7.1 : 1
0.1	25	No	23.2	12.6 : 1
1	25	No	328.4	5.3 : 1
0.1	400	No	23.8	12.9:1
0.1	400	Yes	22.8	12.4:1

- **Hafnium silicate etches at a higher rate than HfO_2 in dilute HF solutions**
- **Heat treatment in hydrogen does no affect the etch rate of hafnium silicate significantly**

Alternative Etch Chemistries for Hafnium Oxide and Silicate

- Literature data indicates that dissolution of metal silicates such as copper silicates is possible in ammoniacal solutions with a pre-reduction treatment in H_2/N_2 or CO/CO_2
- First set of experiments carried out on hafnium oxide and silicate films exposed to $50\%H_2/50\%N_2$ at different temperatures for different duration
- Films subsequently immersed in ammonium hydroxide solutions

Feasibility of Etching of HfO_2 and $HfSi_xO_y$ in Ammonical Solutions Using a Pre-reduction Treatment

Reduction Temperature (℃)	400	200	100
Reduction Time (hr)	0.5	1	3
pH of Ammonium Hydroxide	9.95	13.8	
Time in Ammonium Hydroxide (hr)	1	21	
Etch Rate (HfO_2 and $HfSi_{0.74}O_{3.42}$)	insignificant		

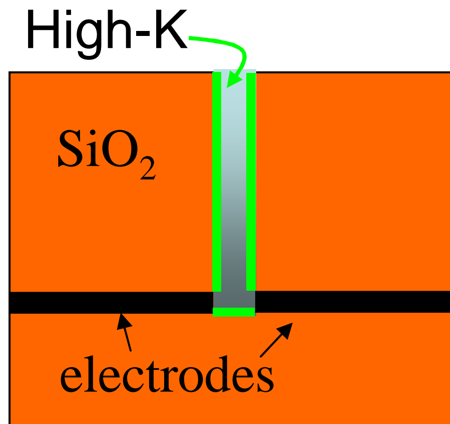
Pre-reduction in H_2/N_2 mixture appears to be ineffective in making HfO_2 and $HfSi_{0.74}O_{3.42}$ soluble in ammoniacal solutions.

Subtask 2: Low-Water and Low-Energy New Rinse and Drying Recipes and Methodologies

BACKGROUND

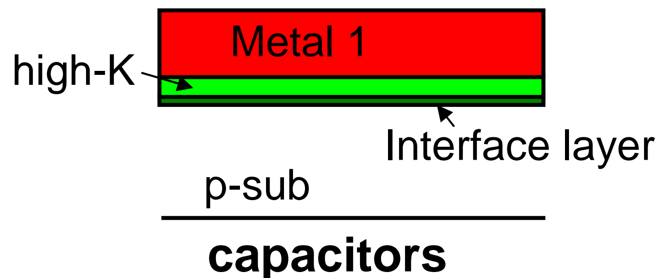
- Formation of high-k metal gate structures requires cleaning of fine geometries containing materials not traditionally used by the semiconductor industry. Wet etching must be quenched at the appropriate time
- More single wafer tools are used for cleaning, rinsing and drying because of better yield. Optimization of cycle time is critical for throughput and reduced resource usage
- Elucidating rate-limiting mechanisms to make possible multi-stage, resource-efficient recipes requires in-situ and real-time measurements and accurate simulation capabilities
- Validation of low resource-usage processes for high-volume manufacturing using electrical test structures

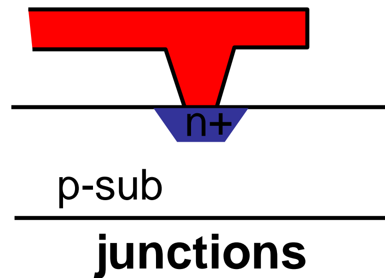
Test Structures for Experimental Work

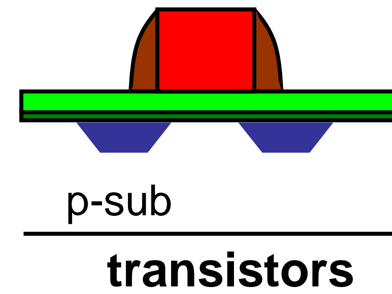


AC impedance of high aspect ratio feature to determine cleaning and drying kinetic parameters in-situ

Quartz Crystal Microbalance to determine etch rates and adsorption/desorption rates

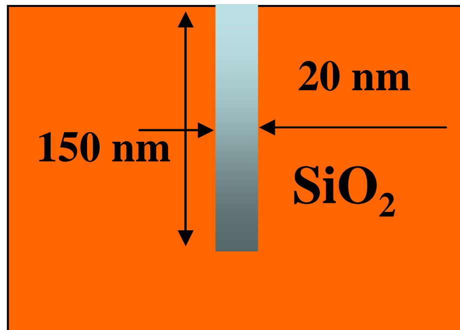




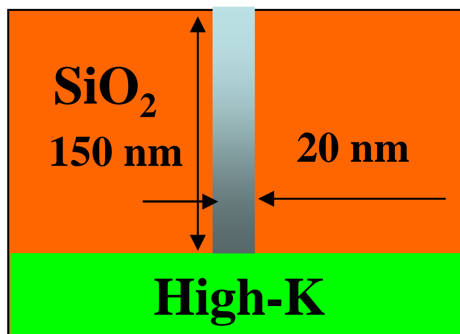


Electrical test structures (capacitors, junctions, transistors) to evaluate impact of new recipes on performance

Rinsing/Cleaning of Heterogeneous Nano- Structures



Conventional Structure



Structure with high-k

The introduction of high-k dielectric makes the surface structure heterogeneous. Rinse must clean both surfaces

A newly developed spin-rinse model was used to parametrically study the heterogeneous structure rinse.

Multi-component transport equations :

$$\frac{\partial C_i}{\partial t} = \nabla \cdot (D_i \nabla C_i + z_i F \mu_i C_i \nabla \varphi)$$

Surface adsorption and desorption:

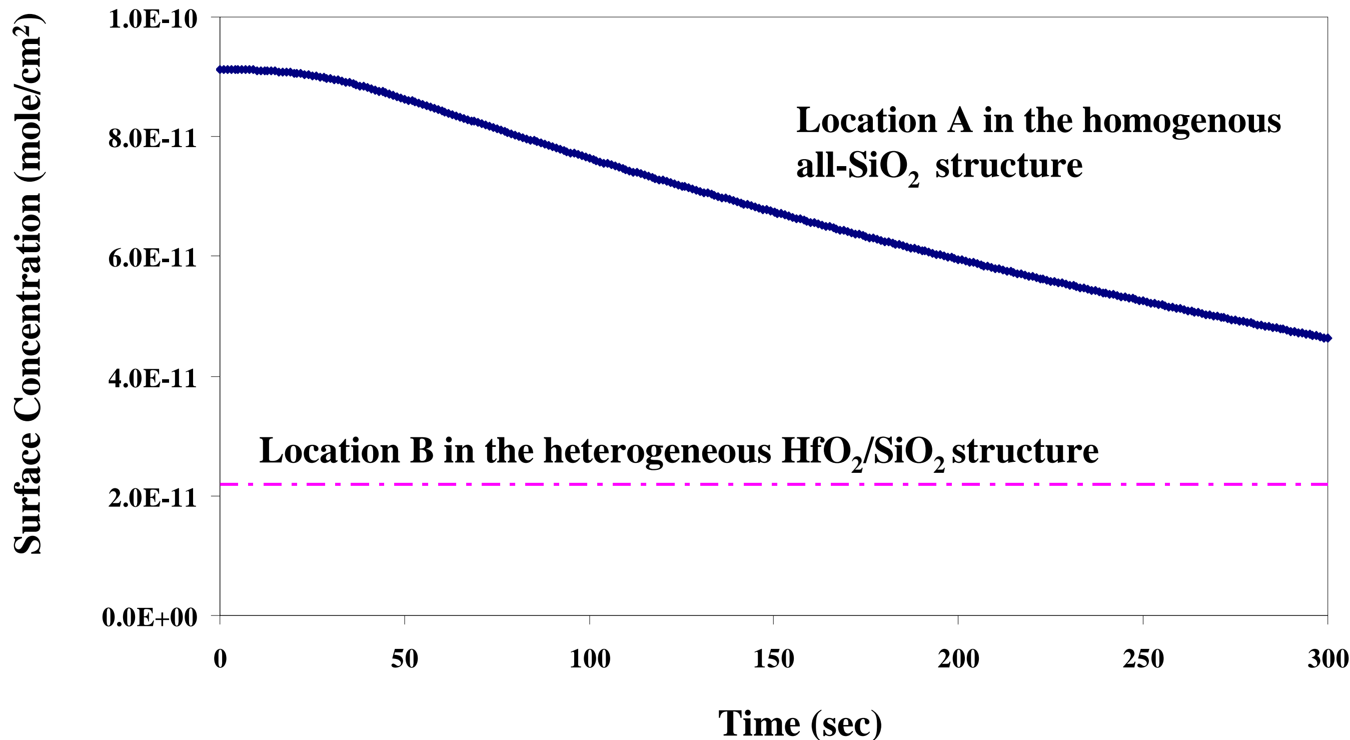
$$\frac{\partial C_S}{\partial t} = k_a C_b (S_0 - C_S) - k_d C_S$$

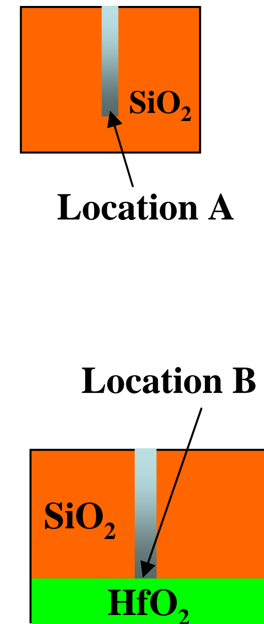
Poisson equation: $$\nabla^2 \varphi = -\frac{\rho}{\varepsilon}$$

Nomenclature

- C_i = Liquid Concentration
- D_i = Diffusivity
- C_s = Surface Concentration
- S_0 = Maximum sites available
- k_a = Adsorption coefficient
- k_d = Desorption coefficient
- Φ = Electrostatic Potential

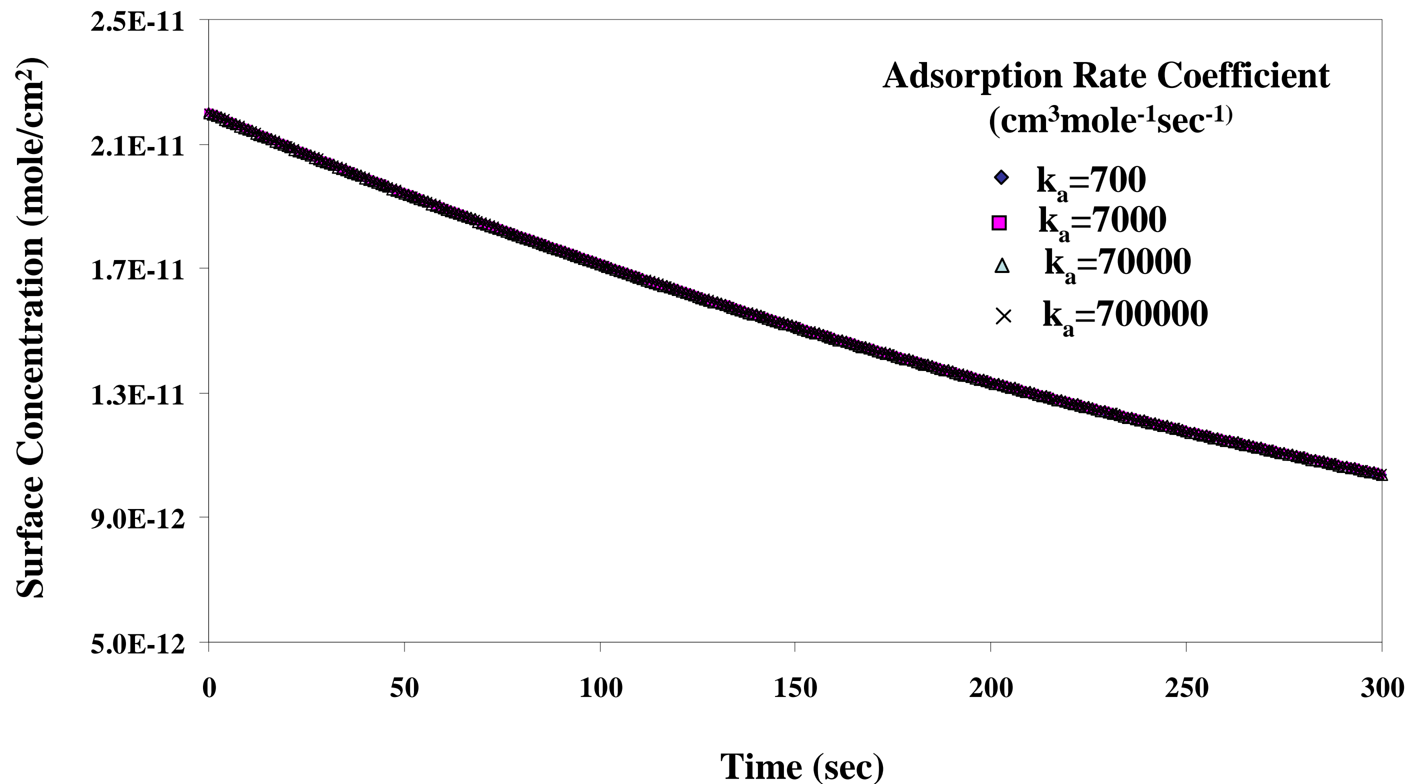
Challenges in Rinsing of Nano-Structures that Include HfO_2





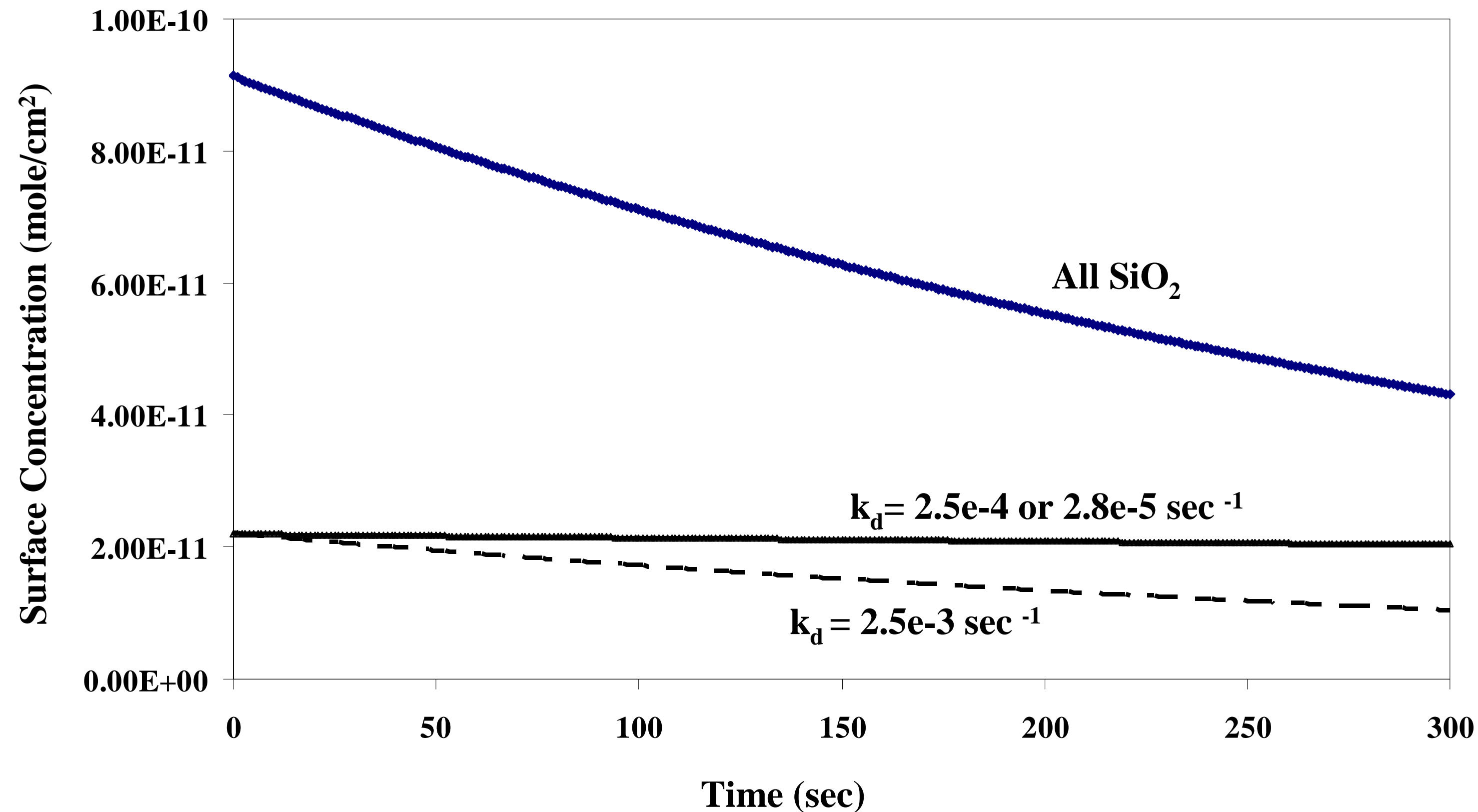
- HfO_2 has lower surface adsorption capacity compared to SiO_2. However, the sites are more energetic and adsorb contaminants more strongly (difficult to clean).
- Current rinse recipes for SiO_2 need to be modified in applications involving heterogeneous structures with Hf-based high-k dielectrics.

Impact of Adsorption Rate on the Cleaning of High-k Dielectric Nano-Structures



Adsorption of contaminants on various dielectrics appears to be thermo-dynamically favorable; it readily takes place as long as surface is not saturated.

Impact of Desorption Rate on the Cleaning of High-k Dielectric Nano-Structures



The desorption dynamics play a key role in the cleaning of various high-k dielectrics (bottleneck and rate limiting in the overall process)

Electrical Tests Structures

- **Ge as a performance booster and sample novel material**
  - **High electron/hole mobility**
  - **High process compatibility**
  - **Low temperature process**
  - **Possible V_{dd} scaling for reduced power dissipation**

	Si	Ge
Electron *m* (cm^2/Vs)	1600	**3900**
Hole *m* (cm^2/Vs)	430	**1900**
Band gap (eV, 300K)	1.12	**0.66**
Dielectric constant	11.9	**16**
Melting point (^oC)	1415	**937**

- **Key challenges: Interface property of Ge MOS gate stack**
  - **GeO_2 is regarded as a promising interface gate dielectrics***
  - **Since GeO_2 decomposition/GeO evaporation temperature is very low (430°C), low temperature oxidation is needed with high density of oxidant source**

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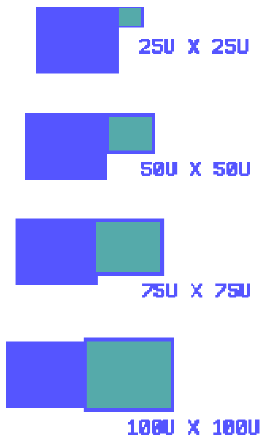
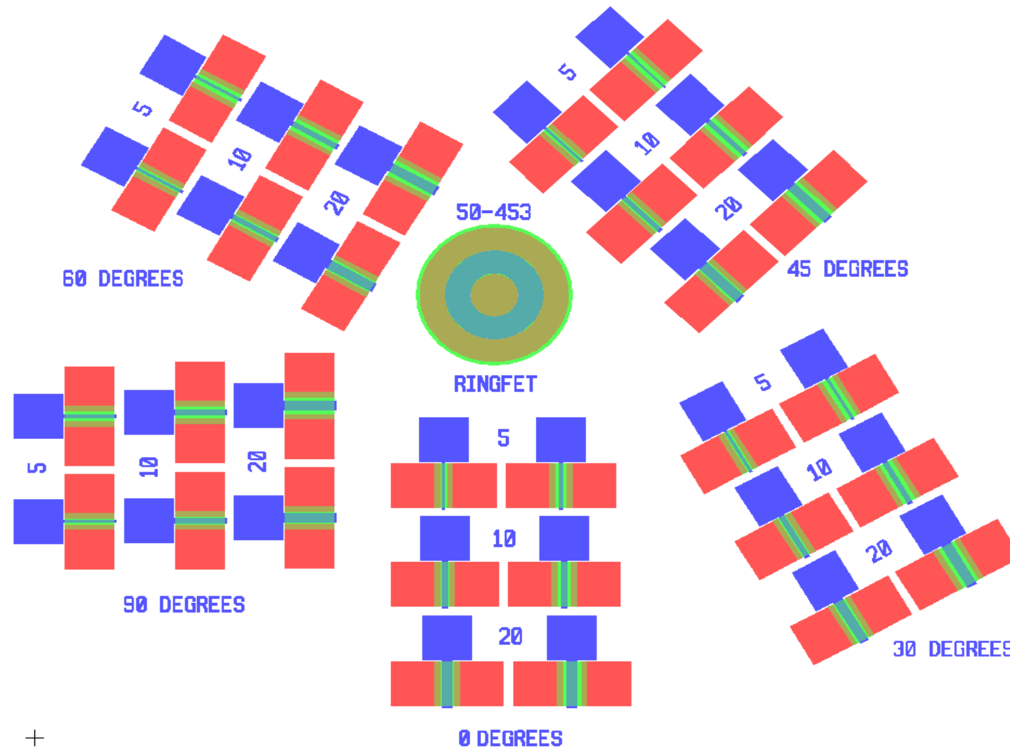
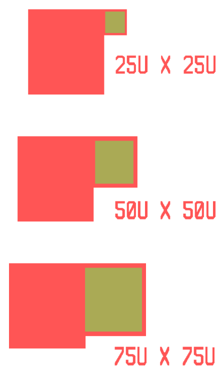
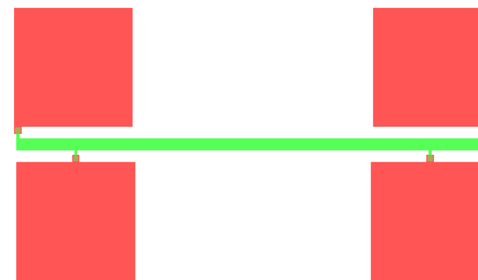
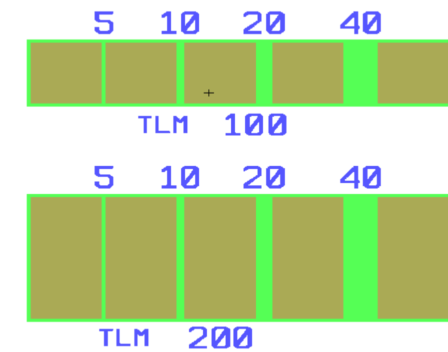
MOSFET Photolithography Mask Design









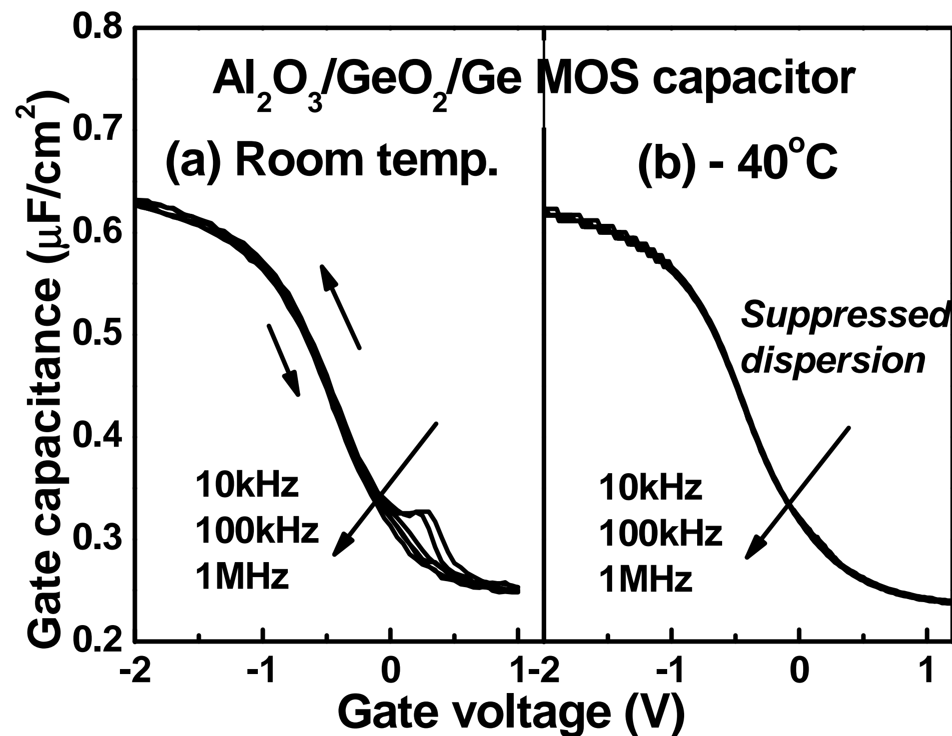


Experiments: Baseline of Cleaning Process using Capacitor Test Structures

- Sample preparation
  - (100) and (111) Ge surface was cleaned by PRS100 organic remover and by HCl/HF
  - Surface was oxidized by Slot-Plane-Antennal (SPA) radical oxidation system
    - Thermal oxidation was also done as a reference
- Electrical property
  - 5nm ALD Al_2O_3 was deposited on GeO_2/Ge
  - Sputtered Al metal pad
  - 400°C FGA anneal
  - XPS was used to identify surface chemical property
  - Synchrotron radiation photoemission spectroscopy (SRPES) was used for band offset measurement

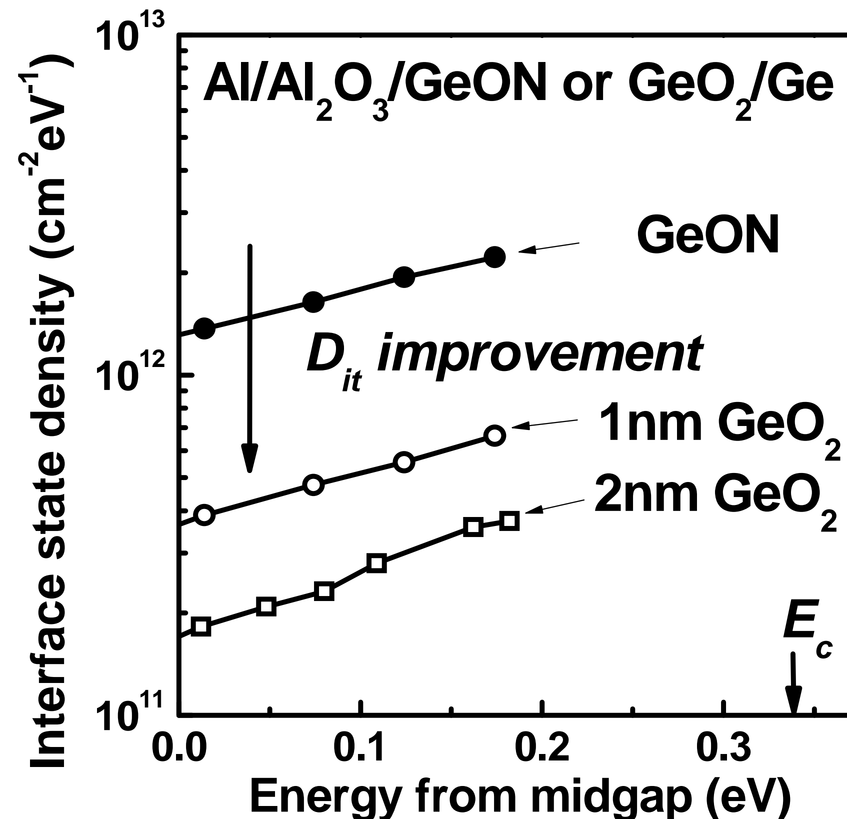
Electrical Properties of GeO_2/Ge Interface

- $Al/Al_2O_3/GeO_2/Ge$ Ge MOS capacitor:
  - 350°C ALD Al_2O_3 deposition + 400°C FGA anneal
  - Very small hysteresis and frequency dispersion
  - Low temperature measurement suppresses frequency dispersion due to minority carrier response



Interface State Density (D_{it}) of GeO_2/Ge

- **Comparison between GeON and GeO_2 using capacitor structures**
  - **D_{it} was measured by conductance method**
  - **Significant improvement from GeON**
  - **Achieved $D_{it} = 1.4x10^{11} cm^{-2}eV^{-1}$ at midgap**



Summary

- Conducted baseline etch tests on ALD HfO_2 and $HfSi_xO_y$ in dilute HF
- Investigated the feasibility of etching the materials in ammonium hydroxide solutions after a pre-reduction treatment in H_2/N_2 gas mixtures
- Determined the rinse process parameters that are needed and will be used in developing reliable and robust low-water rinse recipes for cleaning of heterogeneous nano-structures
- Benchmarked high-k process with electrical characterization using new electrical test structures

Industrial Interactions and Technology Transfer

- **Collaborative interactions with Initiative for Nanoscale Materials and Processes, INMP, at Stanford which is supported by 7 semiconductor and semiconductor equipment manufacturing companies.**
- **Interactions with ASM (Eric Shero and Eric Liu) for preparation of high-k test samples**

Future Plans

Next Year Plans

- Pre-reduction of High-k wafers in CO/CO_2 mixtures to improve etching
- Use of complexing and chelating agents such as EDTA, and disulfonic acids in ammoniacal solutions to enhance dissolution
- Development of methodology and recipes for efficient rinsing and drying of heterogeneous structures using both process simulation and experimental measurements
- Ge P/N-MOSFET fabrication and electrical characterization
  - carrier mobility analysis – substrate orientation and channel anisotropy
- Electrical testing methodology applied for comparison of etch and clean/rinse/dry of high-k dielectric using new high aspect ratio features

Publications, Presentations, and Recognitions/Awards

- **Masaharu Kobayashi, Gaurav Thareja, Masato Ishibashi, Yun Sun, Peter Griffin, Jim McVittie, Piero Pianetta, Krishna Saraswat, Yoshio Nishi, "Radical oxidation of germanium for interface gate dielectric GeO_2 formation in metal-insulator-semiconductor gate stack,"** ***Journal of Applied Physics*****, 106, 104117, 2009.**

- **X. Zhang, J. Yan, B. Vermeire, F. Shadman, J. Chae, "Passive wireless monitoring of wafer cleanliness during rinsing of semiconductor wafers,"** ***IEEE Sensors*** **(accepted).**