Task ID: 425.028

Task title: Lowering the Environmental Impact of High-k and Metal Gate-Stack Surface Preparation Processes

Deliverable title: Report on the non-fluoride chemical systems for etching of hafnium oxides and silicates: etch rate data for untreated and pretreated films

Abstract:

In the formation of high k- metal gate structures by the "gate first" process, etching of high k material after 'P-metal' removal to prepare the surface for 'N- metal' deposition is required. Additionally, selective etching of high k material with respect to SiO_2 is also needed. Currently used chemical system for etching Hf based high-k materials is dilute HF containing HCl; however, these high k materials become very difficult to etch when subjected to a thermal treatment. HF based systems appear to induce galvanic corrosion of polysilicon, which is in contact with metal gate materials; reducing the oxygen level of HF has been recommended to reduce corrosion

Key Technical Results:

A) Lowering the HF Usage:

Material used was 300 mm ALD HfO_2 wafers, film Thickness: ~ 230 Å provided by ASM.

Experimental procedure was as follows:

- Wafer was cleaved into 2 x 3 cm pieces for testing
- Cleaned by IPA, rinsed with DI water and dried by N_2
- Etch rate determined from thickness measurements made by spectroscopic ellipsometer (J. Woollam Co.) at 5 different locations
- Heat treatment and reduction tests were conducted in a tube furnace; 50% N2 and 50% H2 gas mixture was used for reduction tests
- Dilute HF was used for baseline etch rate measurements; ammonium hydroxide was tested as an alternate etchant

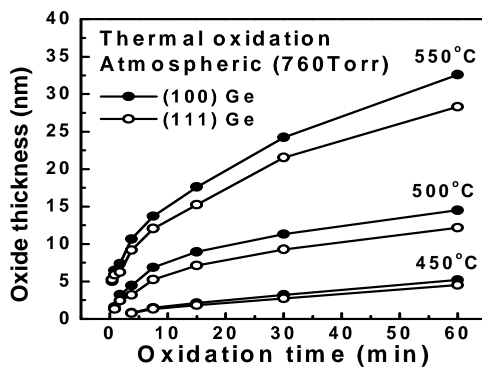
The results are shown in the following Table:

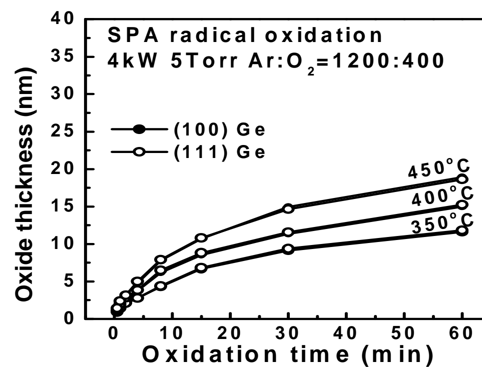
HF concentration (%)	Temperature (℃)	Reduced in 50%H_2/50%N_2	$ER_{HfSixOy}$ (Å/min)	Selectivity $ER_{HfSixOy}:ER_{SiO2}$
0.01	25	No	2.2	7.1 : 1
0.1	25	No	23.2	12.6 : 1
1	25	No	328.4	5.3 : 1
0.1	400	No	23.8	12.9:1
0.1	400	Yes	22.8	12.4:1

Literature data indicates that dissolution of metal silicates such as copper silicates is possible in ammoniacal solutions with a pre-reduction treatment in H_2/N_2 or CO/CO_2. First set of experiments carried out on hafnium oxide and silicate films exposed to $50\%H_2/50\%N_2$ at different temperatures for different duration. Films subsequently immersed in ammonium hydroxide solutions

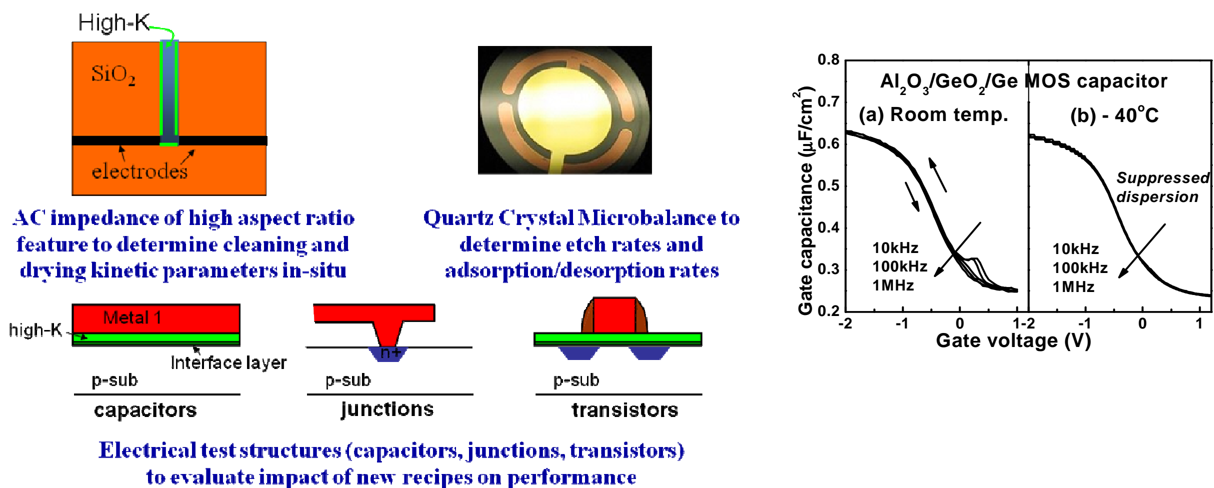
B) GeO_2 Oxidation Kinetics

Thermal oxidation and SPA radical oxidation of germanium were compared. SPA oxidation has lower activation energy (0.37eV) than thermal oxidation (1.64eV) due to high reactivity of radicals with small radius. Definite orientation dependence was observed for thermal oxidation of germanium as compared to SPA radical oxidation which does not show any substrate orientation dependence. XPS, Ellipsometry, AFM were used in this analysis.





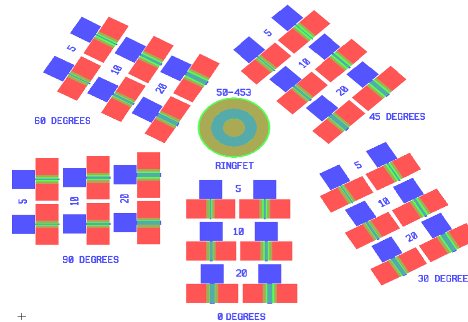
C) Test Structure Design and Development



Electrical analysis of MOSCAP fabricated using GeO_2 IL + Al_2O_3 gate dielectric and Al metal gate provided well behaved CV characteristics, negligible hysteresis and frequency dispersion (10 kHz-1MHz) and low D_{it} (evaluated using conductance method). Very low (-40C) temperature measurement of CV characteristics suppresses frequency dispersion

due to minority carrier response. XPS was used to confirm that Al_2O_3 high-k prevents thermal desorption of GeO_2 IL below 600C which is beyond the thermal budget for germanium MOSFET processing.

EELS analysis was used to obtain a band gap estimate of 5.5 eV for GeO_2. Conduction and valence band offsets of 1.2±0.3 and 3.6±0.1 eV satisfies the criterion of band offset > 1eV to suppress gate leakage. MOSFET Photolithography masks have been designed and analysis is underway to study the impact of this high quality GeO_2 on the mobility of charge carriers for both holes and electrons.



D) Summary:

- Conducted baseline etch tests on ALD HfO_2 and $HfSi_xO_y$ in dilute HF
- Investigated the feasibility of etching the materials in ammonium hydroxide solutions after a pre-reduction treatment in H_2/N_2 gas mixtures
- Determined the rinse process parameters that are needed and will be used in developing reliable and robust low-water rinse recipes for cleaning of heterogeneous nano-structures
- Benchmarked high-k process with electrical characterization using new electrical test structures