Task ID: 425.028
Task title: Lowering the Environmental Impact of High-k and Metal Gate-Stack Surface Preparation Processes
Deliverable title: Report on the electrical characterization of high k after metal removal

One goal of this research is to develop efficient rinse processes for removal of etching residues after the high-k dielectric material etching. The approaches we have taken are using theoretical model and experiment study to determine the removal mechanisms and the bottleneck of the process, and then, by using this information, develop efficient rinses. To simulate the removal of the etching residue from high aspect ratio structure, we developed a comprehensive rinse model[1]. To use this rinse model, we have to collect the physical parameters of the materials involved in the system such as residue's adsorption and desorption rate constants on the high-k dielectric surface. Therefore, we are trying to use quartz crystal microbalance (QCM) to find these rate constants. The QCM method is chosen because its high mass resolution (< 0.4 ng/cm^2).

We used atomic layer deposition (ALD) to deposit Hafnium dioxide on top of a quartz crystal as shown in Fig. 1 (a) and (b). The Hafnium precursor is $Hf(NMe_2)_4$; the deposition temperature is 200 °C. We got 2 nm HfO2 on top of the Quartz crystal as shown in Fig. 1(c).

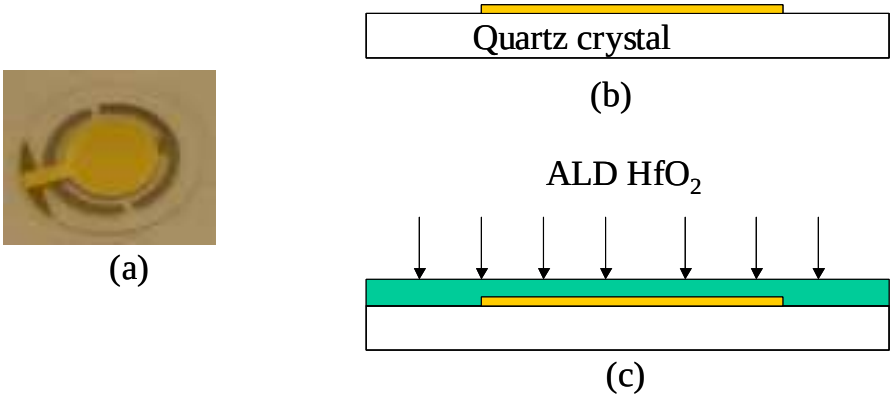


Fig. 1 Making a new crystal with HfO_2 top layer

We then used the new crystal with HfO_2 in dilute ammonium hydroxide solution to monitor the adsorption process of ammonium on HfO_2. We chose ammonium because it is one of the planned compound in our enchant mixture which should not be left on

[1] Jun Yan, Kedar Dhane, Bert Vermeire, Farhang Shadman, "In-Situ and Real-time Metrology during Rinsing of Micro and Nano Structures", Microelectronics Engineering, Feb 2009

HfO_2 surface after rinse. One of the temporal adsorption curves is shown in the Fig. 2. The solution is 1:100 (volume ratio) ammonium hydroxide and DI water mixture.

Preliminary analysis of the data in Fig. 2 shows significant amount of ammonium adsorption on HfO_2 surface. The amount of ammonium seems large enough to form multiplayer structure. The other possibility is one layer deposition but on an enlarged area due to roughness on the crystal surface. Further tests using SEM and AFM will be performed to determine which situation is real. Then we will use the correlating model to find out adsorption and desorption rate constants, and then move on to the modeling part of the research.

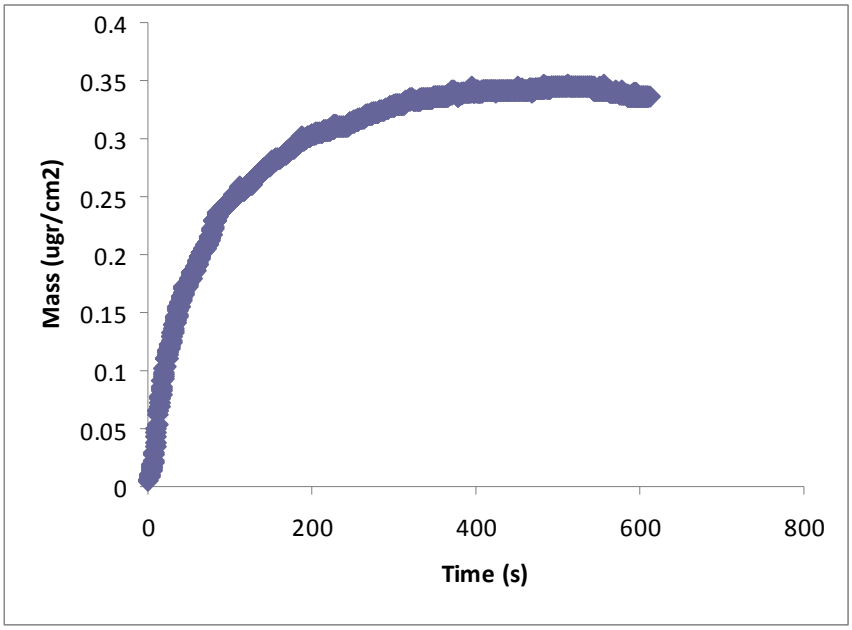
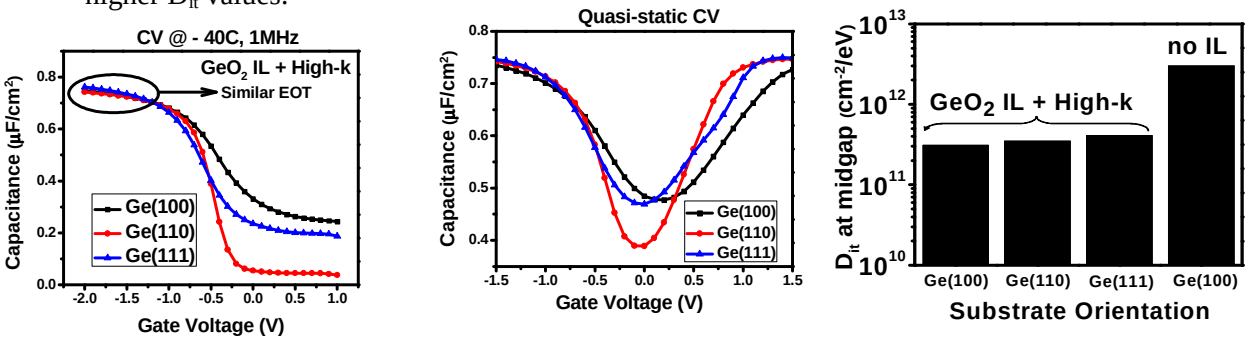


Fig.2. The adsorption curve of ammonium on HfO_2 surface

Integration of GeO_2 interfacial layer (IL) with high k (Al_2O_3) is successfully demonstrated in a gate-first high-k metal-gate MOSFET process. GeO_2 is grown by a slot-plane-antenna (SPA) high density radical oxidation process which provides substrate orientation independent interface state density (D_{it}). The GeO_2 IL provides low D_{it} of ~2 x 10^{11} cm^{-2} eV^{-1} for (100), (110) and (111) Ge substrate orientations. In order to achieve low equivalent oxide thickness (EOT) for the MOS gate stacks, this high quality IL is scaled down to 0.6nm in thickness. Electron mobility (μ_e) enhancement is observed for Ge MOSFETs with GeO_2 IL and Ge (111) substrates provide μ_e higher than universal silicon μ_e

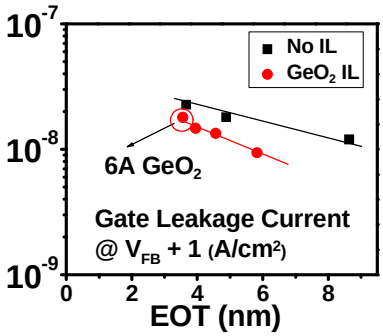
(A) Orientation independent D_{it}

Using quasi-static and low temperature (-40C) conductance measurements, interface state density for GeO_2 IL + High-k (Al_2O_3) MOS gate stacks was evaluated. Substrate orientation independent EOT and low Dit values are observed. No IL (High-k directly on Ge) samples show higher D_{it} values.



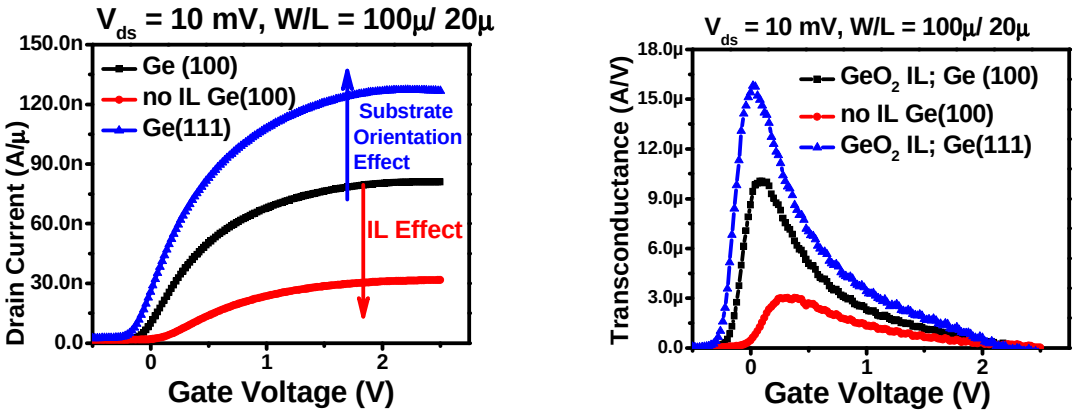
(B) IL thickness scaling

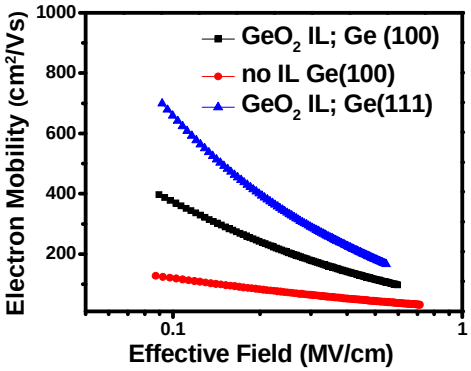
Physical thickness of this high quality GeO_2 IL is scaled to 0.6nm. This enables low EOT MOS gate stacks. Controlled gate leakage is observed for these scaled MOS gate stacks.



(C) MOSFET performance

GeO_2 IL provides enhanced drive current, transconductance and μ_e. Ge (111) substrate provides the highest μ_e due to low D_{it} and low effective mass of electrons in (111) substrate.





Efforts are underway to engineer the source/drain (S/D) junctions using plasma doping and laser annealing. This would enable ultra shallow S/D junctions with very high dopant activation (>10^{20} cm^{-3}) and higher MOSFET drive currents.