Proposed Organization of Thrust B: FEOL Processes

May 1999/Anthony Muscat, U of A

- B-1: Surface Cleaning
  - Examine Fundamentals of New Chemistries
    - Liquids
      - Water/O3 for rework and post-RIE cleaning.
    - Gases
      - HF/vapor
      - post-RIE clean.
    - Modeling
  - Quantify Acceptable Levels of Surface Contamination
    - Define a device structure, a contaminant, and an acceptable level in atoms/cm^2.
      - Ex., acceptable organic level for 30 nm gate oxide.
- B-2: Surface Termination
  - New Chemistries
    - I-CH3OH delivered by gas or liquid.
  - Surface Microstructure
    - Roughness and Uniformity
- B-3: New FEOL Materials
  - Gate Dielectric (high k)
  - Gate Electrode (metal)

Sangwoo Lim

Understanding of Electrochemical Cu Deposition on the Si Surface

Si wet etch mechanism

from the viewpoints of

- properties of chemicals (pH, redox potential....)
- micro-roughness

New passivation technology

- a factor to evaluate the passivation
- resistance to metal contamination

GOI (Gate Oxide Integrity)

- degradation of lifetime and dielectric brekdown voltage
- effect on the oxidation kinetics

High-k dielectrics

- effect on the dielectrics

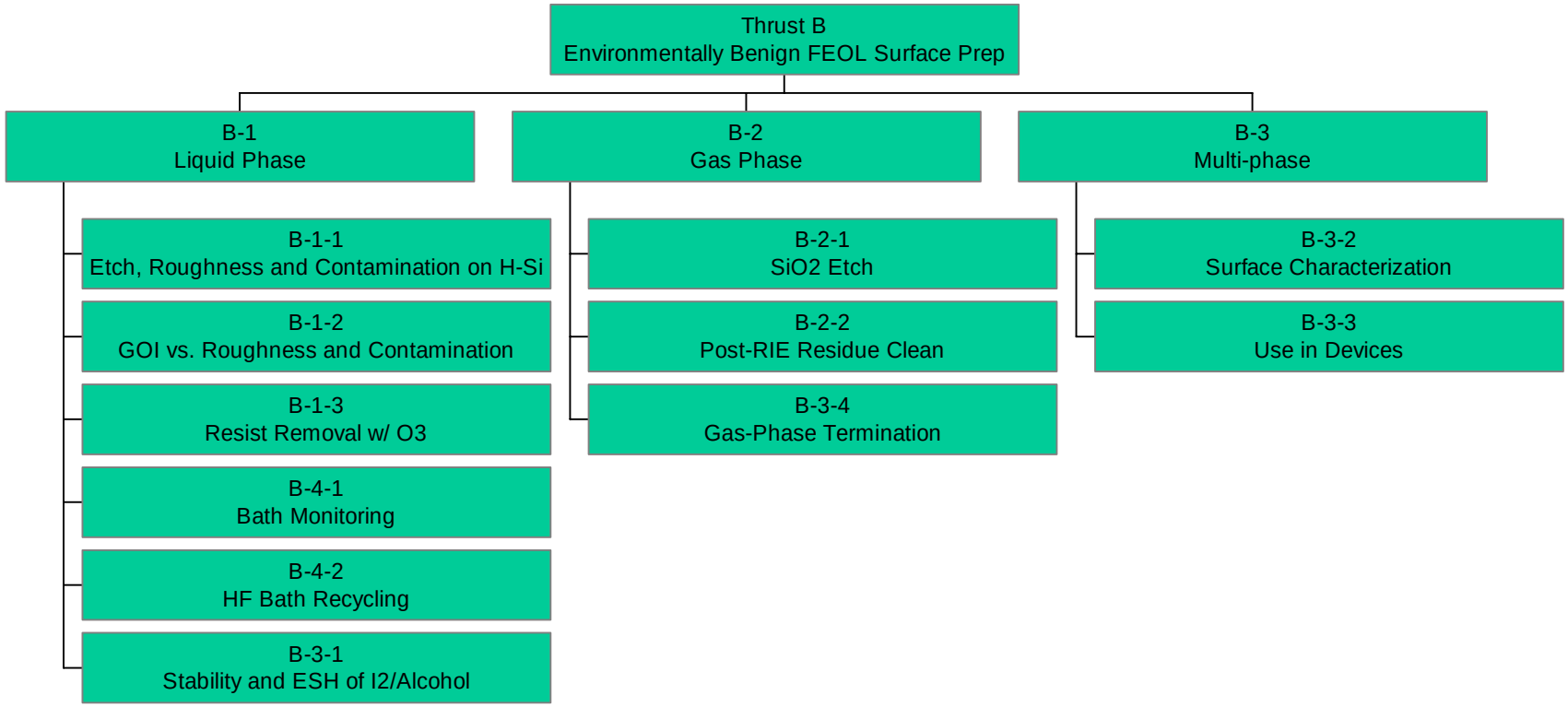
- **What are the factors to control the Cu deposition on the Si surface?**
- **What is the way to reduce the Cu contamination on the Si surface?**
- **How much Cu on the Si surface will affect the device properties?**

Understanding of Cu Deposition

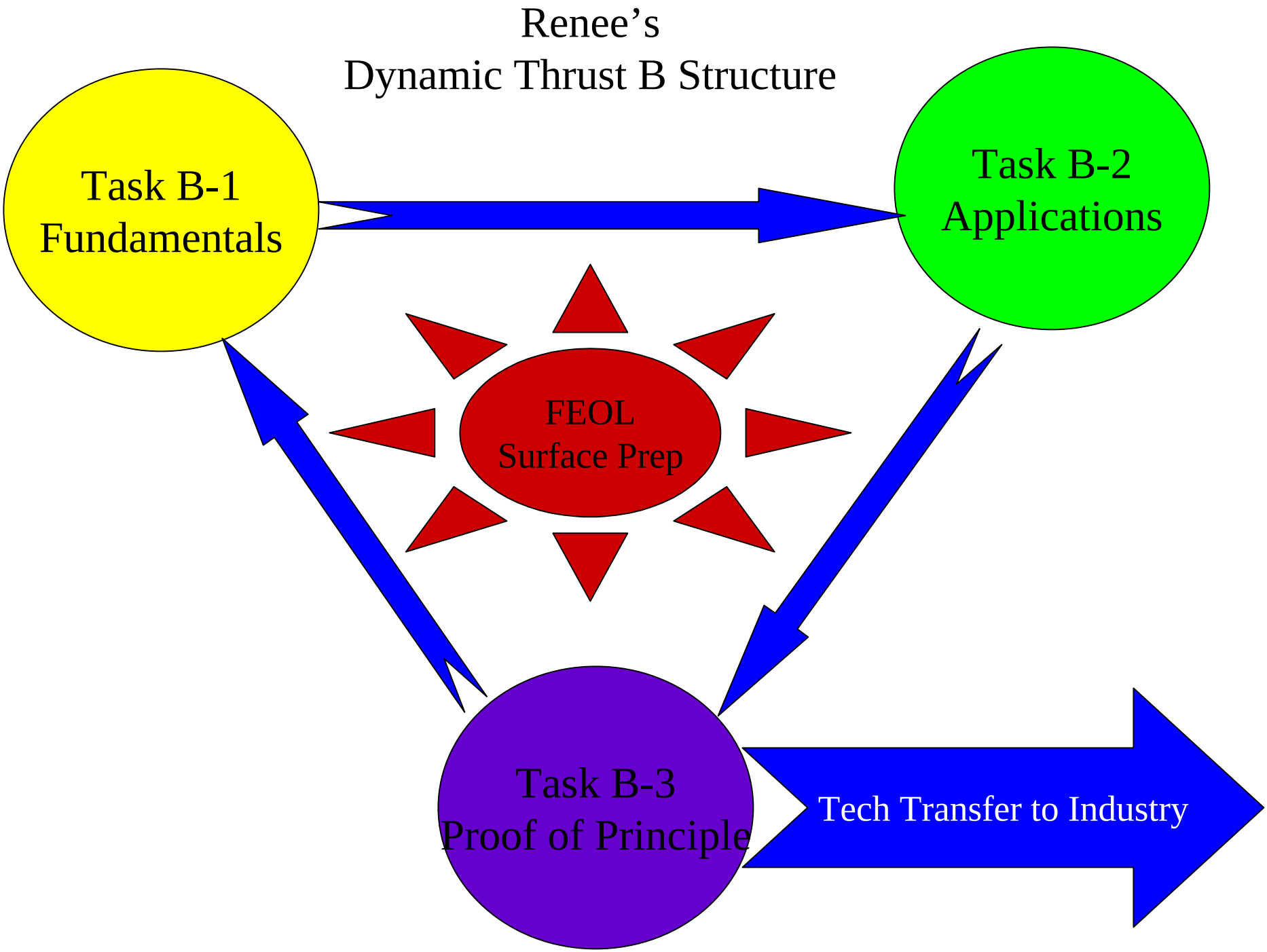
suggestion of a novel passivation → **showing the Cu (metal) contamination resistance** → **enhancement of deveice performance (high-k dielectrics)**

Proposed Structure of Thrust B

(Gerardo Montano and Casey Finstad, 5/13/99)



By connecting projects through their phases, we will tend to connect those projects with similar experimental setups and techniques. Also, liquid phase technology will tend to be more short-term than the multi-phase and (especially) the vapor-phase technologies.


Renee's
Dynamic Thrust B Structure
Task B-1
Fundamentals
Task B-2
Applications
FEOL
Surface Prep
Task B-3
Proof of Principle
Tech Transfer to Industry

New Ideas for Thrust B

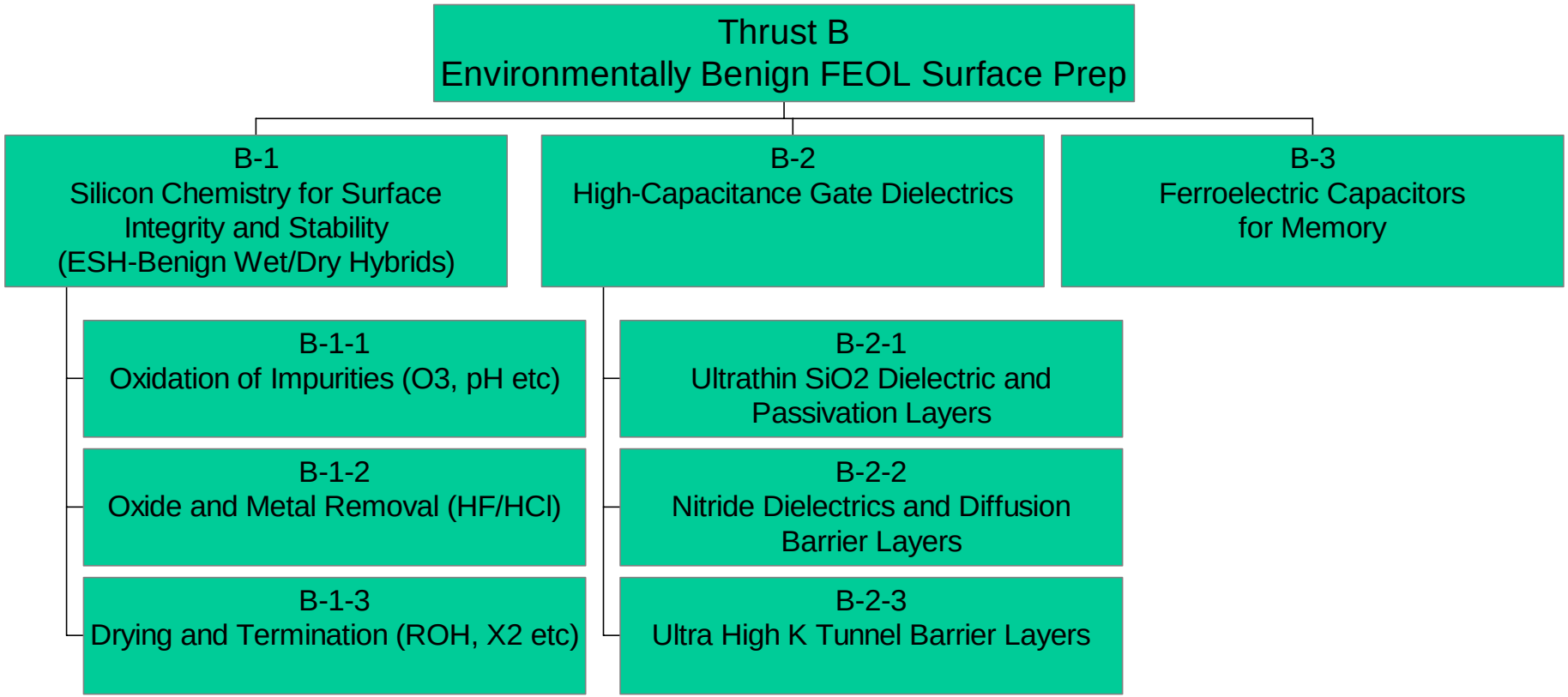
- Interface science for the gate stack materials of the future - dielectrics beyond SiO_2
  - build on/add to fundamental understanding of Si surface cleaning
  - investigate effects of Si surface preparation on novel gate dielectric electrical behavior, interface state density
  - probe the thermal stability of novel dielectrics next to Si - identify processing conditions/thermal budgets that avoid undesired interfacial SiO_2 formation, measure the kinetics of interface reactions

- Processing approaches for Pb-containing high-k dielectrics
  - investigate properties of PZT capacitors made via low thermal budget MOCVD/annealing processes that keep the Pb in the dielectric layer
  - measure Pb incorporation efficiency during MOCVD, and investigate effect of microwave enhanced CVD on Pb utilization
  - measure the kinetics of PbO-loss from PZT films during post-deposition annealing of exposed and electroded dielectrics

Revolutionary Structure of Thrust B

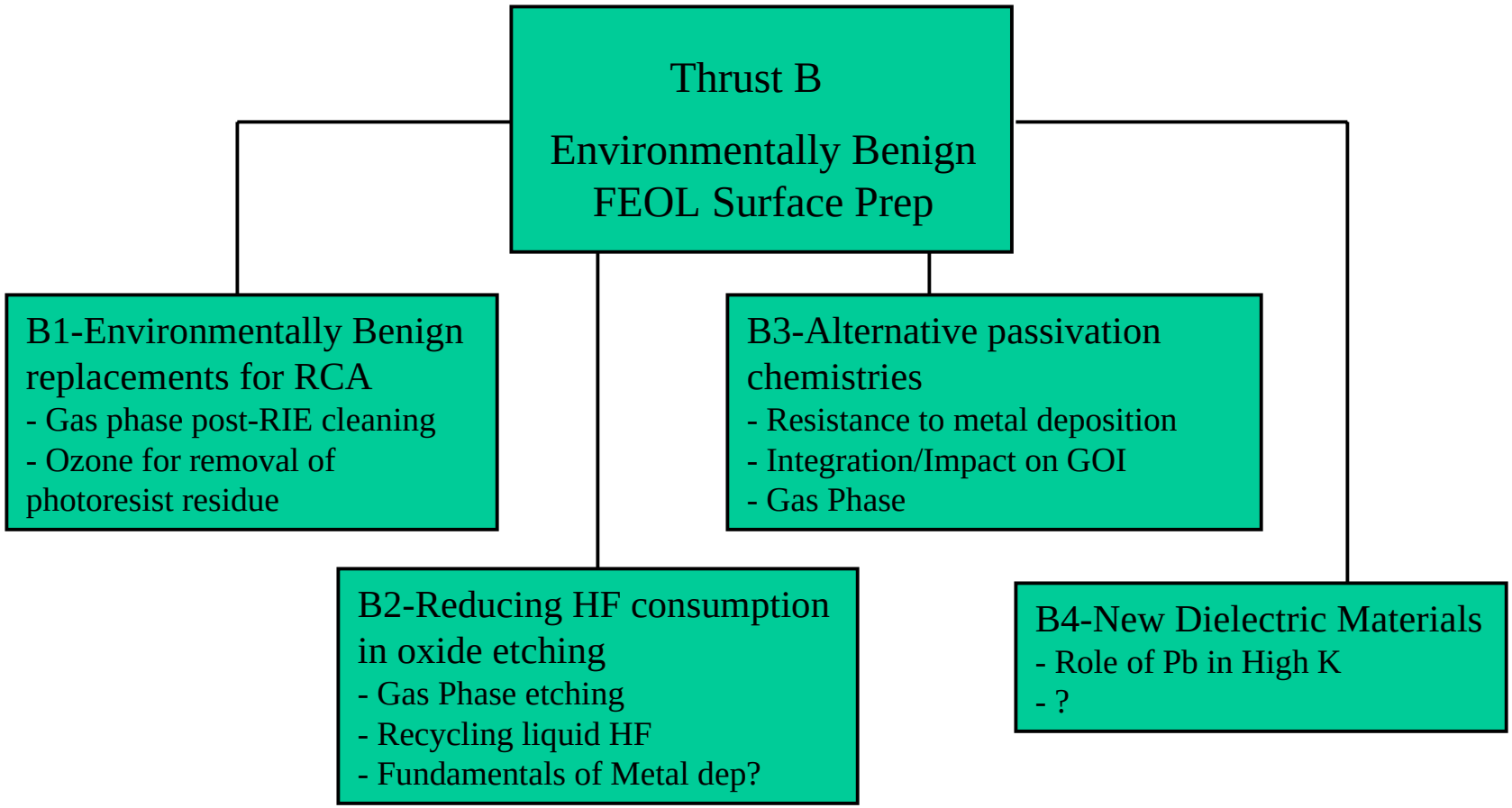
(Chidsey, 5/13/99)

Revolutionary Structure



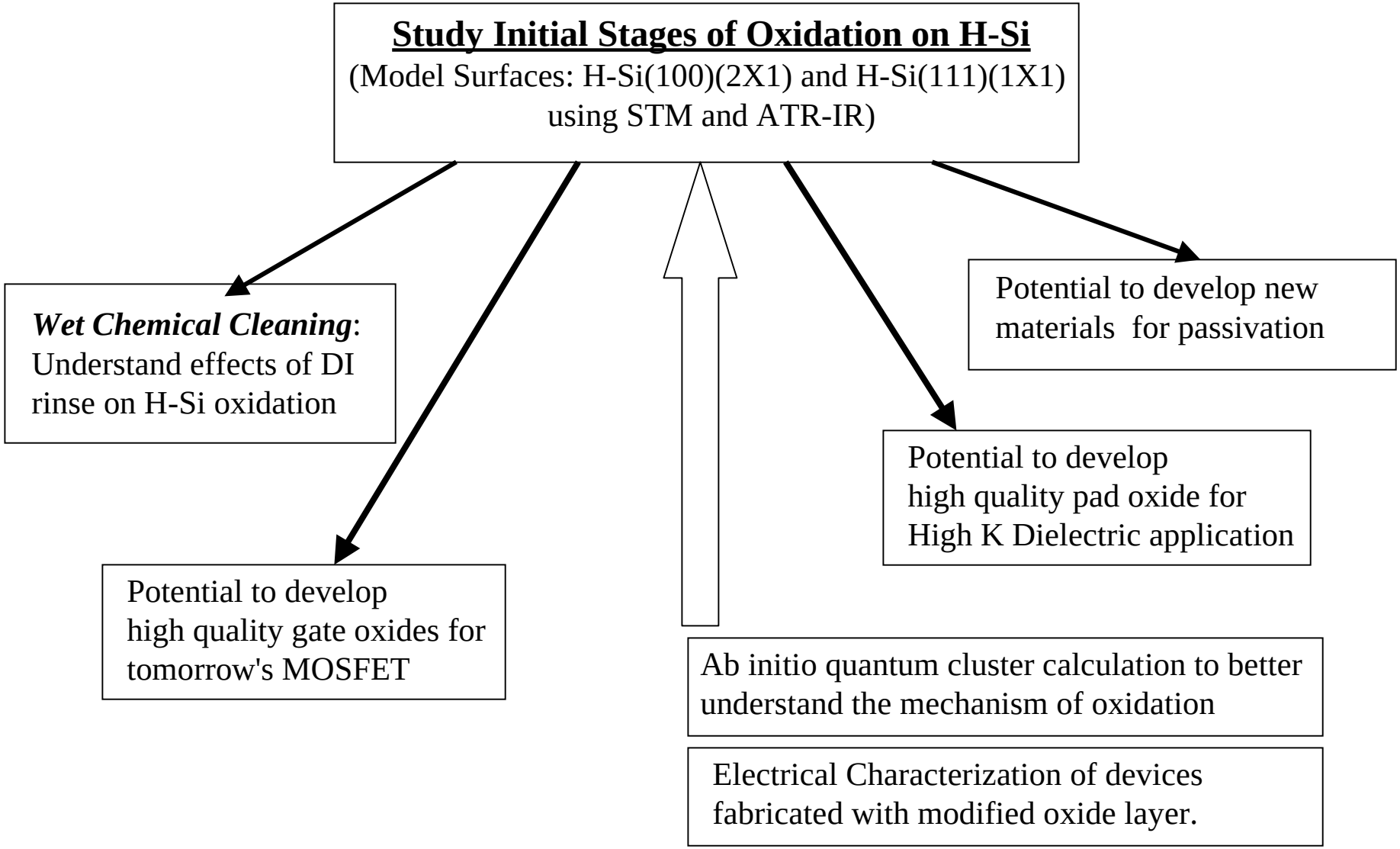
Possible New Structure of Thrust B

(Reddy, 5/13/99)



Omitted: Fundamentals of wet etching,

Impact of roughness and contamination on GOI



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