



SIA Roadmap

Surface Prep Team

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01/19/99

'98 UPDATE

- ❖ **Table 21 revised, based on international reviewers input, and forwarded on 1/11 for posting on web**
 - 3 changes recommended for '98, 2 implemented
 - footnotes D, F & G changed to improve clarity
 - organic contamination targets left unchanged - data do not support yield impact
- ❖ **Updates made in '98 focus on correcting errors**
 - numerical targets left unchanged, in the absence of a model or literature reference to support change



Table 21 Surface Preparation Technology Requirements						
Year of First Product Shipment Technology Generation	1997	1999	2002	2005	2008	2011
DRAM 1/2 Pitch	250nm	180nm	130nm	100nm	70nm	50nm
Logic Isolated Line	175nm	140nm	100nm	70nm	50nm	35nm
Front End of Line (A)						
DRAM critical area (cm ²) (B)	0.16	0.32	0.68	1.6	3.14	6.4
Logic critical area (cm ²) (C)	0.06	0.1	0.13	0.19	0.24	0.43
DRAM GOI D _o (cm ⁻²) (D)	0.06	0.03	0.014	0.006	0.003	0.001
Logic GOI D _o (cm ⁻²) (D)	0.15	0.15	0.08	0.05	0.04	0.03
Light scatterers (E)						
DRAM (cm ⁻²)	0.3	0.15	0.075	0.03	0.015	0.01
Logic (cm ⁻²)	0.75	0.5	0.4	0.25	0.2	0.15
Particle size (nm)	125	90	65	50	35	25
Critical metals (atoms/cm ²) (F)	5.0E+09	4.0E+09	2.0E+09	1.0E+09	< 1.0E+09	< 1.0E+09
Other metals (atoms/cm ²) (G)	5.0E+10	2.5E+10	1.5E+10	1.0E+10	5.0E+09	< 5.0E+09
Organics/polymers (C atoms/cm ²) (H)	1.0E+14	7.0E+13	5.0E+13	3.5E+13	2.5E+13	1.8E+13
Oxide residue (O atoms/cm ²) (I)	1.0E+14	7.0E+13	5.0E+13	3.5E+13	2.5E+13	1.8E+13
Back End of Line (J)						
Particles (cm ⁻²)	0.3	0.15	0.1	0.06	0.045	0.03
Particle size (nm)	125	90	65	50	35	25
Metals (atoms/cm ²) (K)	1.0E+12	5.0E+11	2.0E+11	1.0E+11	< 1.0E+10	<1.0E+09
Anions (atoms/cm ²) (L)	1.0E+11	1.0E+11	1.0E+11	1.0E+11	1.0E+11	1.0E+11
Organics/polymers (C atoms/cm ²) (M)	1.0E+14	7.0E+13	5.0E+13	3.3E+13	2.5E+13	1.8E+13
Oxide residue (O atoms/cm ²) (M)	1.0E+14	7.0E+13	5.0E+13	3.5E+13	2.5E+13	1.8E+13

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- A. Starting wafer up to deposition of the pre-metal dielectric
 - B. Bits/chip multiplied by the critical dimension squared
 - C. Transistors/chip multiplied by 10 times the critical dimension squared
 - D. Based on the critical area at 99% yield per critical step (with 10 critical steps in the entire flow, the total device defect density would be approximately 10 times this number); suggested short loop GOI test (includes some reliability failures): 10 Mv/cm for 100 sec.
 - E. Modeled for 99% yield, as in Table 20. 20% kill ratio assumed.
 - F. DRAM requirement for sum of Ca, Co, Cu, Cr, Fe, K, Mo, Mn, Na, Ni, W measured aftercritical clean for a gettered wafer
 - G. DRAM requirement for sum of Al, Ti, V, Zn (Ba, Sr, and Ta if present in the factory) measured aftercritical clean for a gettered wafer
 - H. Measured aftercritical clean including pre-gate, pre-poly, pre-metal, pre-silicide, pre-contact, and pre-trench fill
 - I. Measured pre-metal, pre-silicide, and pre-contact
 - J. Poly-silicide metal dielectric deposition through passivation
 - K. K, Li, Na, measured after critical clean
 - L. Cl, N, P, S, F measured aftercritical clean. Assumes no fluorinated oxide.
 - M. Measured aftercritical clean of a metallic surface region

'99 SCHEDULE

- ❖ **March 17: FEP Roadmap Team meeting**
 - definition of all table line items
 - international input on table line items
- ❖ **April 19: International TWG face-to-face**
 - review first draft
 - topical outline of the text
- ❖ **June 15: First draft complete**
- ❖ **July 8: Present Roadmap at Semicon West**
- ❖ **Aug. 30: Final draft complete**
- ❖ **Sept. 17: Document frozen**



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'99 SURFACE PREP TEAM:

Responsibility

Who

FEOL

GOI D0
light scatterers
critical metals
other metals
organics/polymers
oxide residue

Brown
Kunesh

Muscat, Bay

BEOL

particles
metals
anions
organics
oxide residue

Kunesh

Muscat, Bay

NEW

surface roughness

Rosamilia, Guan

