



Use of Air-Gaps as a Low-K Dielectric

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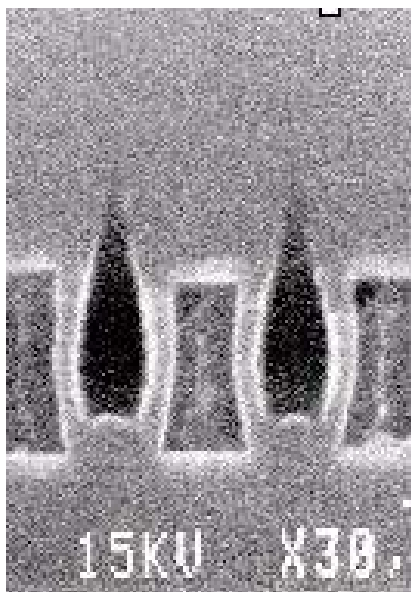


Outline

- Background and Motivation
- Electrical Performance
- Integration Issues
- Thermal Reliability
- Electromigration Reliability
- Summary



Why Air Gaps ?



- Dielectric constant, K , approaching 1.
 - Reduces dominating line to line capacitance.
 - Interlevel SiO_2 left intact.
 - Simple integration.
 - Compatible with scaling trends - air gaps easier to form with higher aspect ratios.
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- Good vehicle to study tradeoffs between performance & reliability



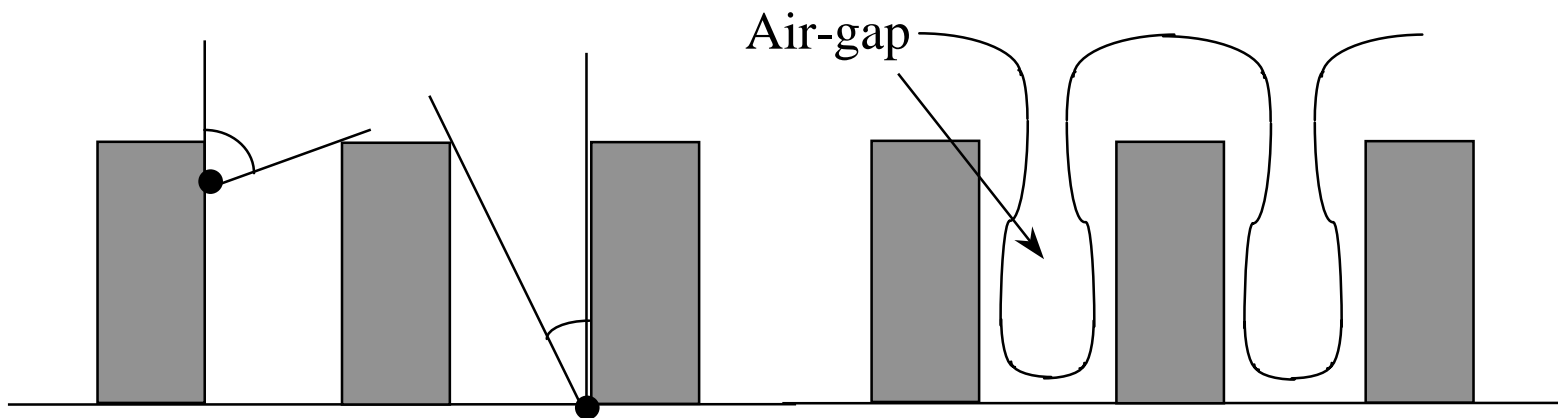
Environmental Impact

- No new materials or precursors
 - SiH_4 , O_2 , Ar
 - can use current toolsets (PECVD, HDP-CVD)
 - do not need new etch or CMP processes
- Known environmental issues
 - chamber clean: presently worked on by others



Air-Gap Formation

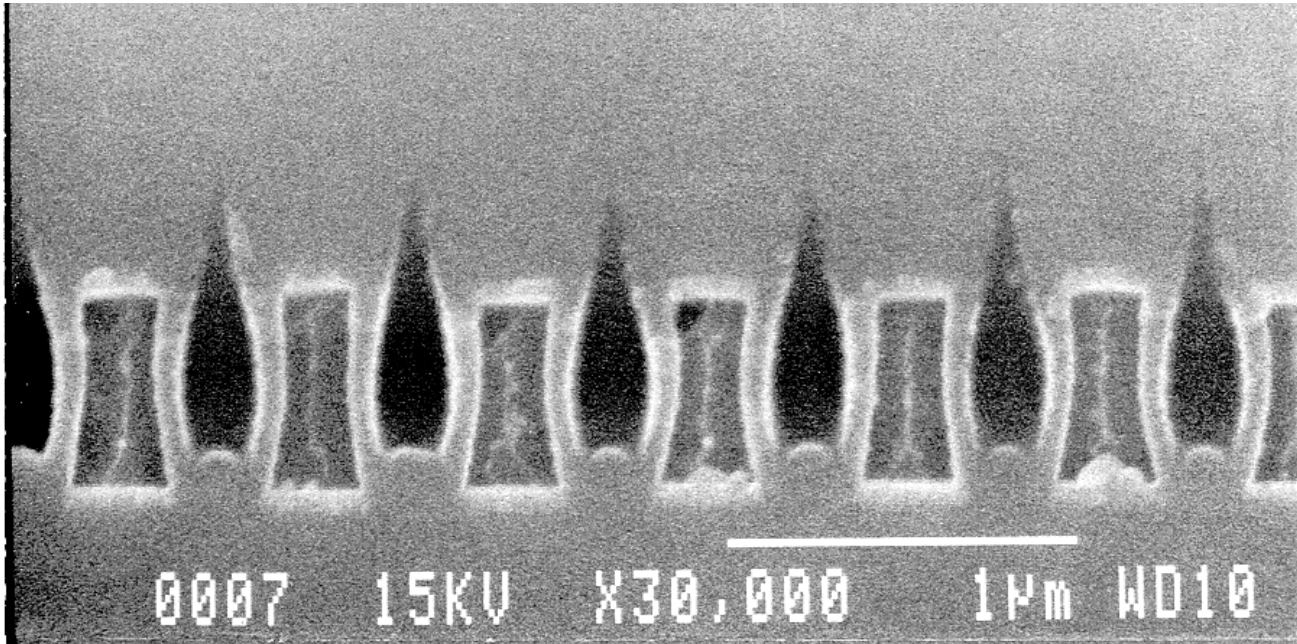
- Air-gap formed by “breadloafing” due to smaller view angle at bottom of trench.



- Greater “breadloafing” \Rightarrow Larger air-gaps



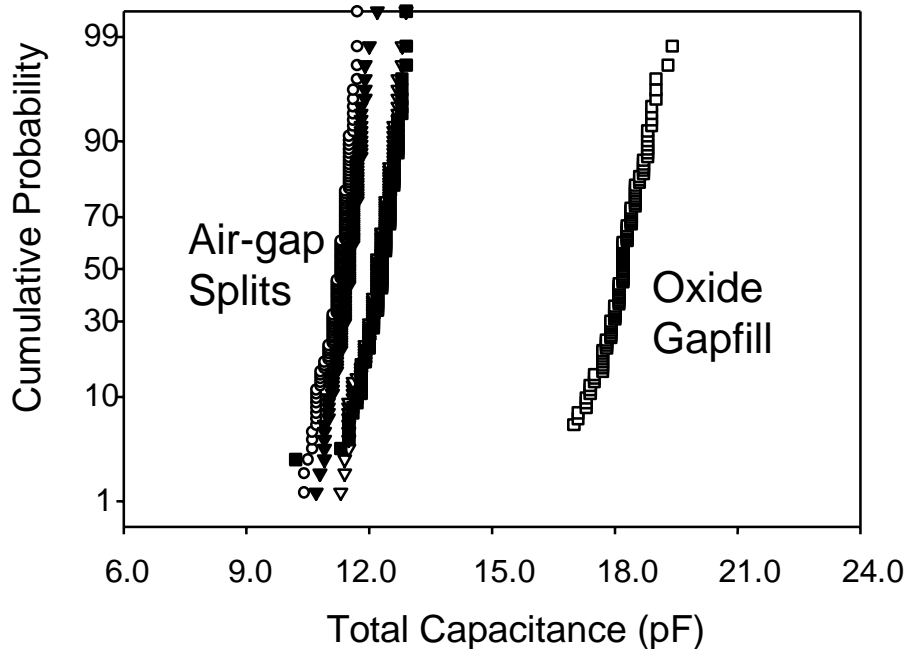
SEM of Experimental Air-Gaps



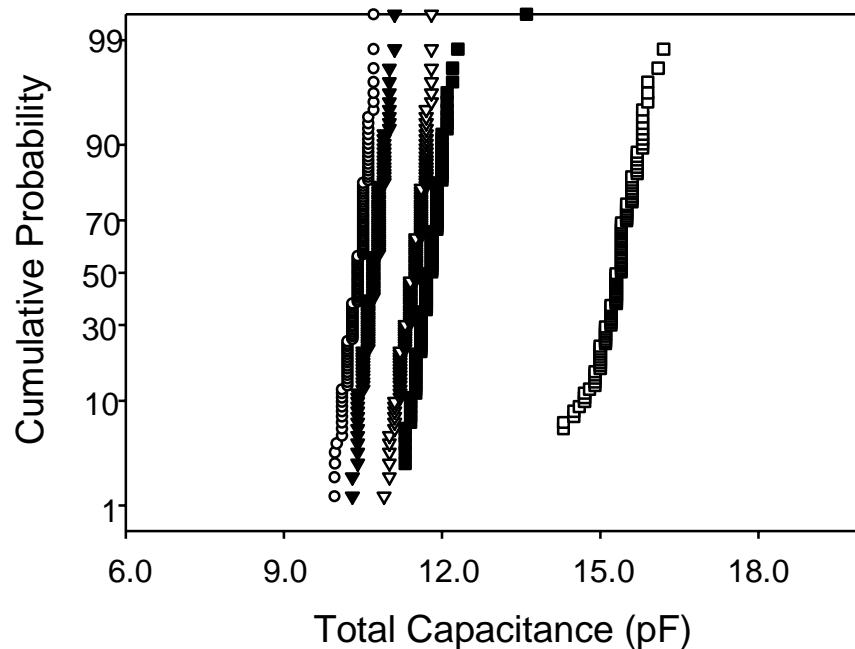


Experimental Capacitance Data

0.3um/0.3um line/space



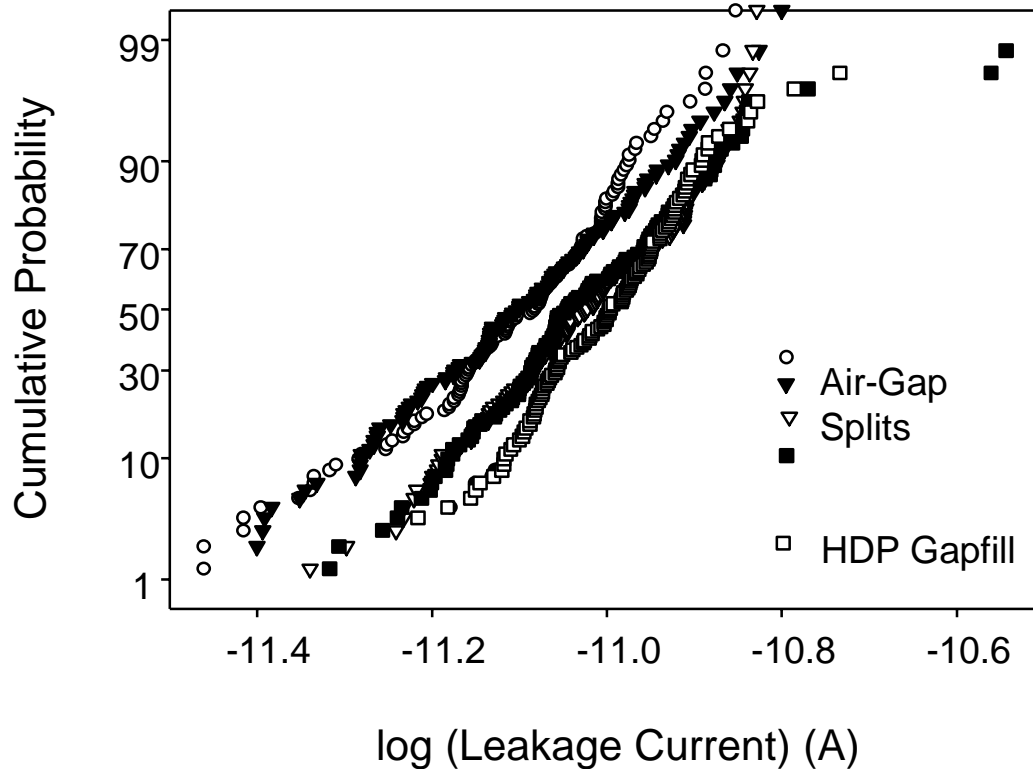
0.4um/0.4um line/space



- ~ 33 to 40 % capacitance reduction from HDP oxide gapfill for 0.3μm lines/spaces



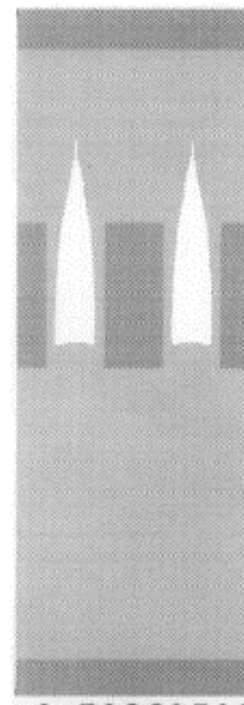
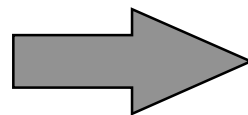
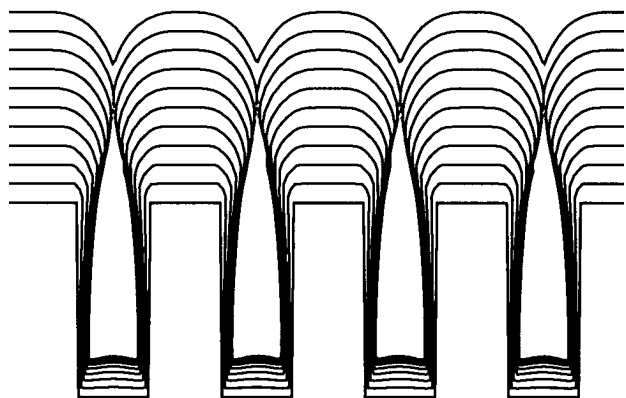
Leakage Data



- 0.3um/0.3um line/space, 6.6V applied.



Import SPEEDIE Air-gap Profile to Raphael

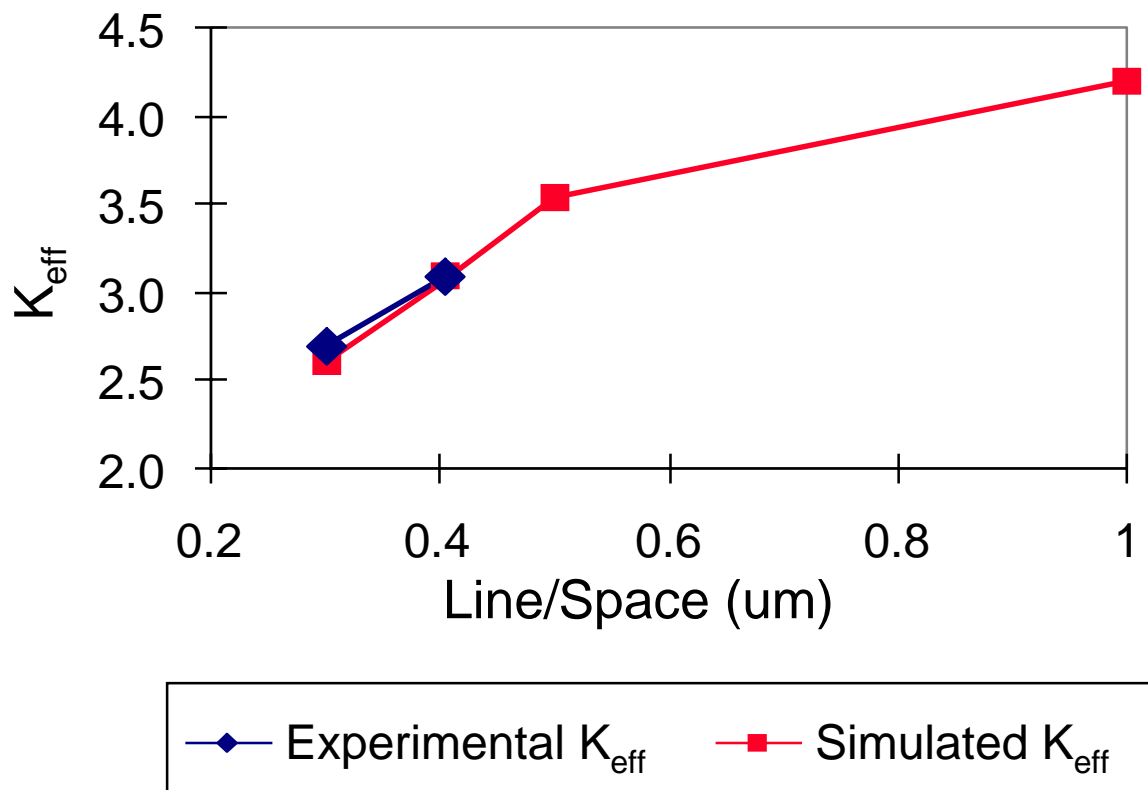


- Deposition simulated using SPEEDIE

- Capacitance extraction using TMA Raphael



K_{eff} vs. Feature Size

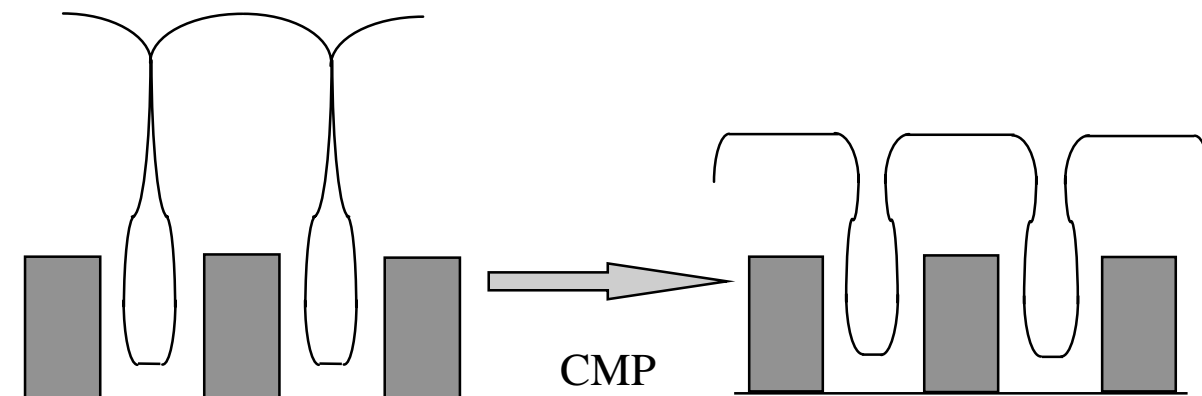


- For small pitches, K_{eff} varies linearly.

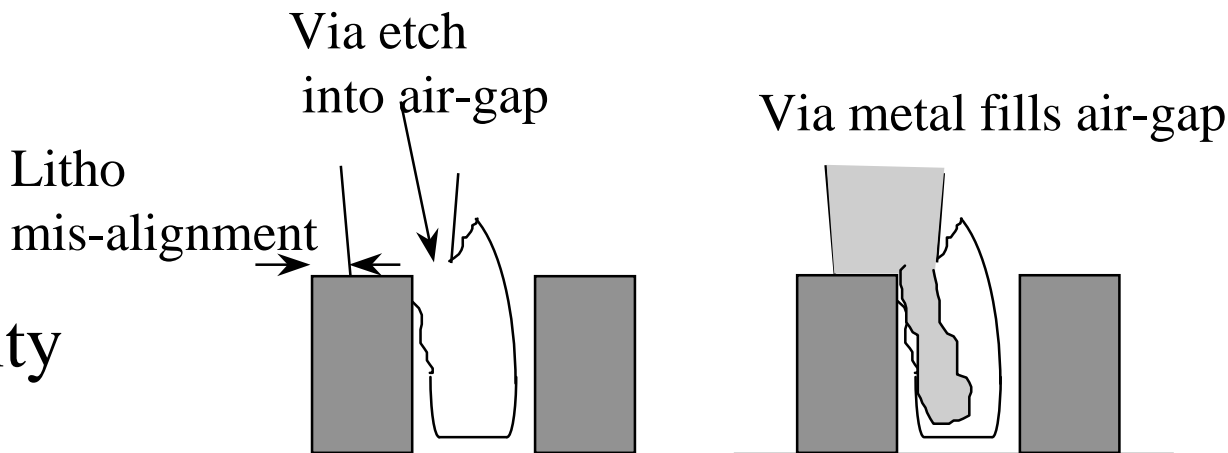


Process Integration Issues

- CMP Reliability

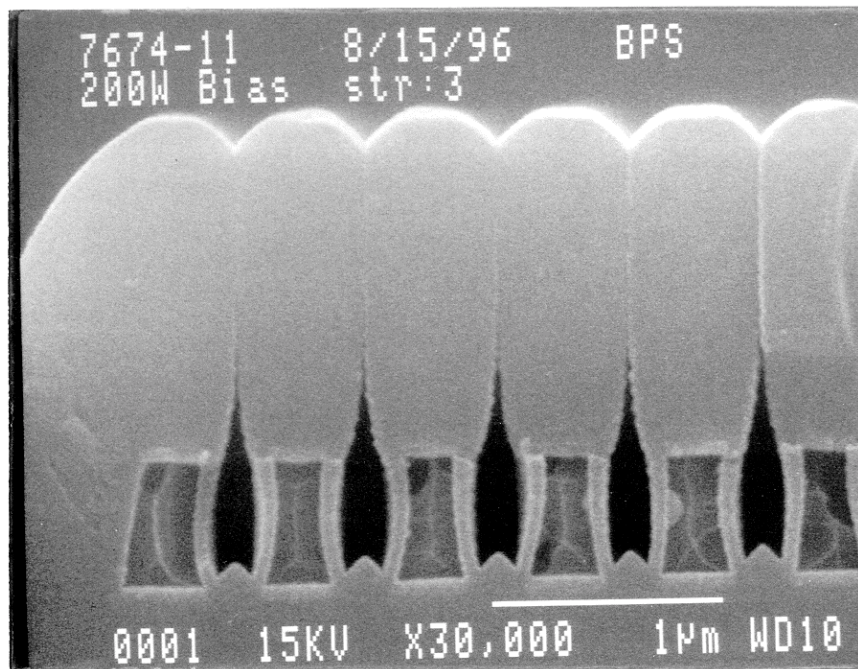


- Via Reliability

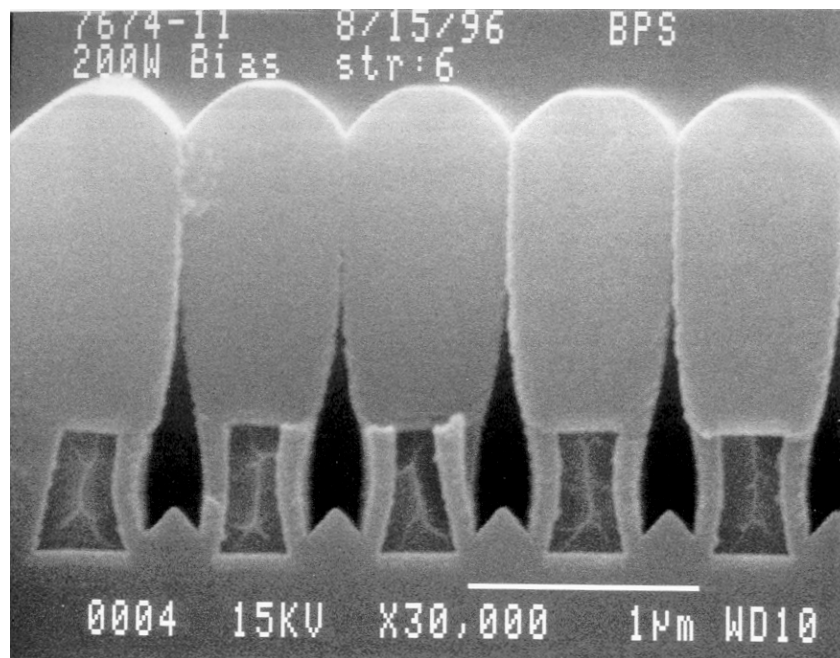




SEM Images of Seam and Void Extension



Line/Space = $0.3\mu\text{m}/0.3\mu\text{m}$



Line/Space = $0.4\mu\text{m}/0.4\mu\text{m}$

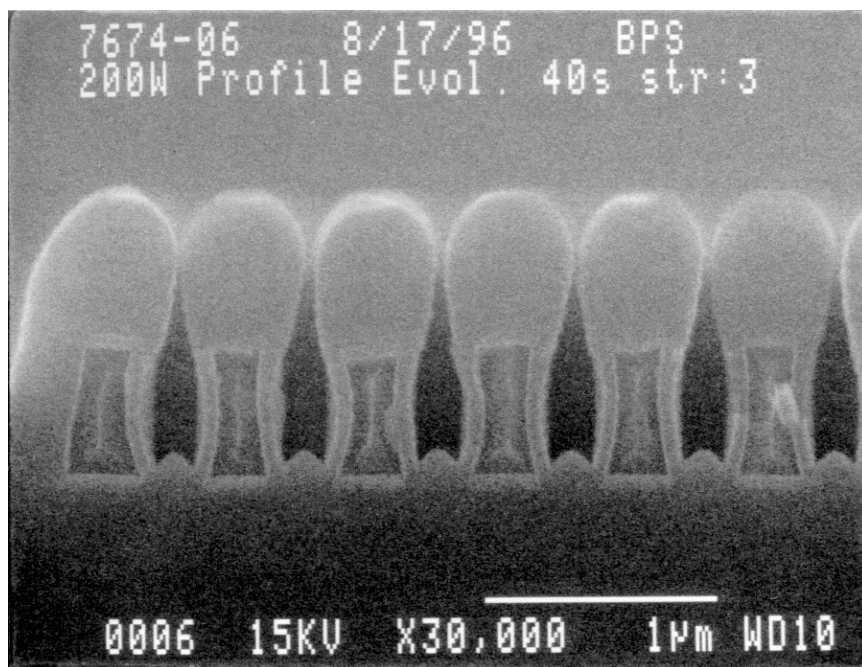


Proposed Solution: Two Step HDP CVD Process

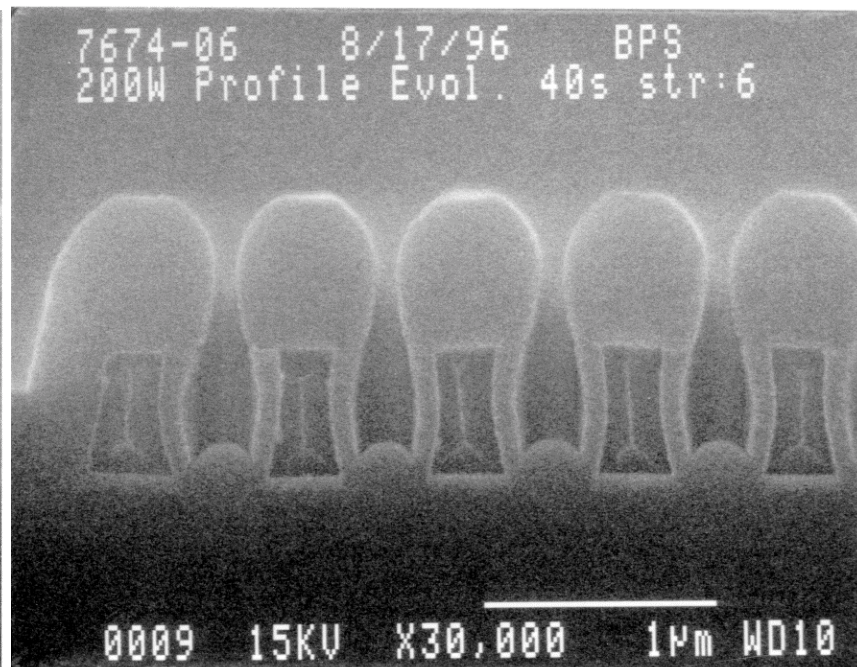
- First step : High deposition to sputter etch (D/S) ratio conditions to form initial void
 - High Gas Flows, Low Substrate Bias
- Second step : Decrease D/S ratio to prevent seam from forming, limit extent of void above metal lines, and provide local planarization
 - Low Gas Flows, High Substrate Bias



Profile After First Step



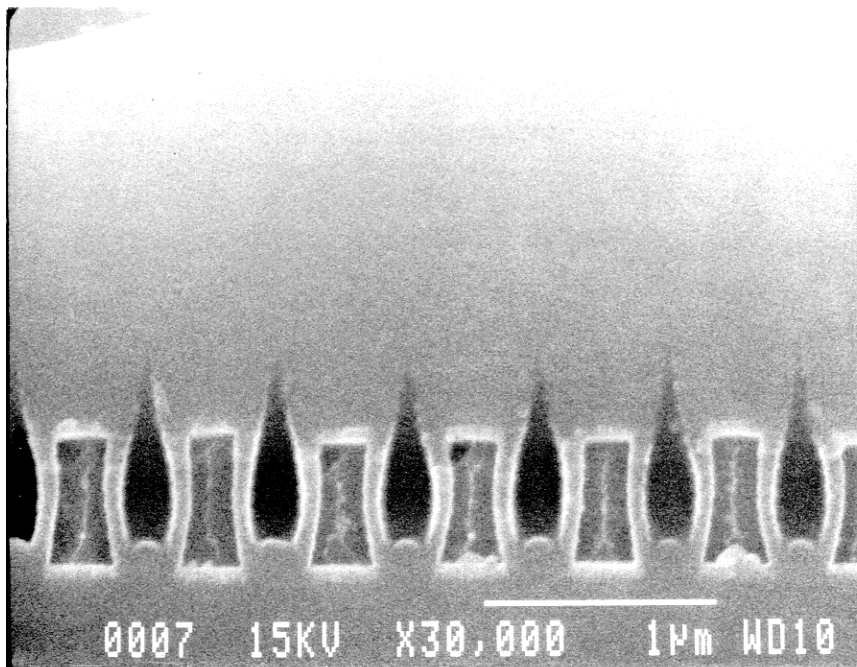
Line/Space = $0.3\mu\text{m}/0.3\mu\text{m}$



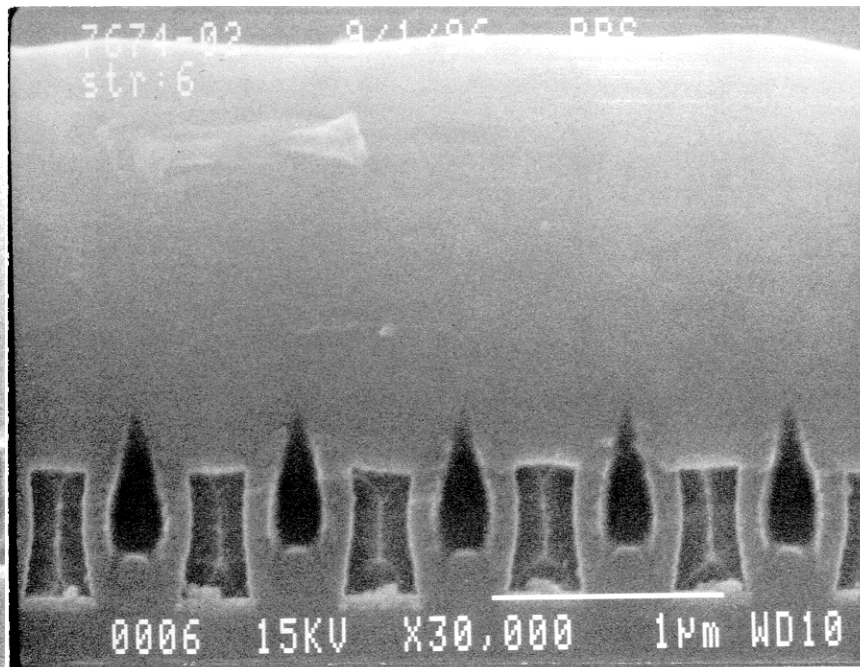
Line/Space = $0.4\mu\text{m}/0.4\mu\text{m}$



Profile After Second Step



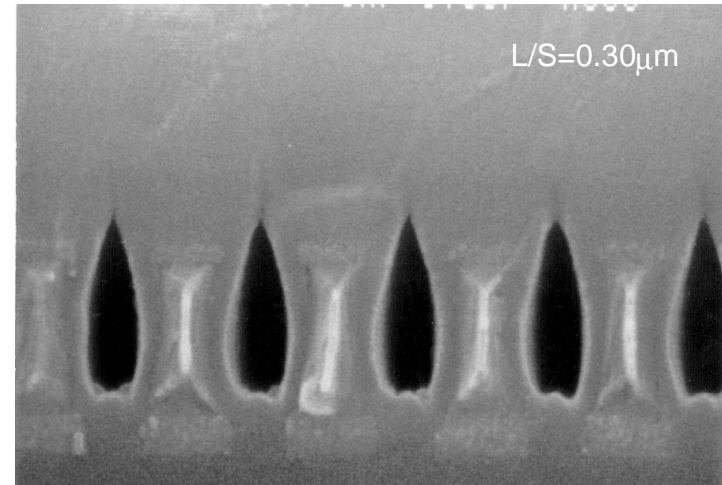
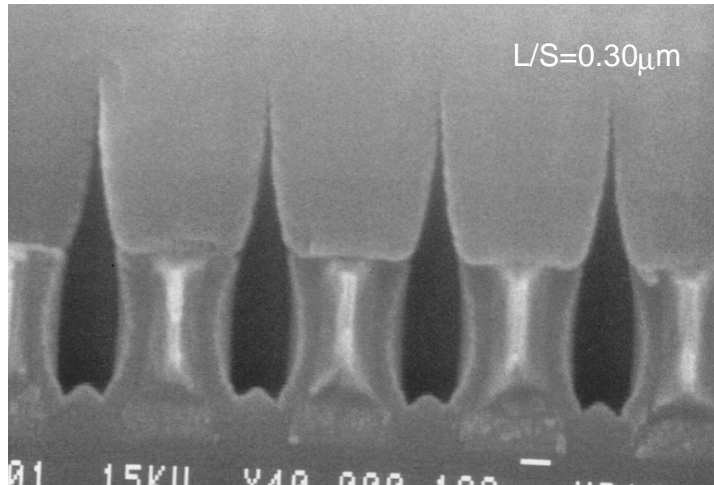
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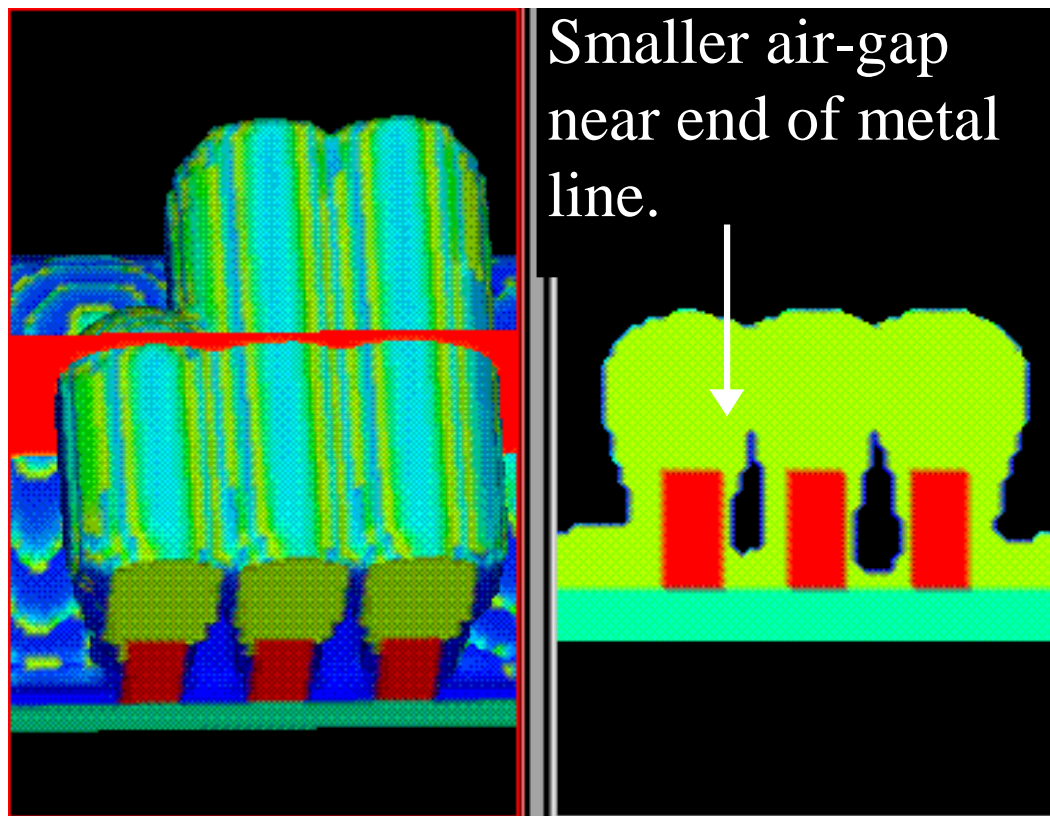
Control of Air-Gap Size and Shape



- Air-gap size and extension above metal lines can be controlled by varying deposition conditions.
- Samples shown held up to CMP



Layout Dependence of Air-Gaps

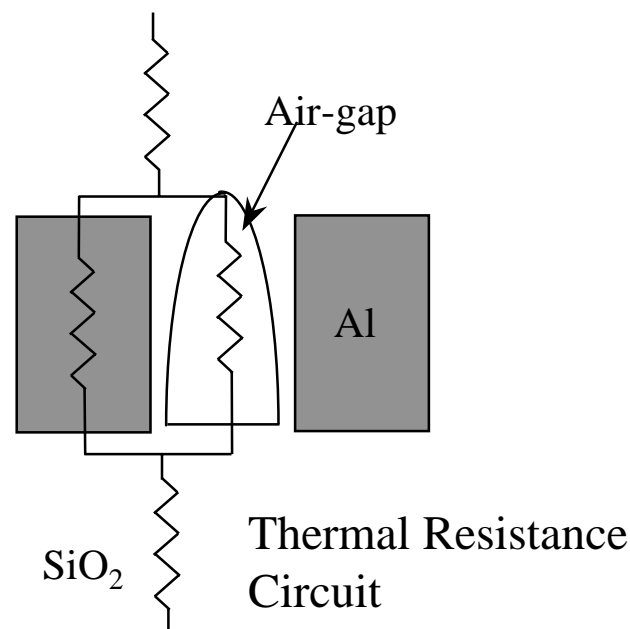


- Additional deposition flux at end of metal lines results in smaller air-gaps which may help via reliability.



Simulated Joule Heating and Thermal Reliability

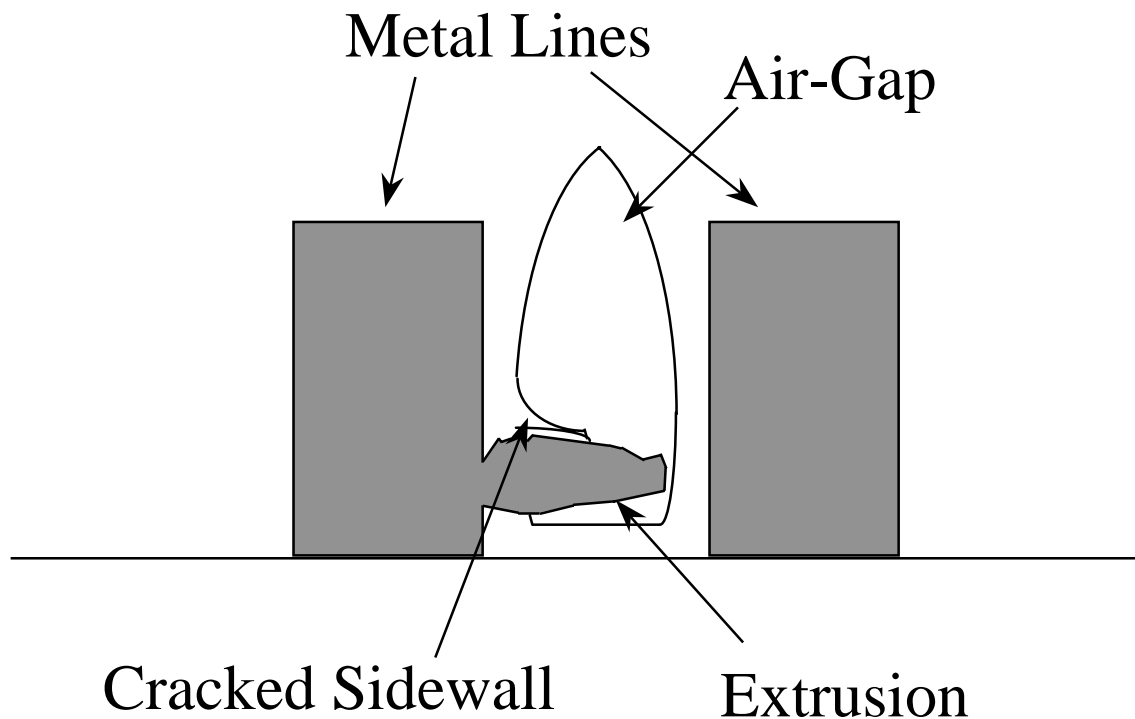
Material	ΔT above $T_{\text{substrate}}$
Homogeneous SiO_2	4.9 K
Homogeneous low-K	76.7 K
Air-gaps w/ SiO_2 ILD	5.2 K



- Heat conduction to substrate limited by interlevel dielectric
- Interconnects with air-gaps show comparable thermal performance to conventional SiO_2 .



Electromigration Reliability



- Thin SiO_2 sidewall may lead to shorter electromigration lifetimes.

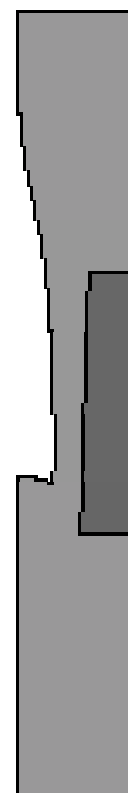
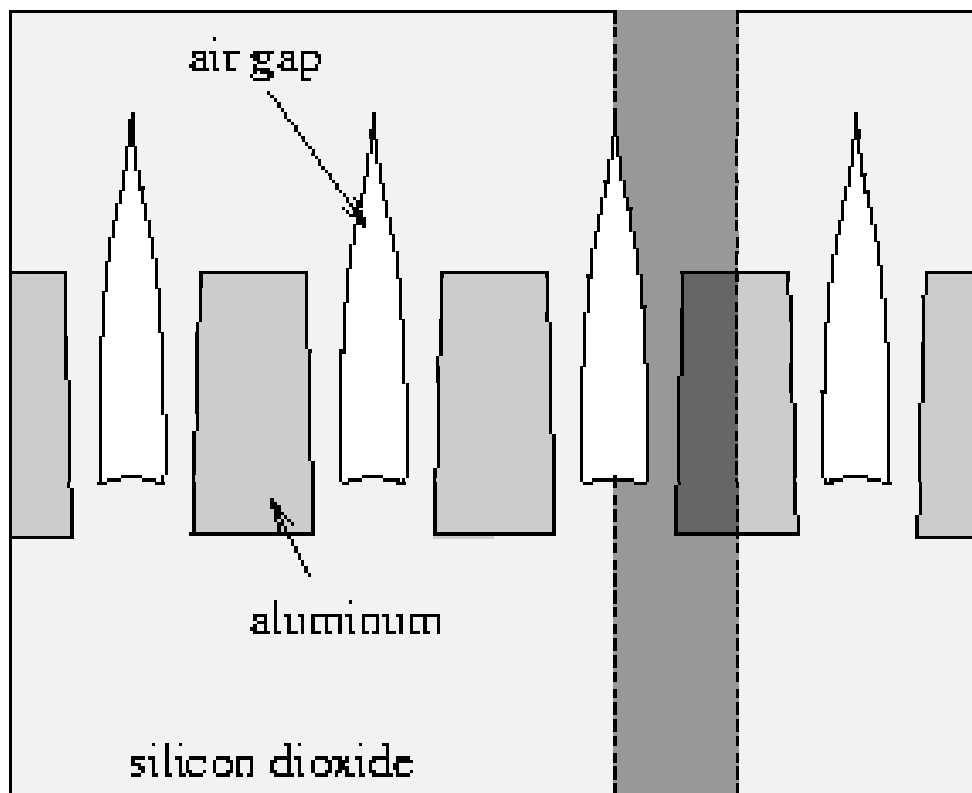


Simulation Methodology to Assess Electromigration Reliability

- 1) Assume fracture stress for dielectric material
- 2) Solve for stress distributions in interconnect geometry as function of loading
- 3) Calculate hydrostatic stress in the metal which occurs simultaneously with dielectric failure
- 4) Use hydrostatic stress to determine MTTF using MIT reliability models by Thompson, et al.



Import SPEEDIE Air-gap Profile to MARC for Electromigration Induced Stress Analysis

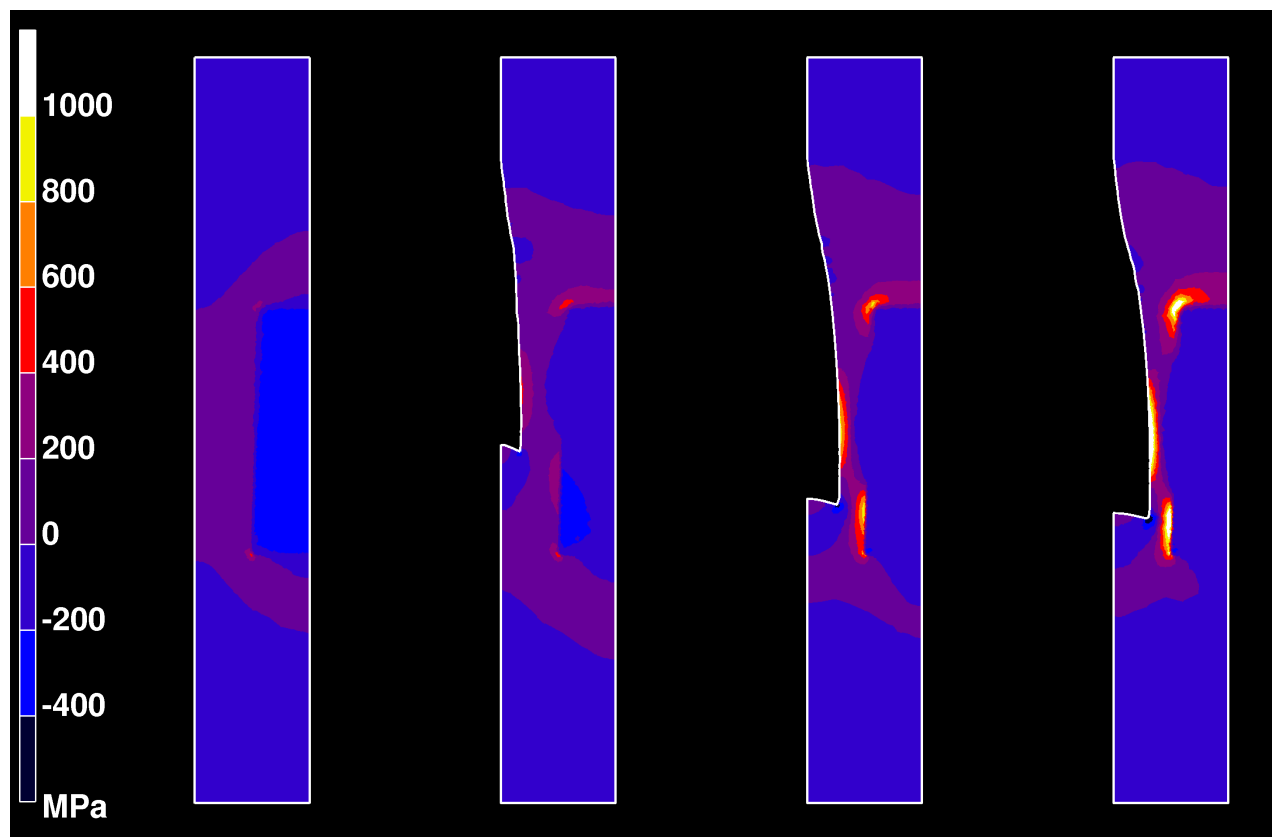


constants used:
Aluminum
 $E = 70 \text{ GPa}$
 $\nu = 0.34$
 $\sigma_{\text{yield}} = 200 \text{ MPa}$

Silicon Dioxide
 $E = 83 \text{ GPa}$
 $\nu = 0.20$



Contour Plots of Maximum Principal Stress

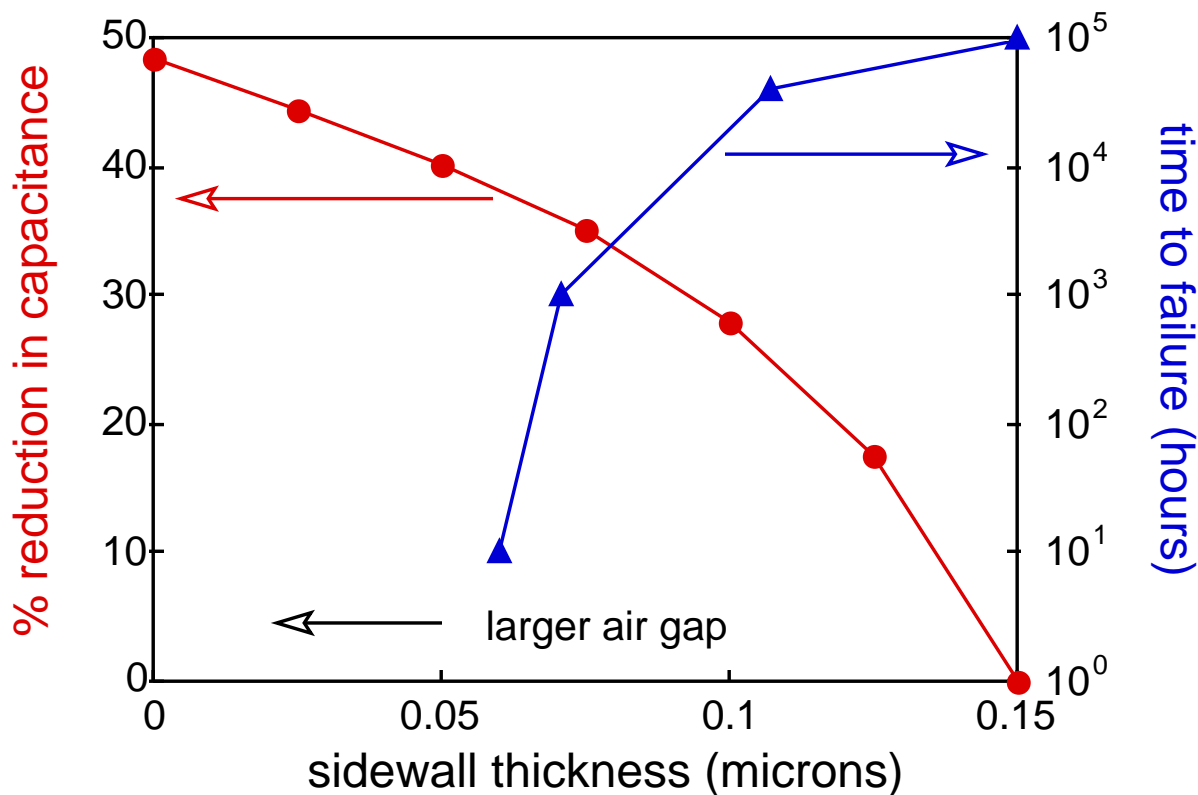


- All structures are shown with the same average hydrostatic stress in the Al (300 MPa)



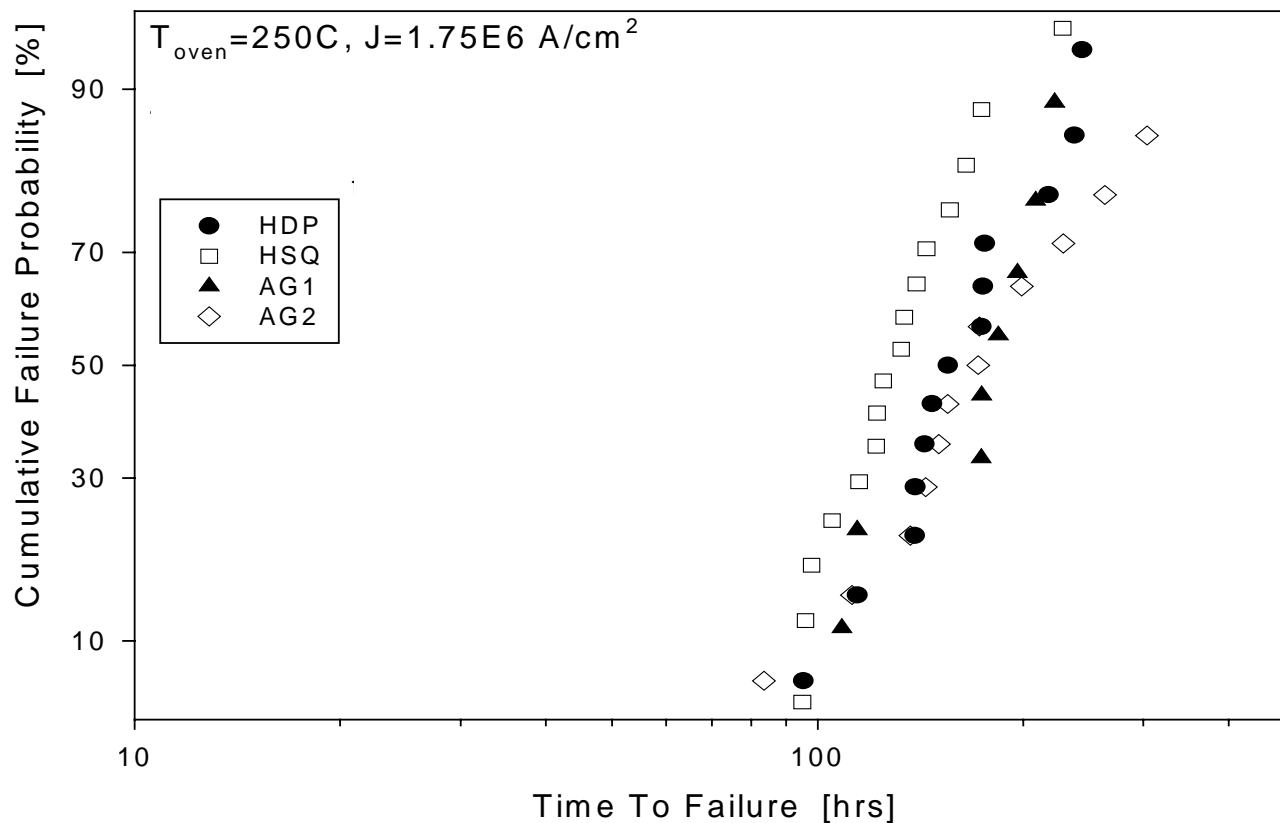
Simulated Reliability/Performance Tradeoff

Time to Failure and Percent Reduction in Capacitance vs. Sidewall Thickness





Preliminary Electromigration Data





Summary and Conclusions

- Developed methodology for assessing tradeoffs between reliability and performance for IC interconnects.
- Capacitance reduction using air-gaps comparable to most low-K materials under investigation.
- Air-gap size and shape can be controlled to address CMP and via reliability issues.
- Thermal performance of air-gaps comparable to homogeneous SiO_2 .
- Preliminary electromigration data show no difference between air-gaps and homogeneous SiO_2 .



Future Work

- Further integration and reliability studies
- Integration of Air-Gaps with Dual Damascene Copper.
- Extension of air as dielectric to “Air-Bridges”.



Acknowledgements

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