Alternative Gate Dielectrics for Scaled CMOS Devices

ERC Review
August 3, 2000

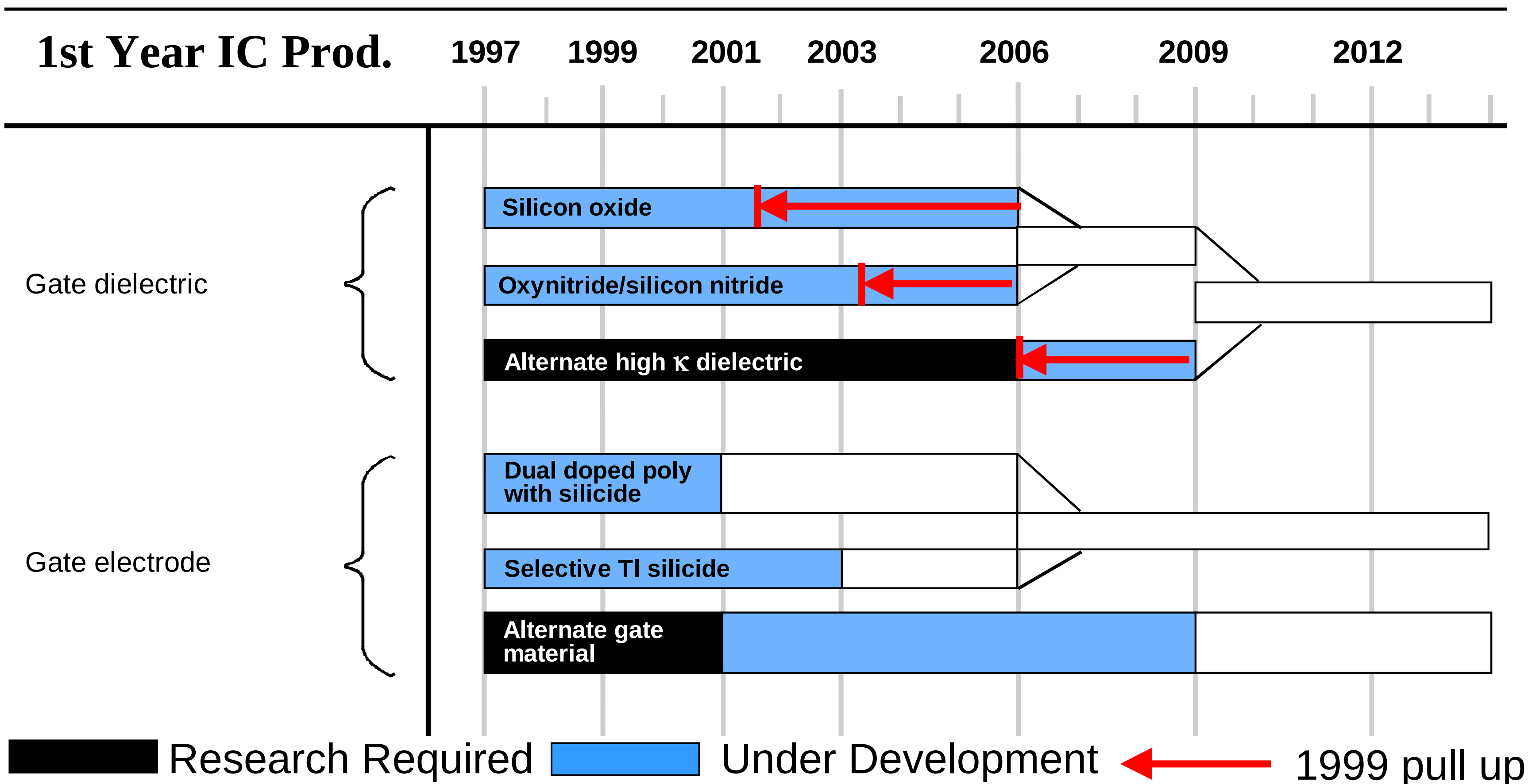
Glen Wilk
Bell Labs, Lucent Technologies

Beyond SiO_2: High-κ Dielectrics

Outline

- **Gate Oxide Scaling - Need to replace SiO_2**
- **Electrical Requirements to replace SiO_2 (High-κ)**
- **Alternate Gate Dielectric Candidates**
- **Future Issues**

IRTS 1997/1999 Roadmap



Semiconductor Industry Association 1997 Roadmap

1999: T_{ox} scaling more aggressive

Table 22 Thermal/Thin Films Gate Etch and Doping Technology Requirements

Year of First Product Shipment Technology Generation	*1997 250 nm*	*1999 180 nm*	*2001 150 nm*	*2003 130 nm*	*2006 100 nm*	*2009 70 nm*	*2012 50 nm*
Equivalent oxide thickness T_{ox}(nm)	**4–5**	**3–4**	**2–3**	**2–3**	**1.5–2**	**< 1.5**	**< 1.0**
Thickness control (% 3σ)	± **4**	± **4**	± **4**	± **4–6**	± **4–8**	± **4–8**	± **4–8**
Sidewall spacer thickness (nm)	**100–200**	**72–144**	**60–120**	**52–104**	**20–40**	**7.5–15**	**5–10**

Why is Gate Oxide Thinning Needed?

Higher speed/functionality ⇒ higher device density ⇒ smaller devices

For transistors: Want High Drive Current $I_D \sim C_{ox}(V_G - V_{th})^2$

Where: $C_{ox} = (\varepsilon_{ox}A) / t_{ox}$ $\varepsilon = 3.9$ for SiO_2 (dielectric constant)

⇒ Maximize C_{ox}: decrease t_{ox} or increase ε

Decrease t_{ox} ⇒ gate oxide thinning

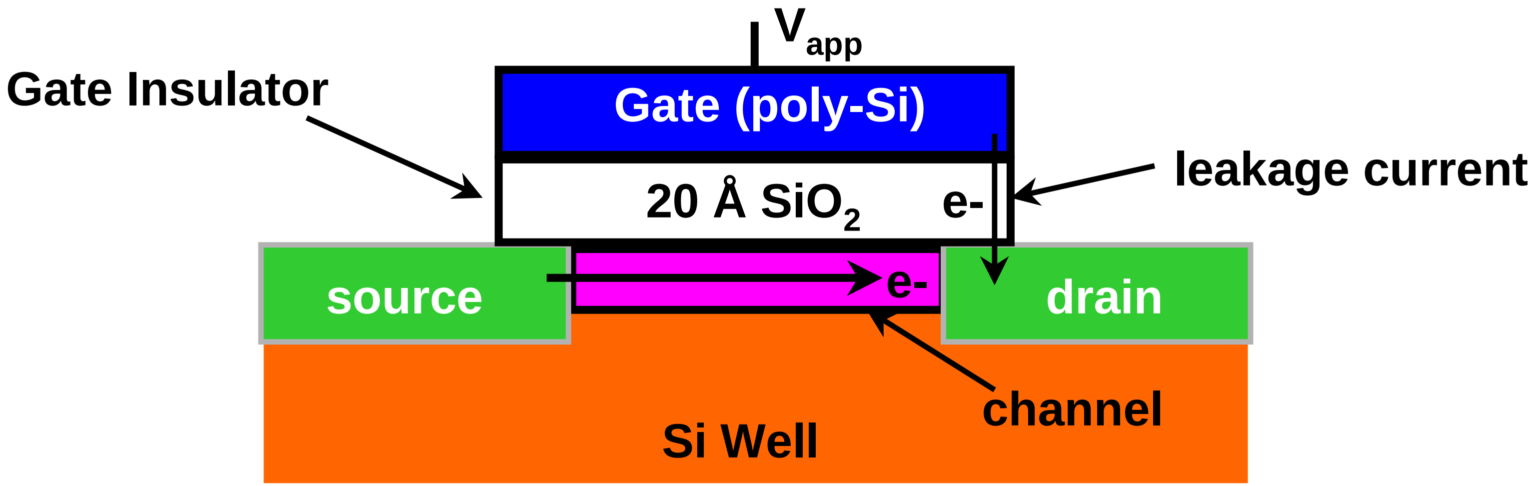
For $t_{ox} < 20$ Å

⇒ High leakage (low battery lifetime)

⇒ Boron Penetration

- **Increase ε_{ox} ⇒ replace SiO_2 with new material**
- ***Or new device design***

MOSFET Scaling Gate Dielectric Issues



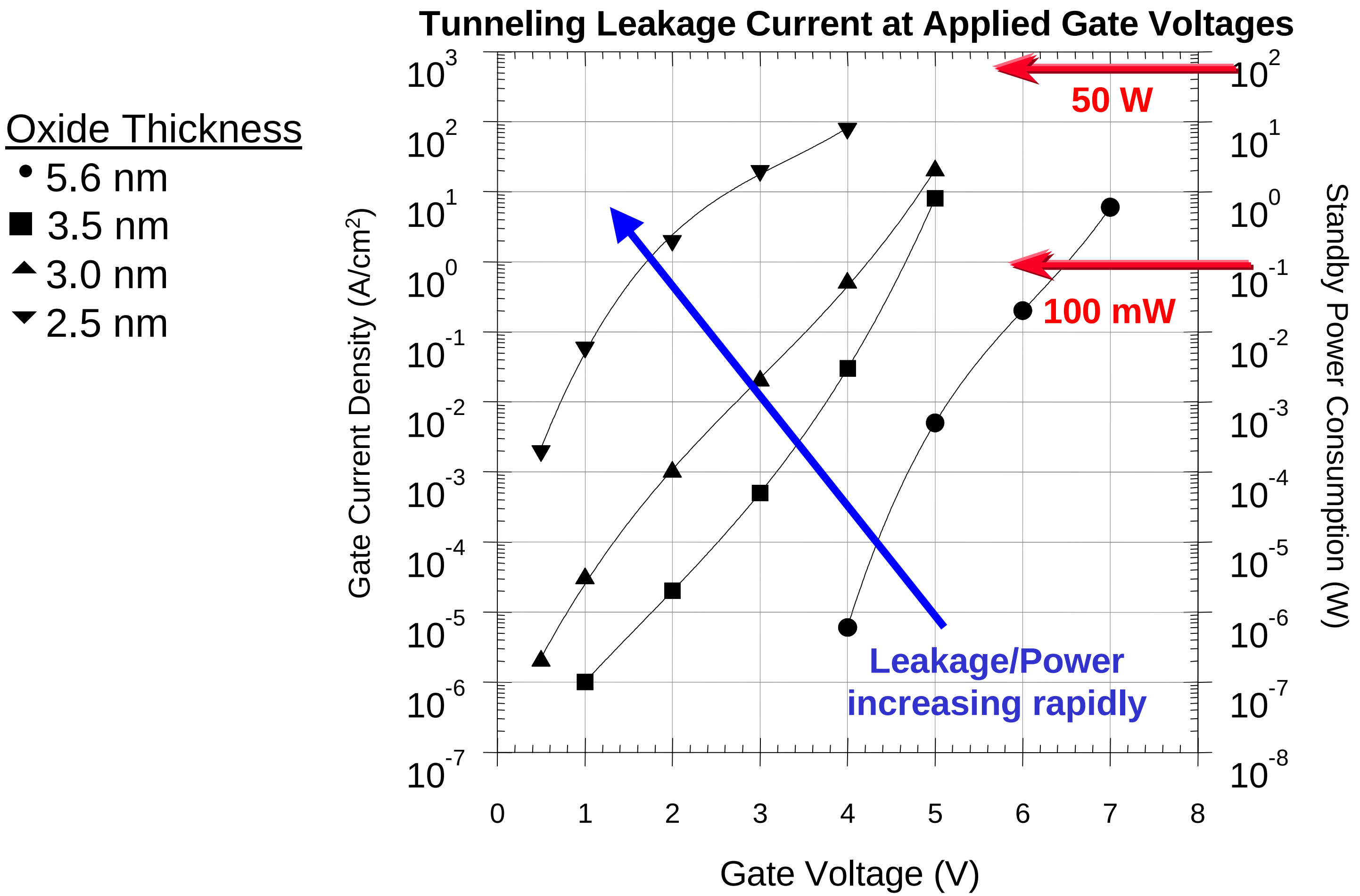
Problem : **Difficult to scale SiO_2 below 14 Å with current manuf.**

Solution: **Replace SiO_2 with high-κ dielectric to continue scaling**

Caution: **SiO_2 used as gate dielectric for 40 years - not simple!**

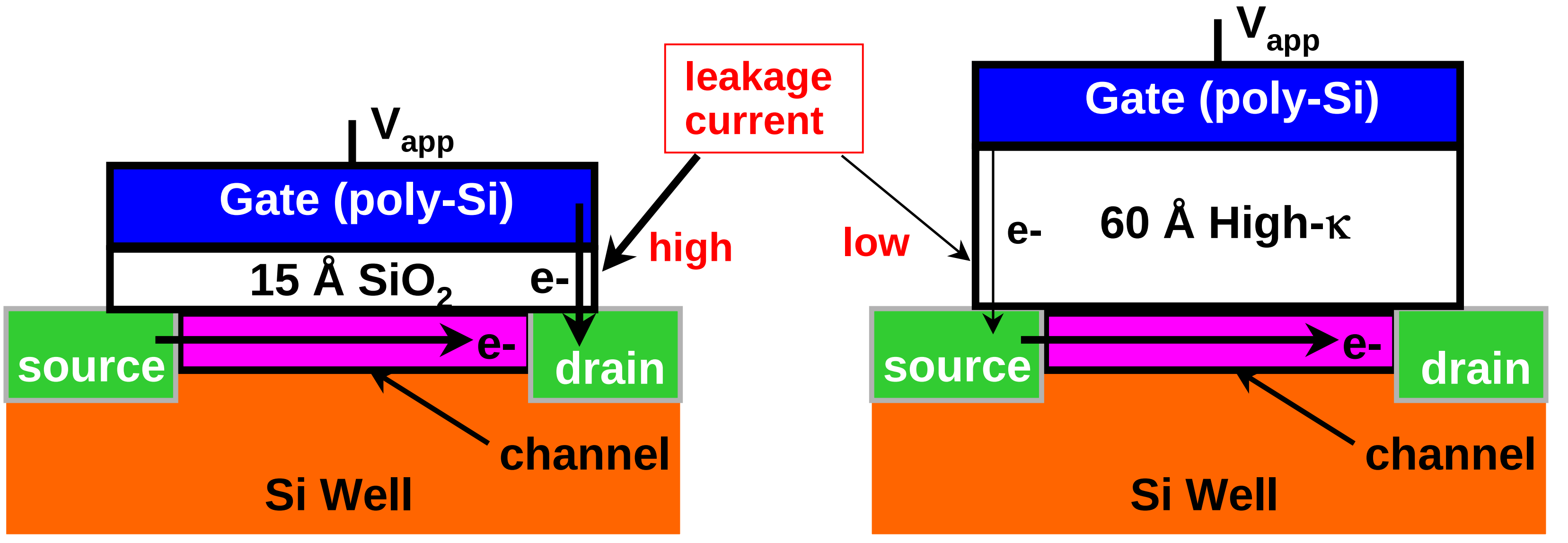
Gate Oxide Thinning: Leakage Current

Assumes 0.1 cm² (or less) total gate area



Lucent Technologies
Bell Labs Innovations

High-κ Leakage Reduction



High-κ film ⇒ thicker gate dielectric ⇒ lower leakage w/ same performance

How to decide which High-κ material is best?

Desirable High-κ Gate Dielectric Properties

Physical Properties

- $\varepsilon \sim 15 - 60$
- Band Offset $\Delta E_c \geq 1.5$ eV
- Thermally stable next to Si
- Remain amorphous on Si
- Block Boron Diffusion

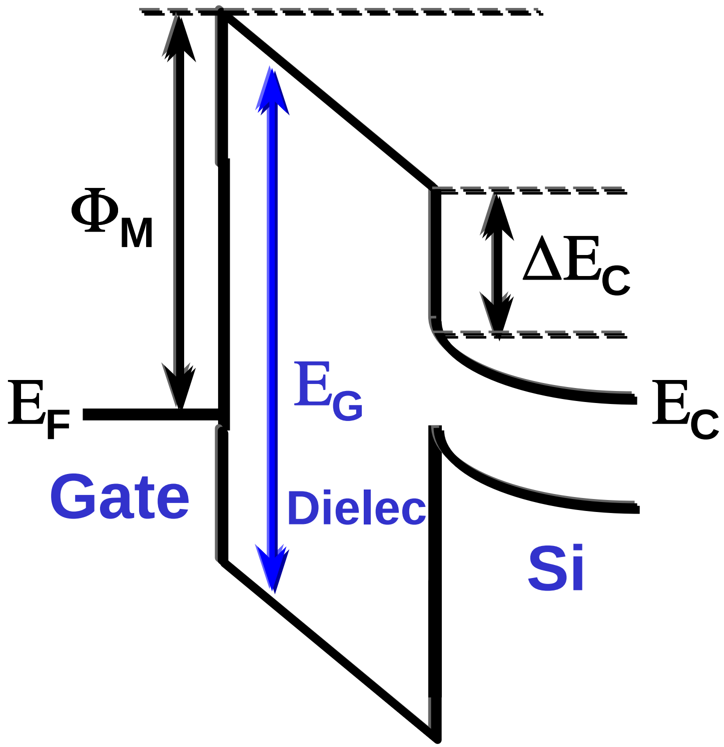
Electrical Properties

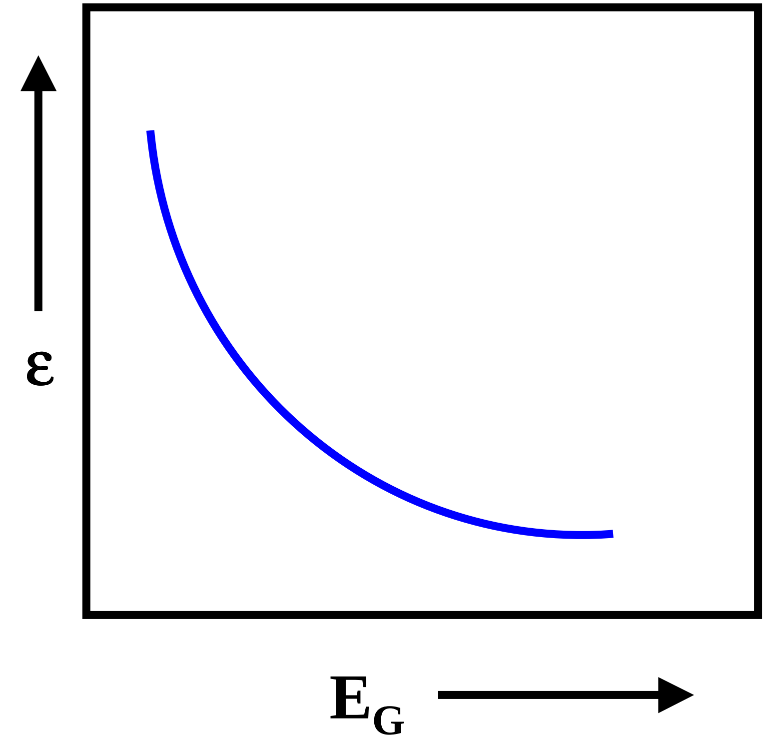
- $t_{ox} < 10$ Å
- $J < 10^{-3}$ A/cm^2 @ V_{DD}
- Minimal dispersion & hysteresis
- High uniformity across wafer
- Reliability as good as SiO_2

t_{ox}: electrically equivalent SiO_2 thickness

Leakage Current: ε vs. E_G (and ΔE_C)

Tunneling through Dielectrics





- **Leakage current ~ exp ($-\Delta E_C$)**
- **Want high E_G, tradeoff with ε**

Gate Dielectric Properties

Material	Dielectric Constant (ε)	Band Gap E_g (eV)	ΔE_c (eV) to Si	ΔH_F (eV/O atom)	Crystal Structure(s)
SiO_2	3.9	8.9	3.2	-4.68	amorphous
Si_3N_4	7	5.1	2	-----	amorphous
Al_2O_3	9	8.7	2.8*	-5.76	amorphous
Y_2O_3	15	5.6	2.3*	-4.93	cubic
CeO_2	26	5.5	(a)	-5.02	cubic
Ta_2O_5	26	4.5	1 - 1.5	-2.09	orthorhombic
La_2O_3	30	4.0	2.3*	-6.17	hexagonal, cubic
TiO_2	80	3.5	1.1	-4.86	tetrag. (rutile, anatase)*
HfO_2	25	5.7	1.4*	-5.77	mono., tetrag., cubic*
ZrO_2	25	7.8	1.5*	-5.66	mono., tetrag., cubic*
$HfSi_xO_y$	15 - 25	~6	1.5*	-5.24	amorphous
$ZrSi_xO_y$	15 - 25	~6	1.5*	-5.21	amorphous

* J. Robertson Fall MRS 1999

- Si_3N_4, Al and Y-oxides - ε too low
- ZrO_2, HfO_2, La_2O_3 good candidates

Gate Dielectric Properties

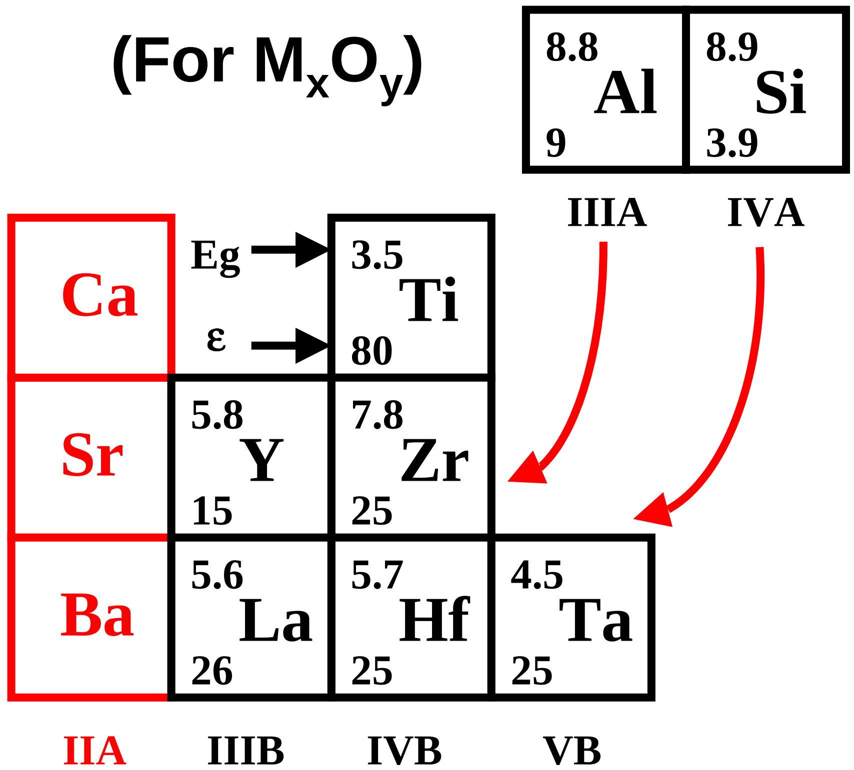
Material	Dielectric Constant (ε)	Band Gap E_g (eV)	ΔE_c (eV) to Si	ΔH_F (eV/O atom)	Crystal Structure(s)
SiO_2	3.9	8.9	3.2	-4.68	amorphous
Si_3N_4	7	5.1	2	-----	amorphous
Al_2O_3	9	8.7	2.8*	-5.76	amorphous
Y_2O_3	15	5.6	2.3*	-4.93	cubic
CeO_2	26	5.5	(a)	-5.02	cubic
Ta_2O_5	26	4.5	1 - 1.5	-2.09	orthorhombic
La_2O_3	30	4.0	2.3*	-6.17	hexagonal, cubic
TiO_2	80	3.5	1.1	-4.86	tetrag. (rutile, anatase)*
HfO_2	25	5.7	1.4*	-5.77	mono., tetrag., cubic*
ZrO_2	25	7.8	1.5*	-5.66	mono., tetrag., cubic*
$HfSi_xO_y$	15 - 25	~6	1.5*	-5.24	amorphous
$ZrSi_xO_y$	15 - 25	~6	1.5*	-5.21	amorphous

- **Combine desirable properties from SiO_2 and Al_2O_3 with MO_2, M_2O_3 and M_2O_5 (M = Zr, Hf, Y, La, Ta)**
- **High-κ M-Si-O and M-Al-O stable & amorphous on Si**

High-κ Cation Candidates

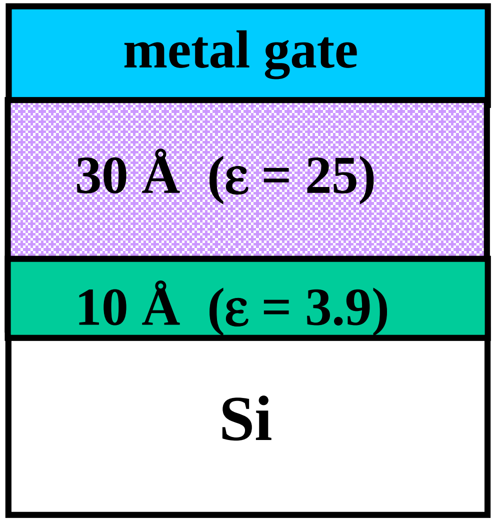
(For M_xO_y)

For $BaSrTiO_3$
single crystal films
by MBE only



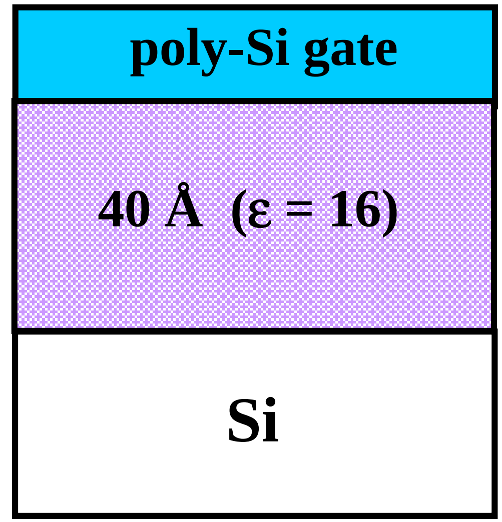
- Cations most likely to replace SiO_2 gate dielectric
- Combinations of Al or Si with transition metal also possible

High-κ Stack vs. Single Layer



(1)

$t_{ox} = 15$ Å



(2)

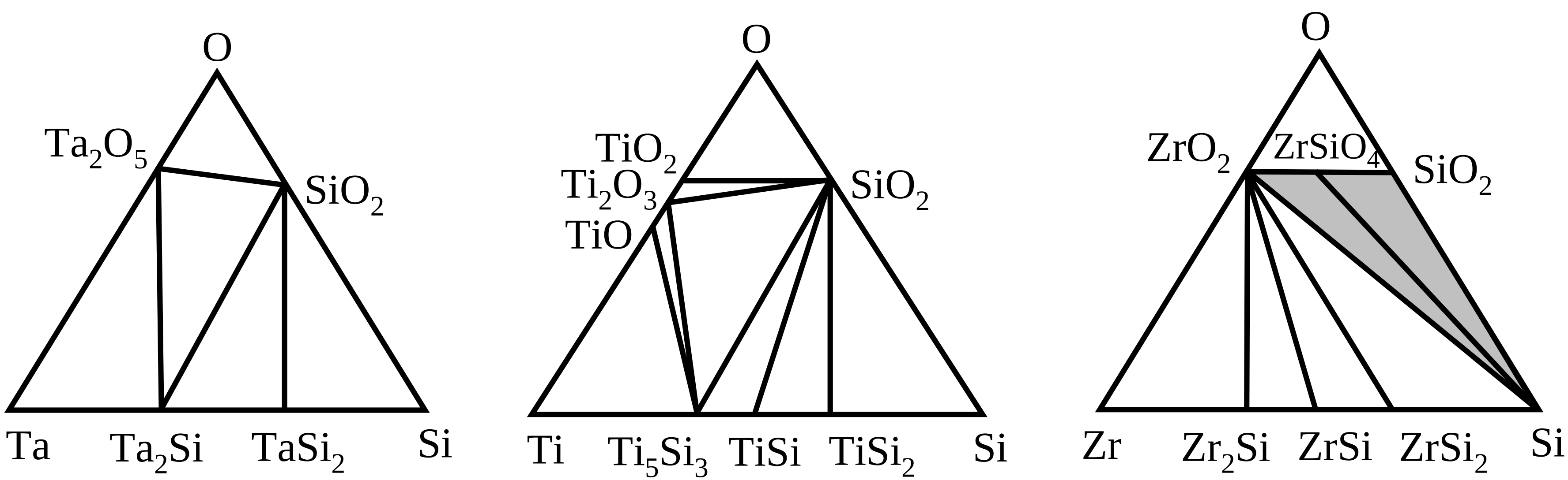
$t_{ox} = 10$ Å

$t_{phys}(1,2) = 40$ Å, assume same leakage

(2) also retains poly-Si compatibility

Stability of Silicates (700 - 900ºC)

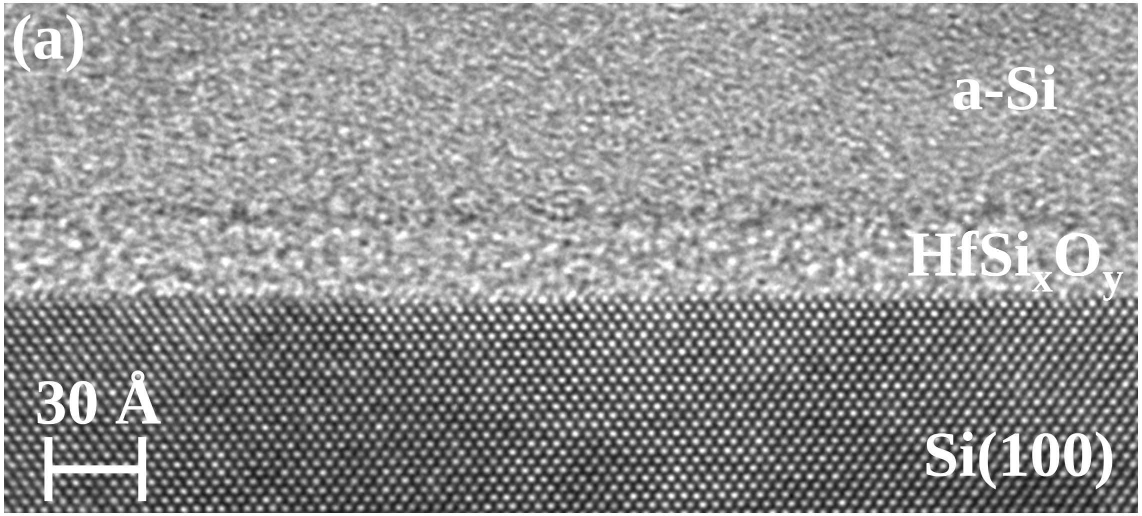
After Beyers, J. Appl. Phys. **56**, 147 (1984)
and Wang and Mayer, J. Appl. Phys. **64**, 4711 (1988)



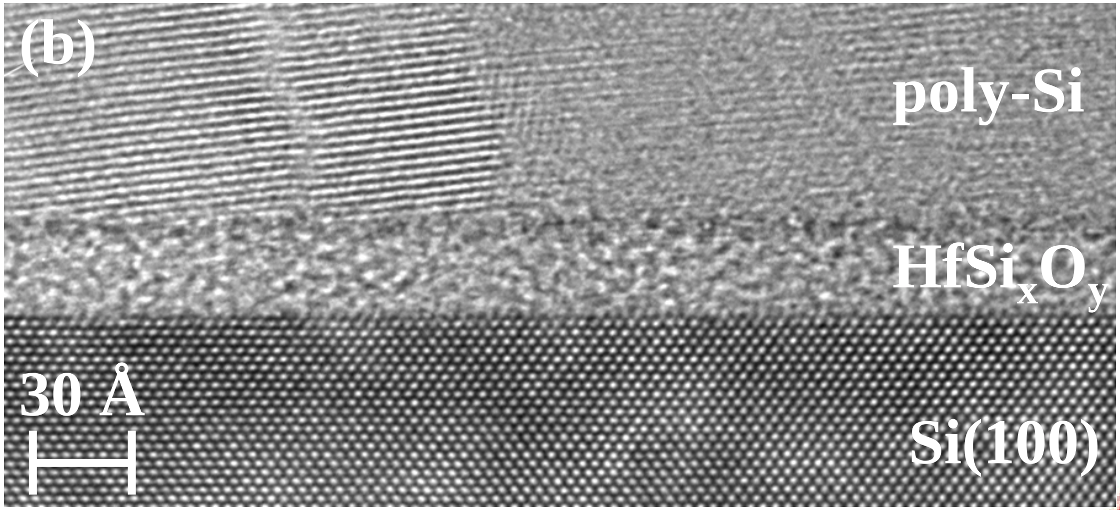
- **ZrO_2/Zr-Si-O stable on Si; Ta and Ti oxide/silicate not stable**
- **Zr, Hf Silicates: no interfacial layer required**

Stability of Silicates on Si: Si cap

As-Deposited top Si at 25C



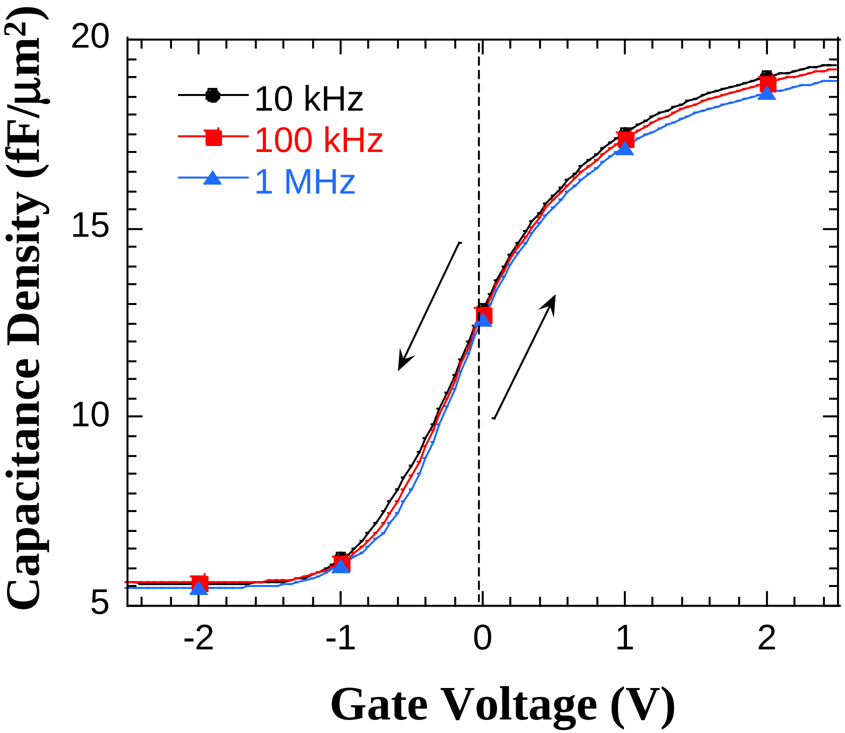
After Anneal N_2/1050C/20 sec

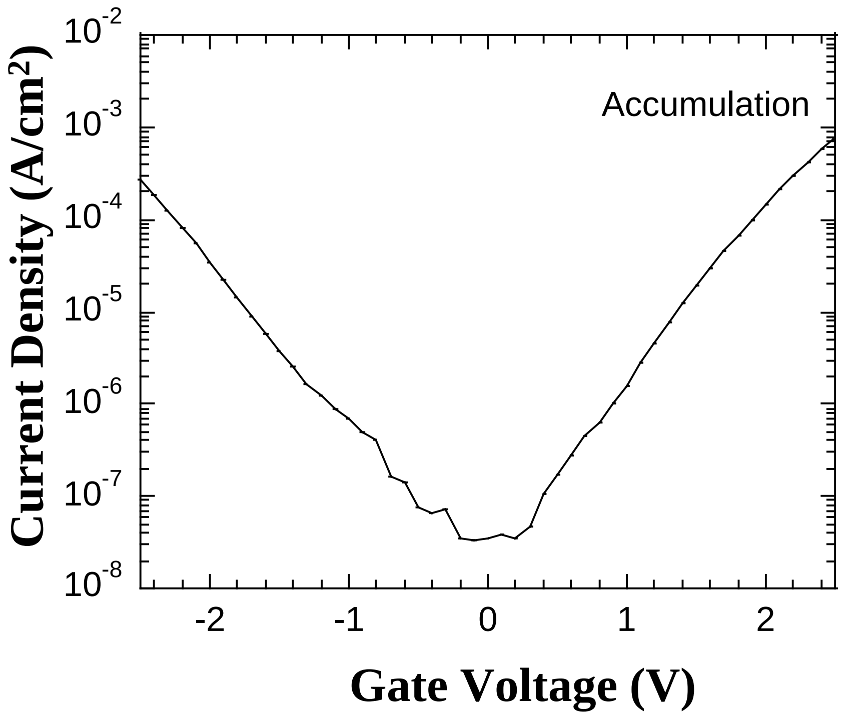


Lucent Technologies
Bell Labs Innovations

Silicate Electrical Properties

Au/50 Å $(HfO_2)(SiO_2)_5$ /n^+ Si





t_{ox} = 17.9 Å (ε ~ 11) **J (@1V) = 1.5 x 10^{-6} A/cm^2**

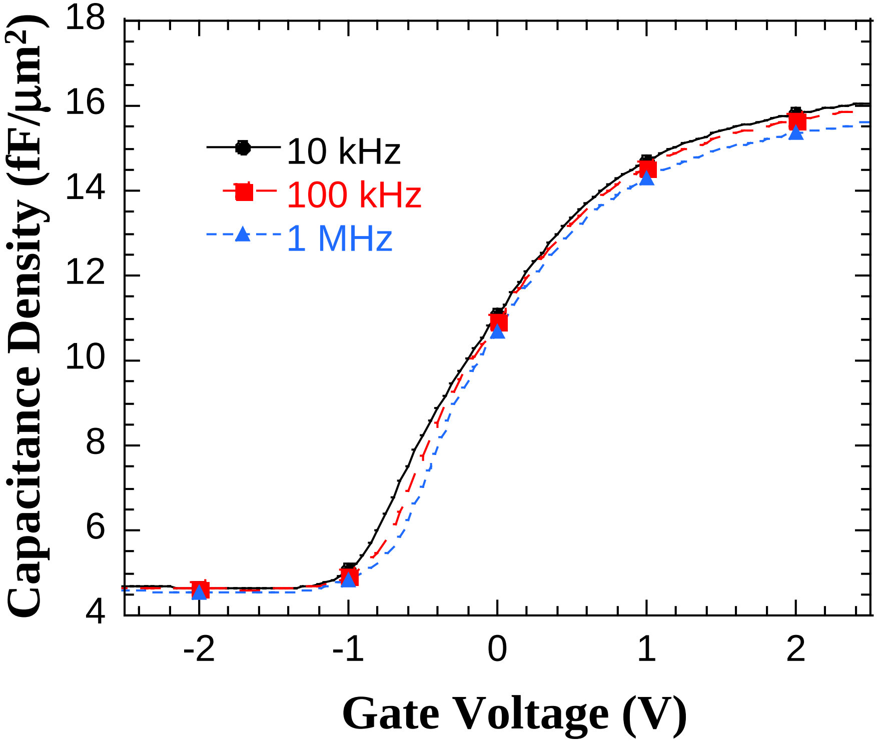
Hysteresis < 10 mV for silicates

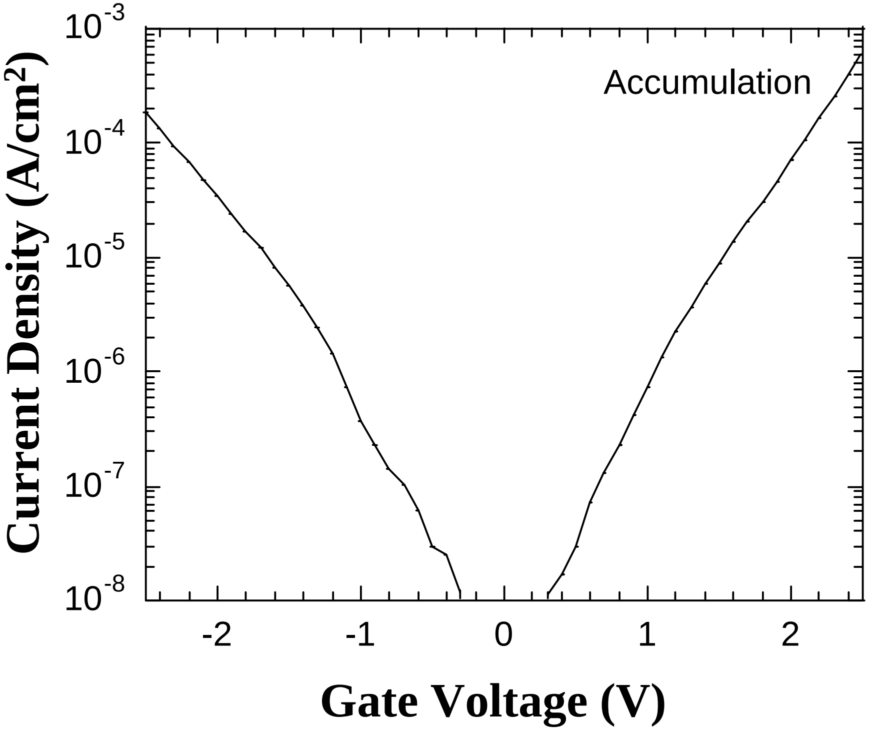
Wilk and Wallace, APL **74**, 2854 (1999)

Lucent Technologies
Bell Labs Innovations

Silicate Capacitor Properties

Au / 50 Å $(ZrO_2)(SiO_2)_7$ / n^+ Si



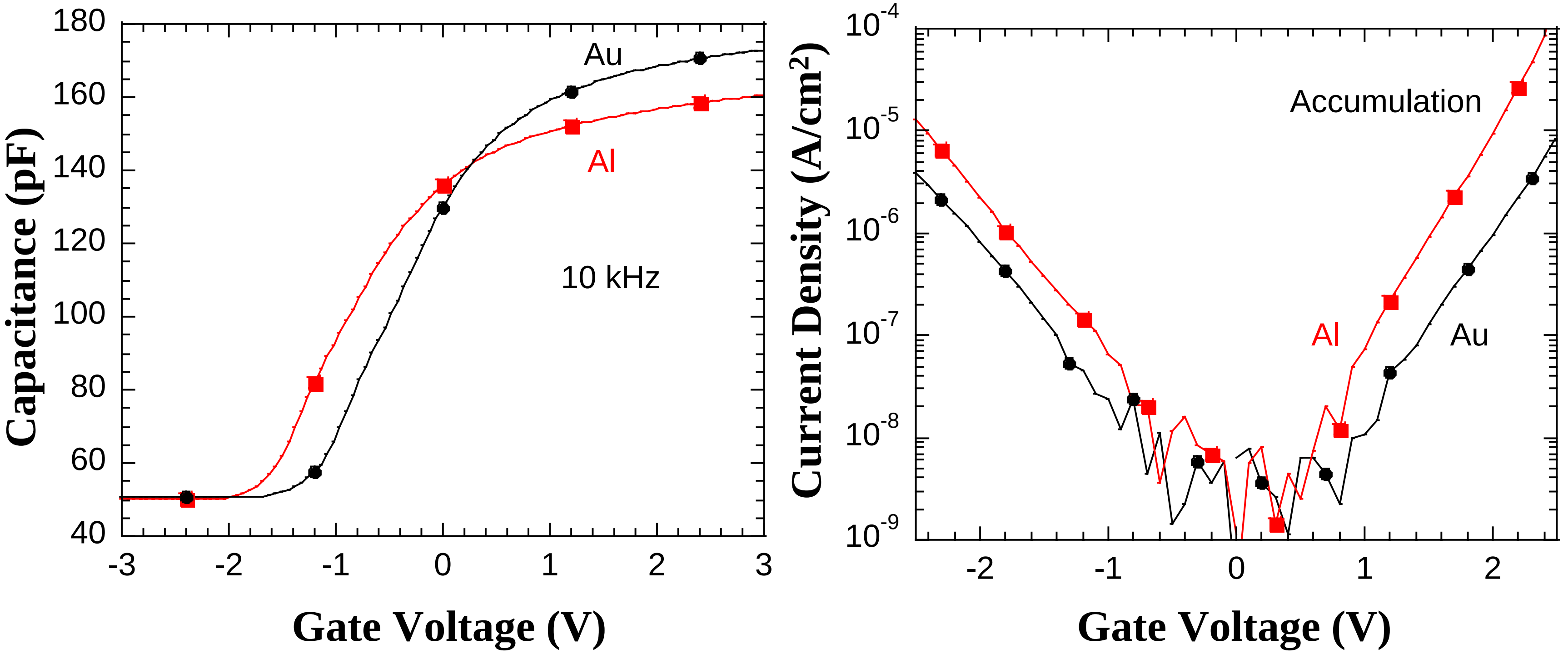


t_{ox} = 20.8 Å (ε = 9.4)

J (@1V) < 1 x 10^{-6} A/cm²

Lucent Technologies
Bell Labs Innovations

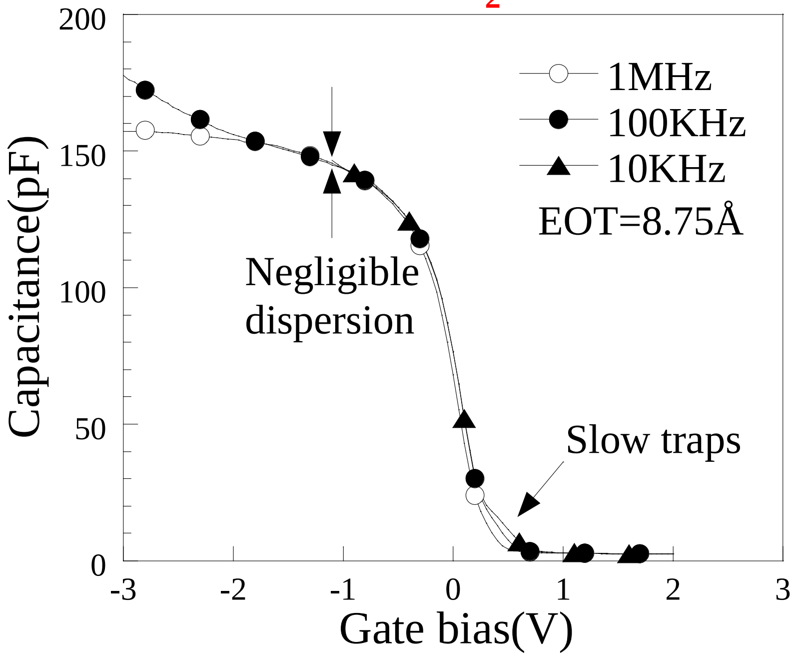
Effect of Electrodes



- **Au electrodes provide lower leakage in both polarities**

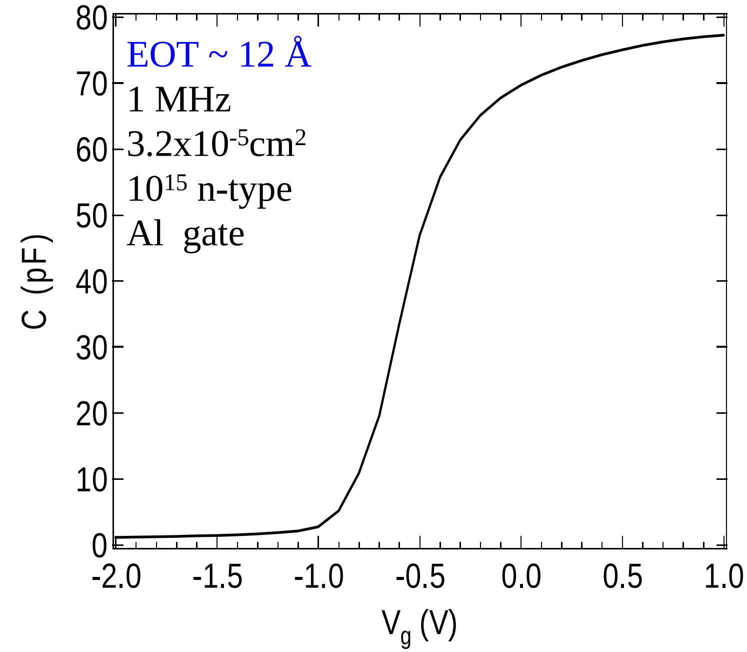
Capacitor Properties of HfO_2 and Y Silicate

HfO_2



Frequency dispersion of HfO_2 at –1V <1%/decade.

Y-Si-O



40Å Y-Si-O film formed by sputter/oxidation of Y on Si(100)

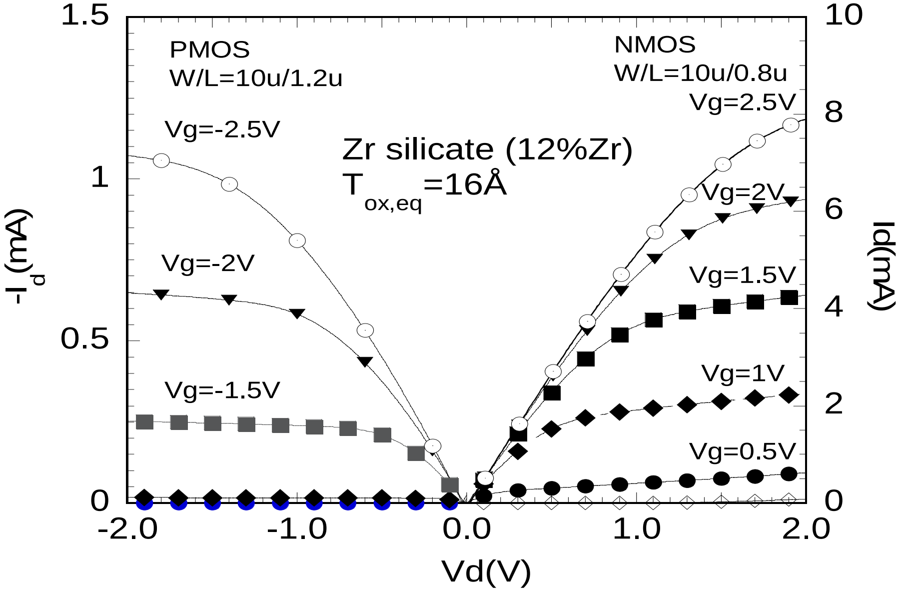
t_{ox} < 10 Å demonstrated with Zr silicate; t_{ox} = 12 Å with Y silicate

W.J. Qi *et al*., VLSI Tech. Dig., p. 40 (2000)

Parsons *et al*, High-κ Workshop New Orleans, p. 30 (2000)

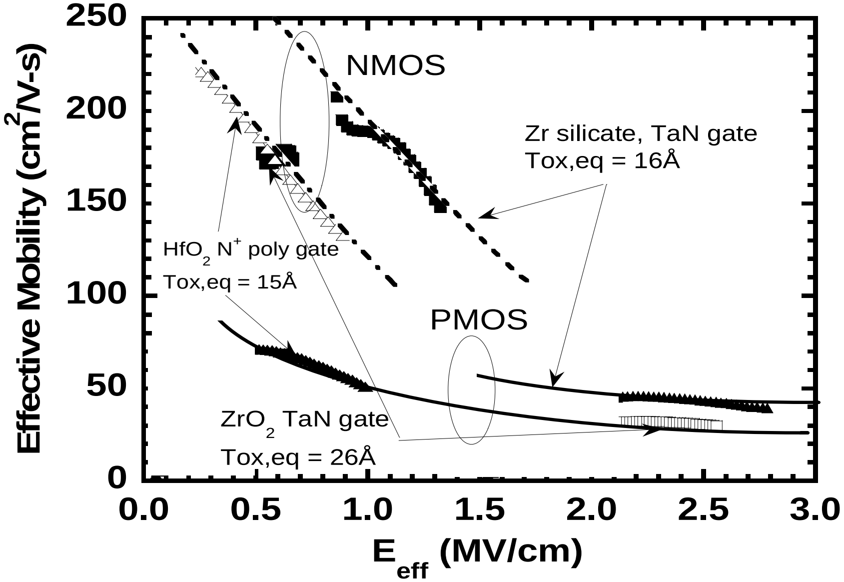
Transistor Properties with Zr Silicate

Zr-Si-O



Id-Vd characteristics of PMOS and NMOS transistors with Zr silicate

Zr-Si-O

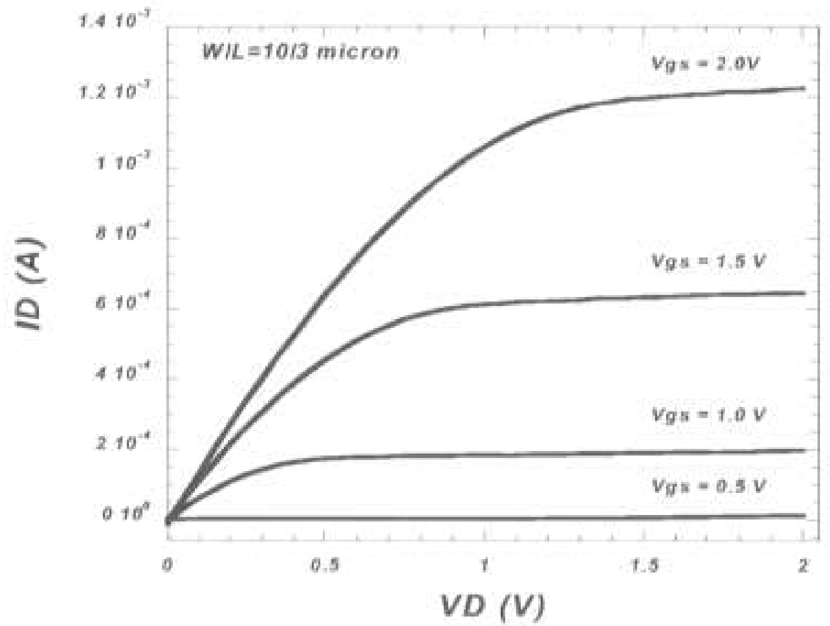


Effective mobility comparison of ZrO_2 and silicate with TaN gate electrode, HfO_2 with n^+poly electrode.

W.J. Qi *et al.*, VLSI Tech. Dig., p. 40 (2000)

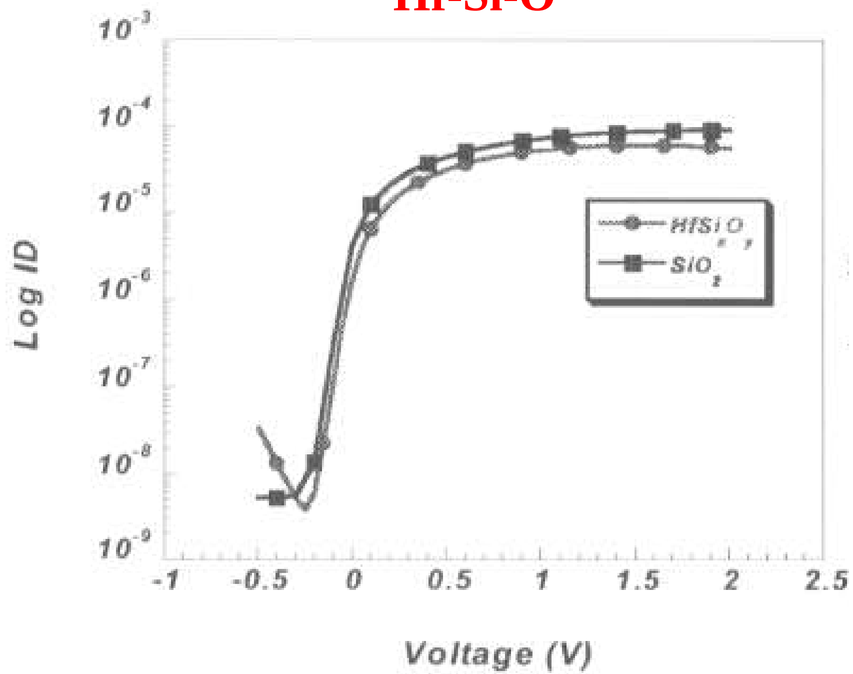
Transistor Properties with Hf Silicate

Hf-Si-O



Id-Vd characteristics of NMOSFET with Hf silicate

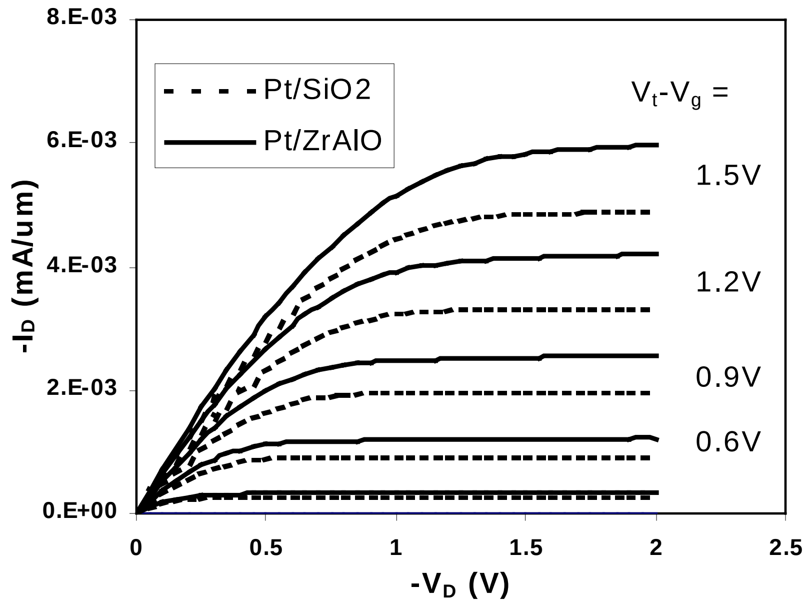
Hf-Si-O



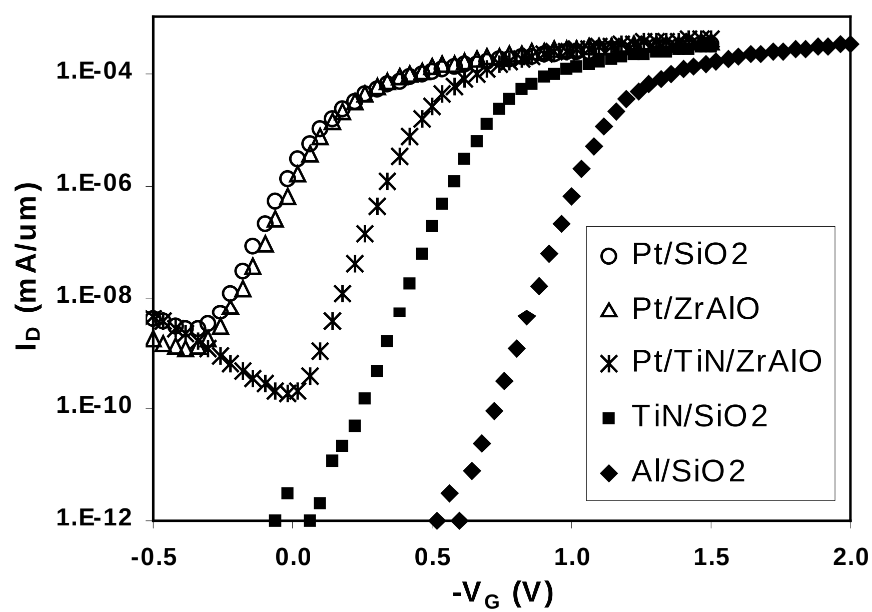
Log Id-Vg of NMOSFET with Hf silicate vs. SiO_2

Misra *et al*, High-κ Workshop, New Orleans, p. 36 (2000)

Transistor Properties with Zr Aluminate



Drain characteristics of 10 x 10 μm pMOSFET with Pt gate and Zr-Al-O and SiO2 dielectrics



Subthreshold (Vd = -0.1 V) of pMOSFET with Al, Pt and TiN gates on Zr-Al-O and SiO_2 dielectrics. Transistor size 10 x 10 μm

Ma *et al*, High-κ Workshop, New Orleans, p. 12 (2000)

Lucent Technologies
Bell Labs Innovations

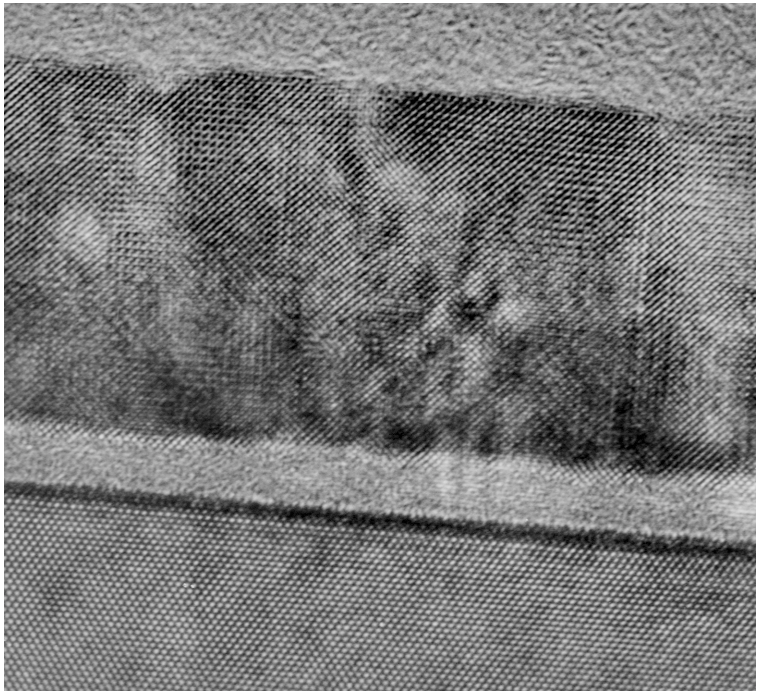
Epitaxial High-κ on Si

150 Å $SrTiO_3$/3 ML BaSrO/Si

$SrTiO_3$

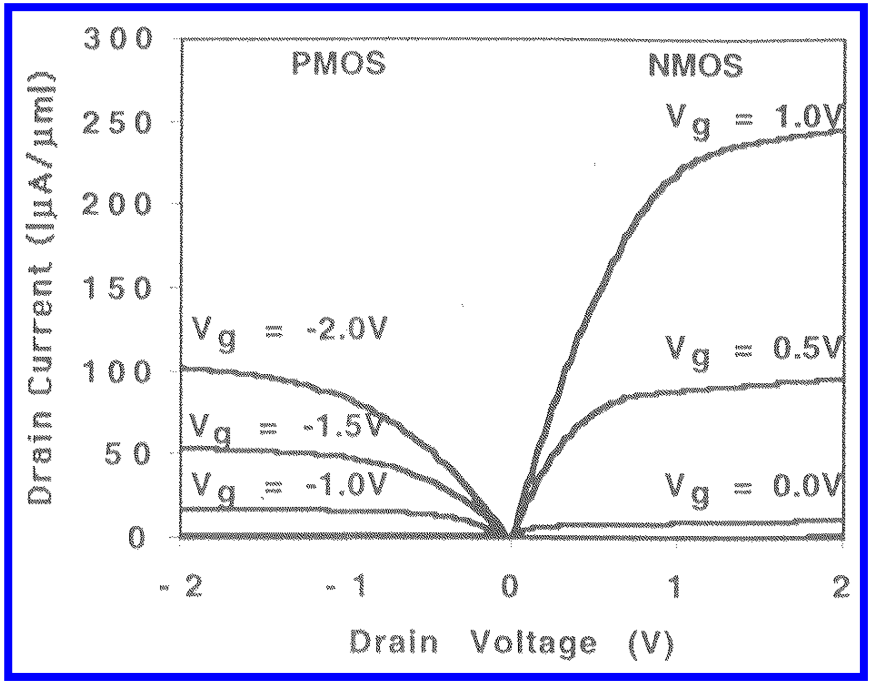
BaSrO

Si(100)



Single crystal growth on Si(100)

TaN/110 Å STO/3 ML BSO/Si

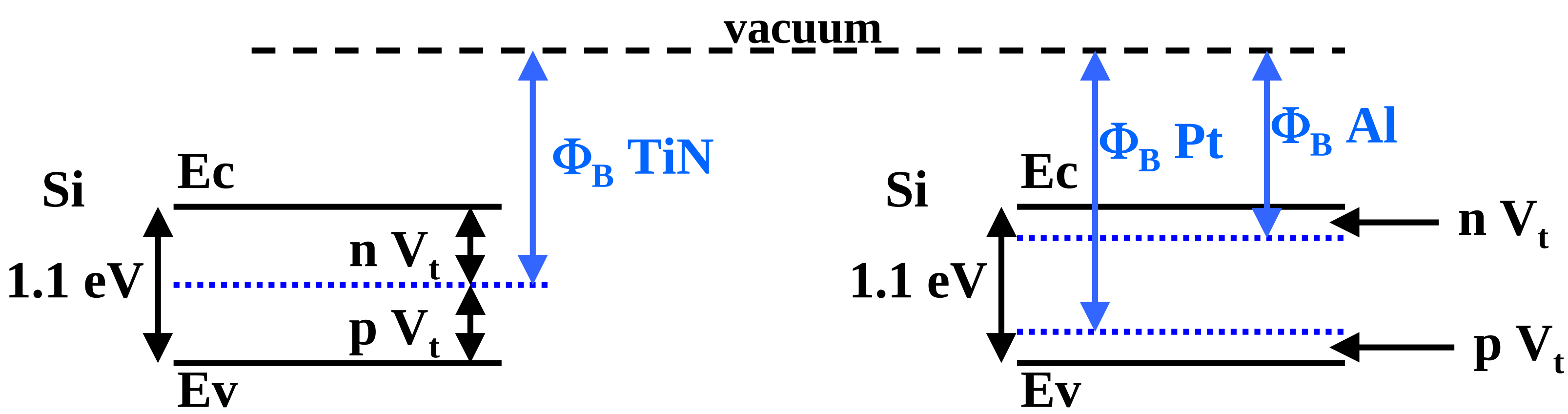


I_d-V_d for 2x10 μm nMOS & pMOS
t_{ox} < 10 Å - good transistor props.

McKee *et al*. Phys. Rev. Lett. **81**, 3014 (1998)
Eisenbeiser et al., APL **76**, 1324 (2000)

Metal Gate Issues

Single Midgap Metal — **Dual Metals**



- **Metal gates desirable: eliminate poly depletion and B diffusion**

- **Midgap metals have threshold voltage V_t ~ 0.5 eV - too high**
- **Need dual metals to achieve low V_t - which metals?**
- **Ta or TaN suitable for nMOS; RuO_2 or Pt suitable for pMOS**

- ***MAY* need metals of Ta, Ru or Pt for gate electrodes**

Key Issues for High-κ Gate Dielectrics

- **Interface control**
- **Require t_{ox} < 15 Å, will need t_{ox} < 10 Å**
- **Require $J < 10^{-3}$ A/cm^2 @ V_{DD}**
- **Thermal Stability**
- **Gate Electrode Choice? Need Compatible materials**

Summary

- **SiO_2 running out of time - need high-κ replacement in 5 years**
- **Metal oxides and alloys most likely candidates**
- **Cations Zr, Hf, Ti, Y, La and Ta most likely in dielectric (Motorola and Oak Ridge pursuing Ba, Sr, Ca, Ti materials)**
- **Metal gates *may* be used, and *may* contain Ta, Pt or Ru**
- **Jury is still out on ALL above materials until more actual devices have been fabricated, tested and optimized**