Electrical and Material Properties of ALCVD ZrO_2 Gate Dielectrics

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Presentation Contents

- Desired Properties of Scaled Gate Dielectric
- Atomic Layer Deposition (ALCVD)
- Electrical Properties
- Material Properties
- Annealing Studies
- Summary/Tech Transfer
- Future Work
- Acknowledgements

Desirable Advanced Gate Dielectric Properties for Sub-0.1 μm MOSFET

Physical Properties

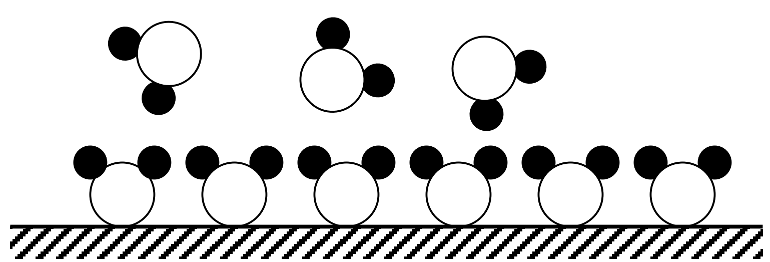
- K ~ 15 - 60
- Thermally stable next to Si (no barrier layer; annealing)
- High-quality interface with Si

Electrical Properties

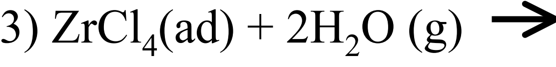
- EOT < 15 Å
- $J < 10^{-3}$ A/cm^2 @ V_{DD}
- $D_{it} < 5 \times 10^{10}$ cm^{-2} eV^{-1}
- V_{FB}, hysteresis < 50 mV (for $+V_{DD}$ to $-V_{DD}$ sweep)
- No C-V dispersion

ALCVD Reaction Cycle

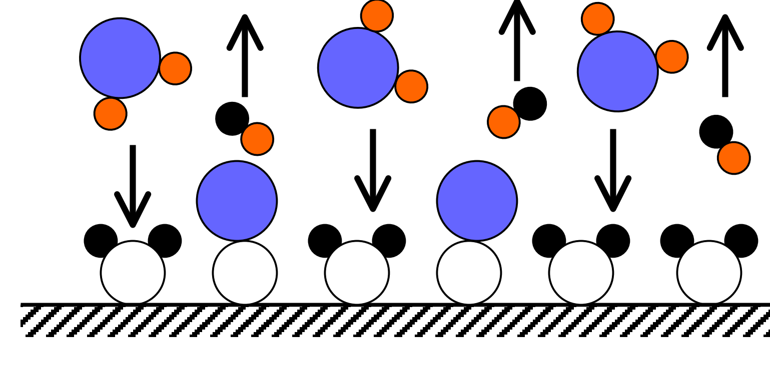
1) $ZrCl_4(g)$



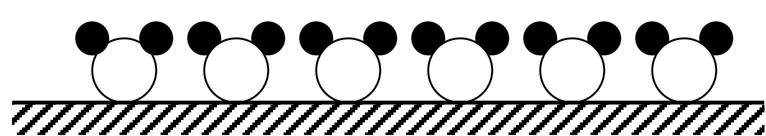
3) $ZrCl_4(ad) + 2H_2O\ (g) \rightarrow$



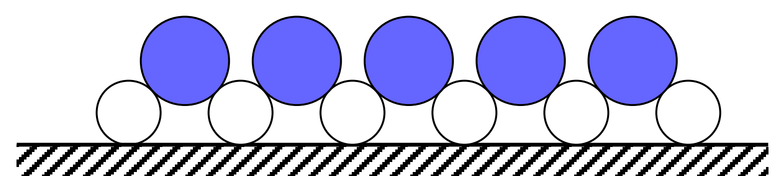
$ZrO_2\ (ad) + 4HCl\ (g)$



2) $ZrCl_4(ad)$



4) $ZrO_2(ad)$

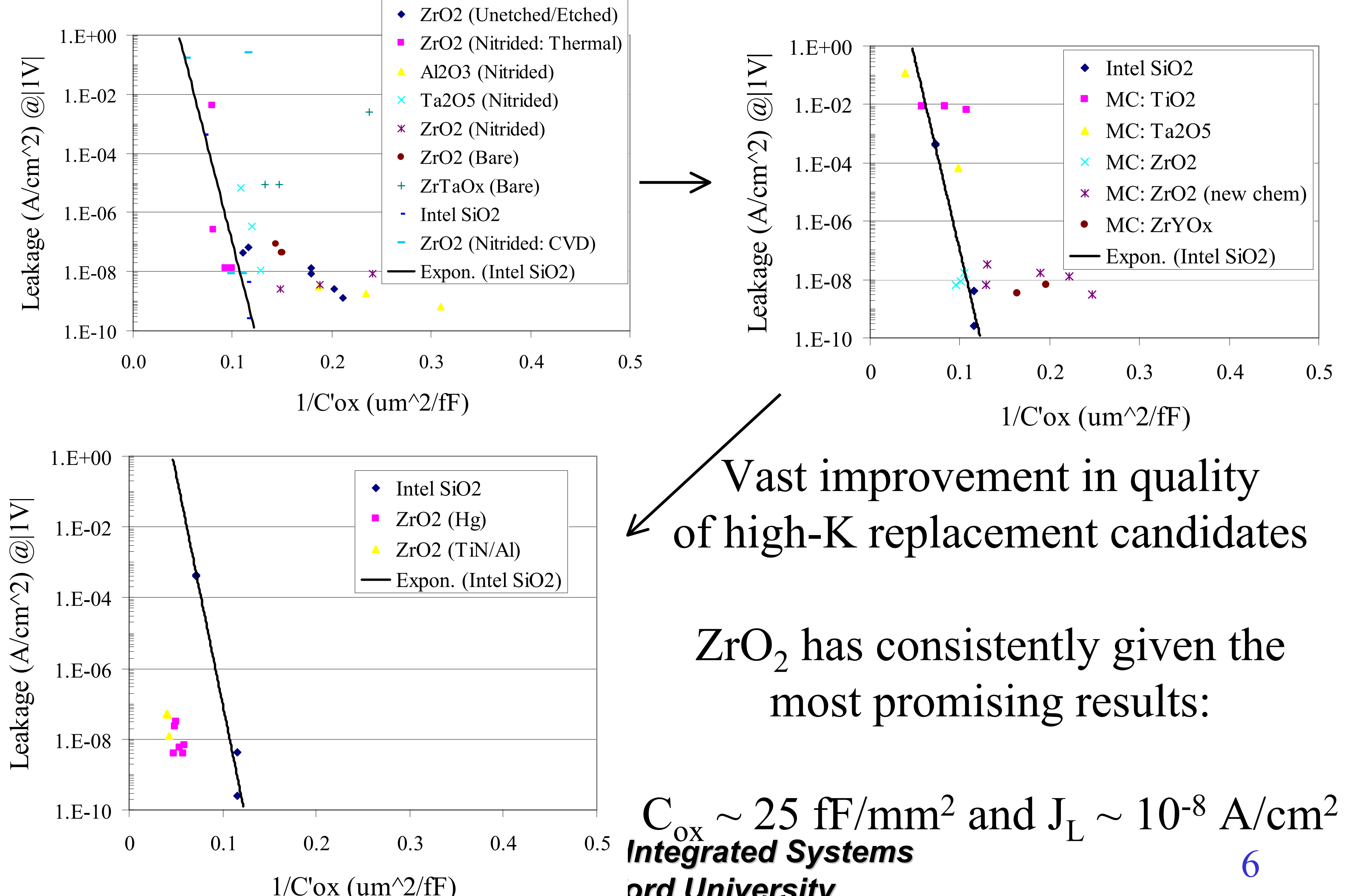


- Self-limiting surface reaction steps with purge in between steps

Characteristics Features of ALCVD

Characteristic Feature	*Inherent Implication on Film Deposition*	*Practical Advantage*
Self-limiting growth	Thickness only dependent on number of deposition cycles	Accurate and simple thickness control
	No need for reactant flux homogeneity	Large area capability Large batch capability Excellent conformality Good reproducibility
Separate dosing of reactants	No gas phase reactions	Favors precursors highly reactive towards each other, enabling effective material utilization
	Sufficient time is provided to complete each reaction step	High quality materials are obtained at low processing temperatures

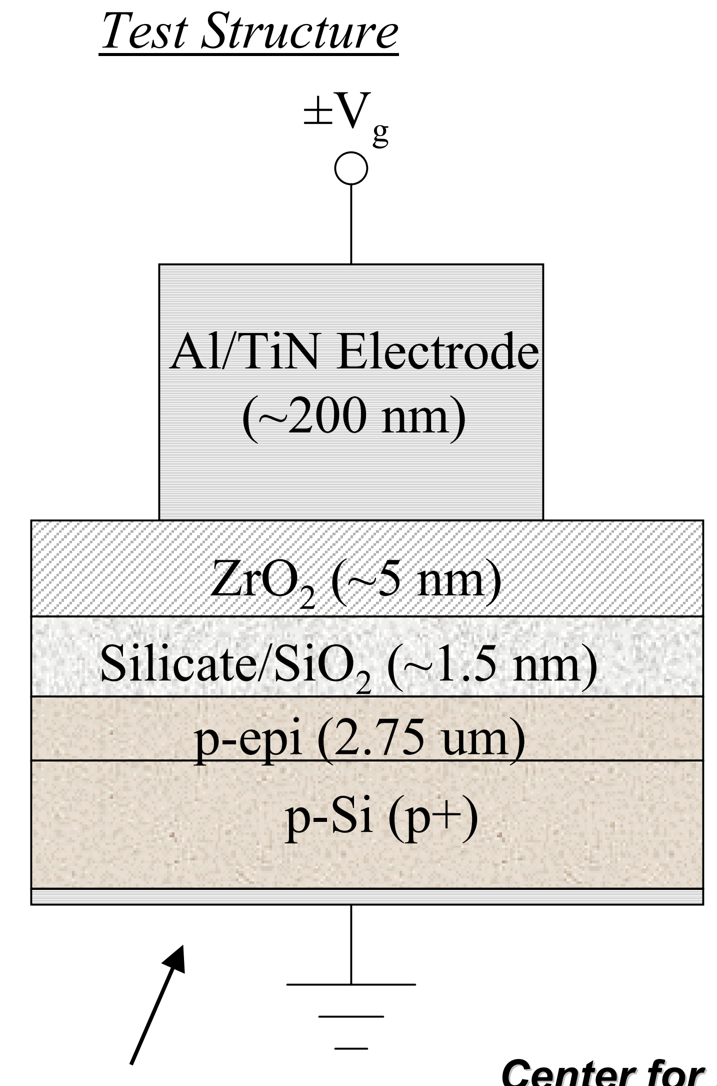
Improvement of High-K Candidates



Electrical Measurements

Gate Structure / Measurement Setup

Test Structure



Dielectric Deposition

ALD by ASM Microchemistry

Precursors : $ZrCl_4$, H_2O

Temperature : 300 °C

Test Conditions

C-V : HP 4284A

I-V : HP 4140B

Test temperature : 25 °C

Voltage step : 0.05 V

Delay Time : 1 sec

Cap Area = 7.225×10^{-5} cm^2

Substrate Material

Minimize series resistance

p-epi ($N_A \sim 1 \times 10^{16}$ cm^{-3})

p-sub ($N_A \sim 1 \times 10^{19}$ cm^{-3})

700 °C NH_3 RTN

Leakage vs. EOT Comparison Between SiO_2 and ZrO_2 Dielectrics

Leakage (A/cm^2) @ |1V|

10^{3} 10^{1} 10^{-1} 10^{-3} 10^{-5} 10^{-7} 10^{-9}

12 14 16 18 20 22 24 26

Equivalent Oxide Thickness (A)

SiO2
RS ZrO2
ALD ZrO2

- At the same EOT, ALD ZrO_2 films show lower leakage current than conventional SiO_2 and RS ZrO_2 films
- RS ZrO_2 data from: Lee, J.C. etal, *IEDM* 1999, to be published

J-V and C-V Characteristics of 13.8 Å EOT ZrO_2 Dielectric

Capacitance (fF/um^2)

f = 1 MHz

Gate Bias (V)

Leakage (A/cm^2)

Gate Bias (V)

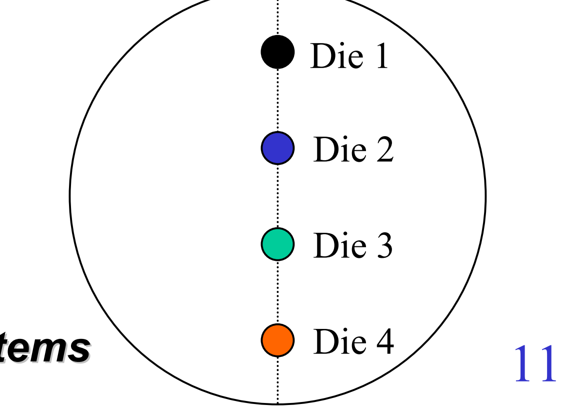
- EOT was calculated from the accumulation capacitance of HFCV (1 MHz) curves without accounting for quantum mechanical effects
- The thinnest EOT obtained thus far is 13.8 Å (physical thickness ~ 50 Å) with a leakage of less than 10^{-7} A/cm^2 at -1 V

Film Uniformity

Capacitance (fF/um²) vs. Gate Bias (V), f = 1 MHz — Die 1, Die 2, Die 3, Die 4

Leakage (A/cm²) vs. Gate Bias (V) — Die 1, Die 2, Die 3, Die 4

•Exceptional uniformity across entire 8 inch wafer resulting in consistent and repeatable electrical characteristics



Frequency Dispersion

Capacitance (fF/um^2)

30
25
20
15
10
5
0

-3 -2.5 -2 -1.5 -1 -0.5 0 0.5 1

Gate Bias (V)

1 kHz
3.16 kHz
10 kHz
31.6 kHz
100 kHz
316 kHz
1 MHz

- The ZrO_2 dielectric shows slight frequency dispersion which may be due to some interface charges or traps

Hysteresis as a Function of Bias Sweep

- Significant hysteresis believed to be due to charge trapping and detrapping ==>need for improved surface preparation, decreased contamination
- Hysteresis is a function of bias sweep: higher max accumulation bias results in more charge injection
- Hysteresis has been seen to increase with NH_3 treated surfaces (UMN group)

CV Walkout

1.4E-10
1.2E-10
1.0E-10
8.0E-11
6.0E-11
4.0E-11
2.0E-11

Capacitance (F)

-1.25
-1.125
-1
-0.875
-0.75

Gate Voltage (V)

Material Characterizations

Synchrotron Angle Resolved XPS of Thin ALCVD ZrO_2

O 1s
Ekin ~ 215 eV
30°
15°
45°
90°

Zr 3d
Ekin ~ 70 eV
Zr,Si-O
Zr-Si

Si 2p
Ekin ~ 150 eV
Si-O
Si-Si

Normalized Intensity [arb. units]
Binding Energy [eV]

Synchrotron XPS Differential Sputter Profile

Polycrystalline

Intensity [arb units]

Depth [nm]

Zr 3d	Zr Silicide	
Zr 3d	Zr Oxide	
Si 2p	Si	
O 1s	Zr Oxide	
O 1s	Si+Zr Oxide	

- Both XPS techiques show metallic Zr or Zr silicide at/near Si surface
- Samples pushing limits of physical metrology

AFM of As-Deposited ALCVD ZrO_2

Digital Instruments NanoScope
Scan size 1.000 µm
Scan rate 1.001 Hz
Number of samples 512
Image Data Height
Data scale 3.000 nm

view angle
light angle

0.2
0.4
0.6
0.8
µm

X 0.200 µm/div
Z 3.000 nm/div

0 deg

ZrO2 As-dep (RMS=0.204nm; P-V=2.26nm)
an.004

•AFM image of a 50Å physical thickness ZrO2 shows that the RMS roughness is approximately 2.0 Å

XTEM Analysis

- TEM image reveals that the 50 Å ZrO_2 film is polycrystalline and that there is a 15 Å interfacial layer between ZrO_2 and Si
  - since the interfacial layer thickness is greater than the EOT (13-14 Å), the interfacial layer is not pure SiO_2 and must have a moderate K value (either silicate or doped oxide)
  - no evidence of silicide layer or precipitates as suggested by XPS
- Fourier transform analysis of TEM micrograph confirms monoclinic crystal structure

XTEM Analysis

XTEM Micrograph of 65Å ZrO2 Film

50 Å ZrO_2

15 Å Silicate

Annealing Studies

N_2 and O_2 Annealing Results

- Gate stack is stable at up to 550 °C for 5 min N_2 RTA
  - Capacitance decreases at T > 550 °C
  - Jack Lee @ UT Austin has seen chemical shifts in Si XPS peaks in interfacial layer at T > 550 °C
  - Has been hypothesized that silicate/interfacial layer decomposes to SiO_2 and ZrO_2
- No significant changes in V_{FB} shift with 5 min O_2 RTA
  - As-deposited ZrO_2 shows good stoichiometry
  - Decrease in leakage and capacitance for T > 500 °C signifies further interfacial oxide growth
- Hg probe used to measure all blanket annealed samples
  - Good for relative comparisons only: underestimates leakage and capacitance and overestimates hysteresis due to contamination layer between Hg and ZrO_2

Hydrogen Annealing

Hysteresis (V)
0.5
0.4
0.3
0.2
0.1
450 500 550 600 650
Anneal Temp (^{o}C)
30 sec
60 sec

Capacitance (fF/um^2)
25
20
15
10
5
0
-3 -2 -1 0 1 2 3
Gate Bias (V)
650 ^{o}C, 60 sec H_2/Ar
As-Deposited

- 650°C, 60 sec anneal in H_2/Ar significantly improves CV “stretch out” (caused by elevated D_{it}), decreases hysteresis (caused by positive oxide charge) and V_{FB} (also caused by positive oxide charge)
- no significant changes seen in leakage or capacitance
- NOTE: Hg probe overestimates ΔV_{FB}

Summary/Tech Transfer of ALD ZrO_2

- 13.8 Å EOT demonstrated with exceptional leakage of less than 10^{-7} A/cm^2
- D_{it} looks noteworthy from CV curves (but still needs to be quantified)
- 650 ^{o}C, 60 sec hydrogen anneal is seen to significantly reduce hysteresis to an acceptable level (< 100 mV for 1 V to -3 V sweep)
- ALD process is suitable for manufacturing of 8 and 12 inch wafers (exceptional uniformity and repeatability)
- Insignificant frequency dispersion

Future Work

- Alternative surface preparations
  - nitridation, oxidation, wet cleaning
- Further electrical testing
  - SILC, D_{it} (quasistatic and/or Terman), constant current, reliability, temperature dependence
- Hysteresis and CV/IV walkout minimization
- Alternative electrodes
  - SiGe deposition in CIS

Future Work

- Improve pre-deposition surface preparation to minimize interfacial layer, defects and contaminants
- Grow thinner ZrO_2 films (20 - 40 Å)
- More microanalyses to determine origin of "silicide/metal" signature at Si surface
- Produce wafers with practical channel doping levels to determine acceptable V_T, fixed charge and hysteresis @ $V_{DD} = 1$ V

Acknowledgements

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