Thoughts on Controlling Interfacial Electron Transfer in Novel FET Structures

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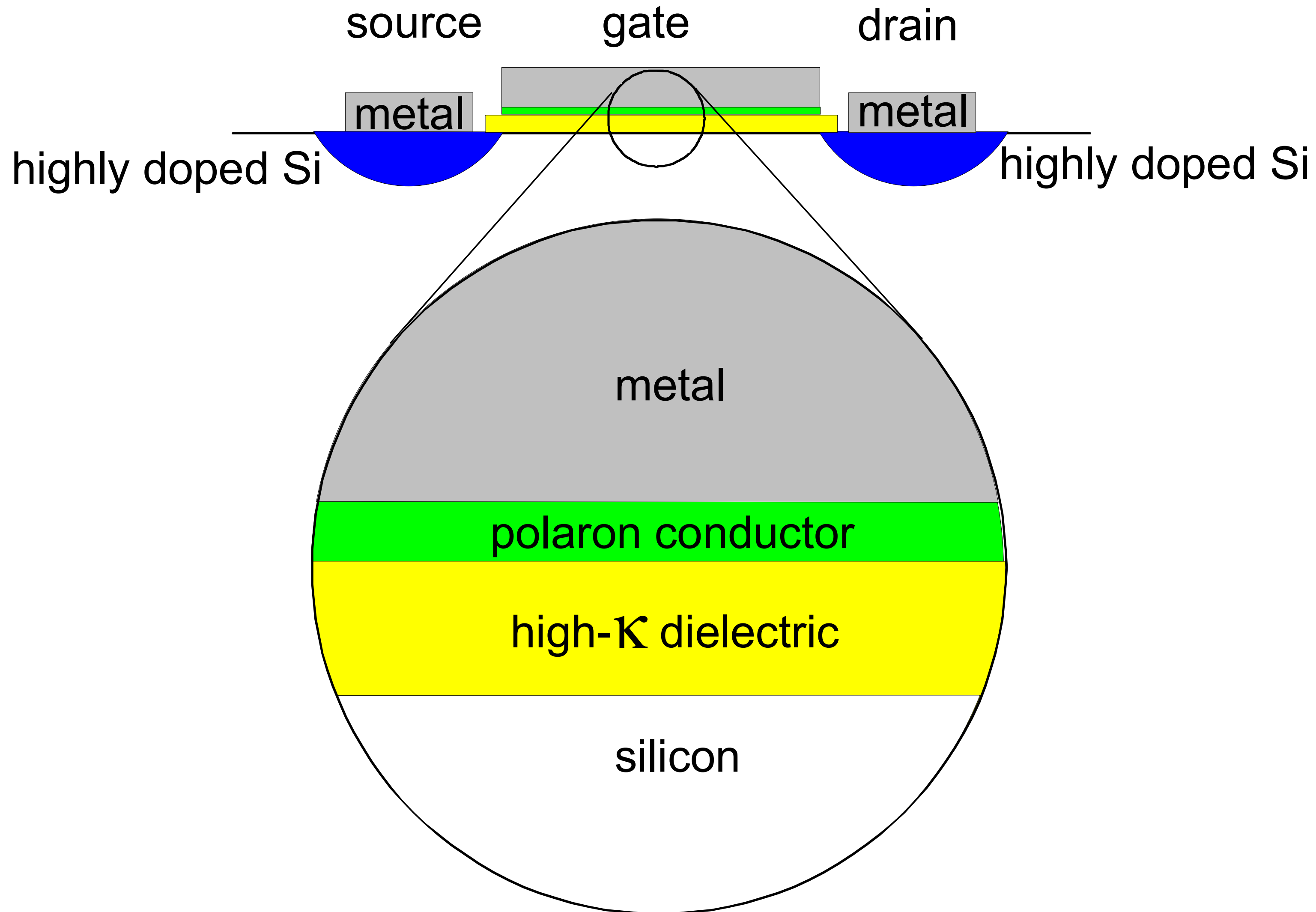
Possible Improvements in Gate Electrodes

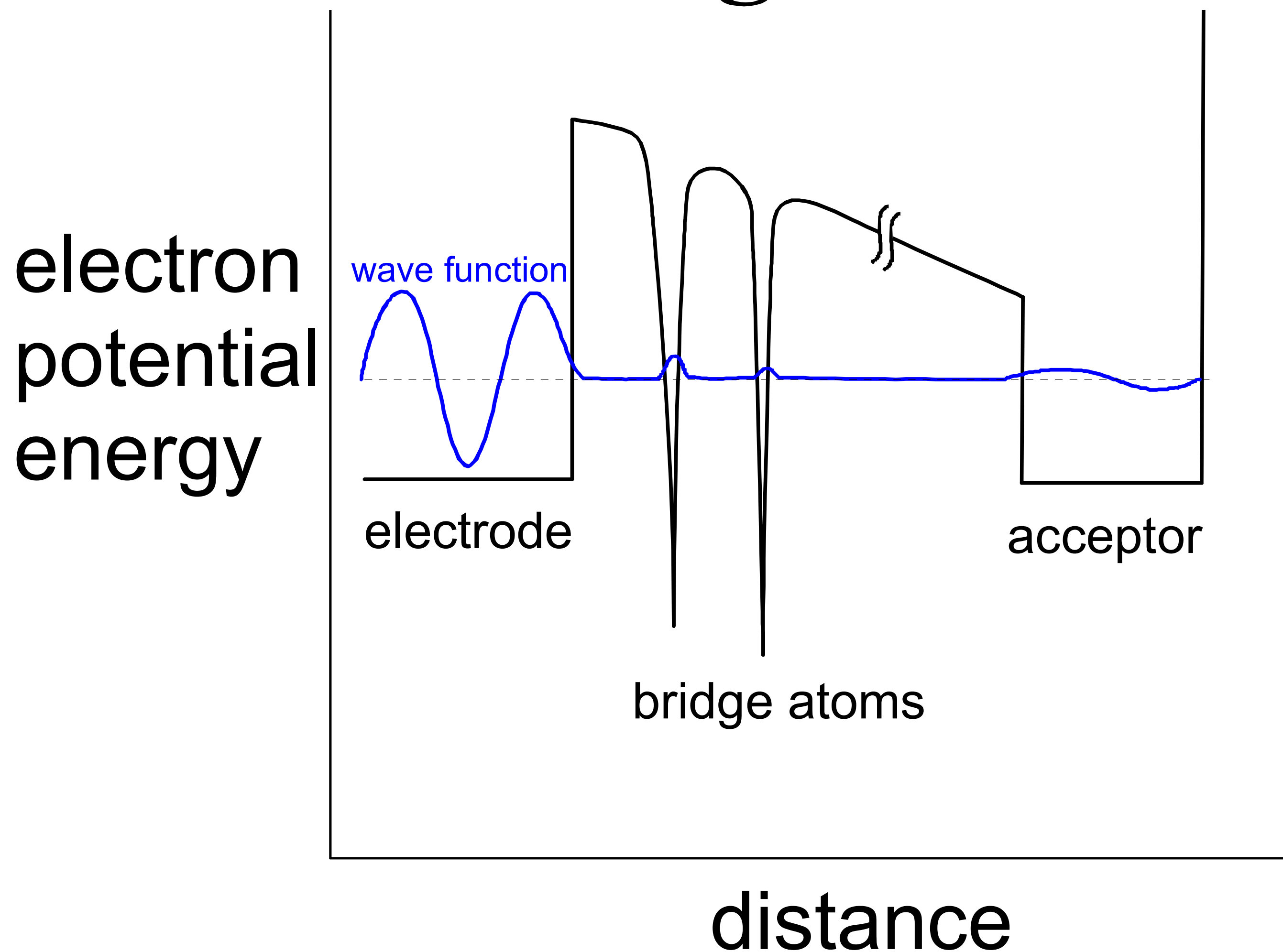
- Use gate electrode with increased charge carrier density to avoid gate electrode depletion effects seen in doped poly-silicon gates

- Use localized carriers at interface of gate electrode with dielectric to reduce tunneling rate across dielectric

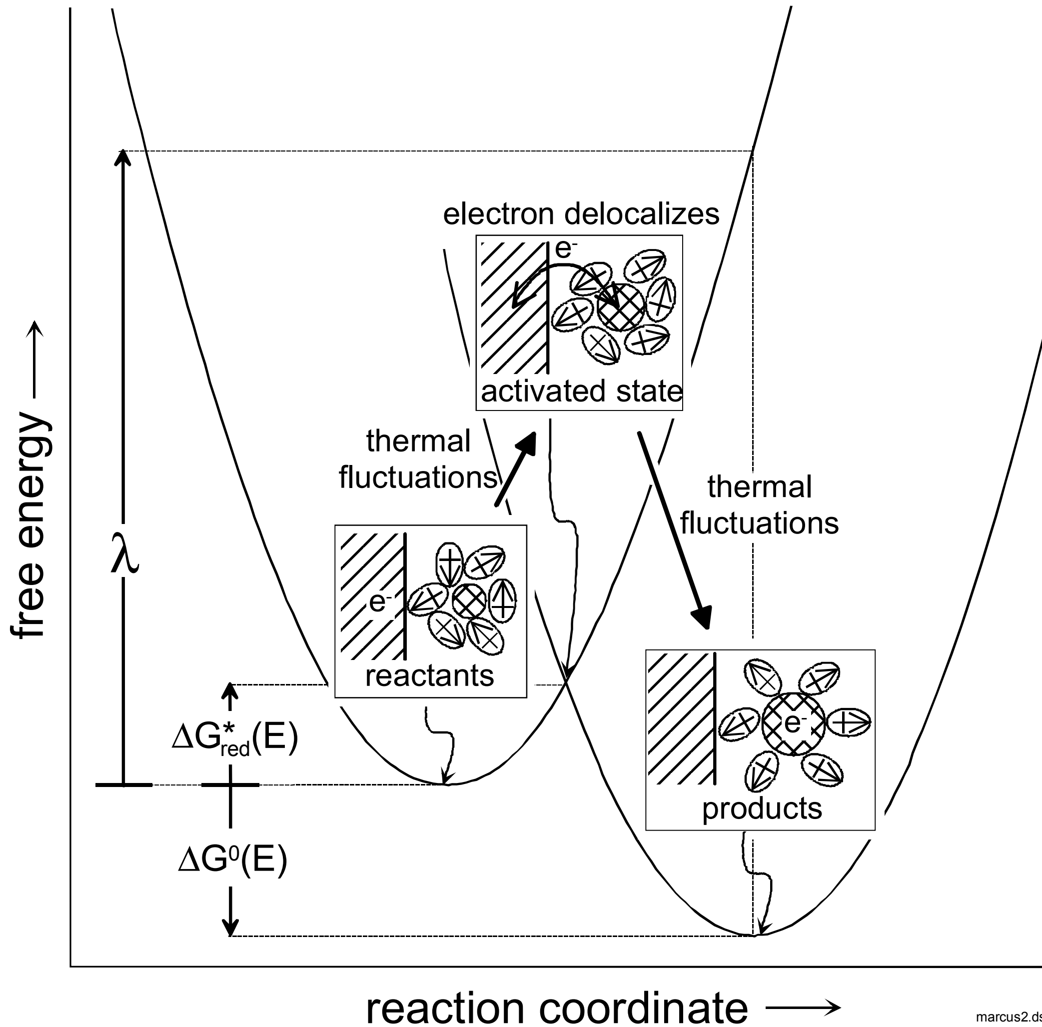
Novel Gates in FET Structure



Schematic of Interfacial Tunneling Barrier



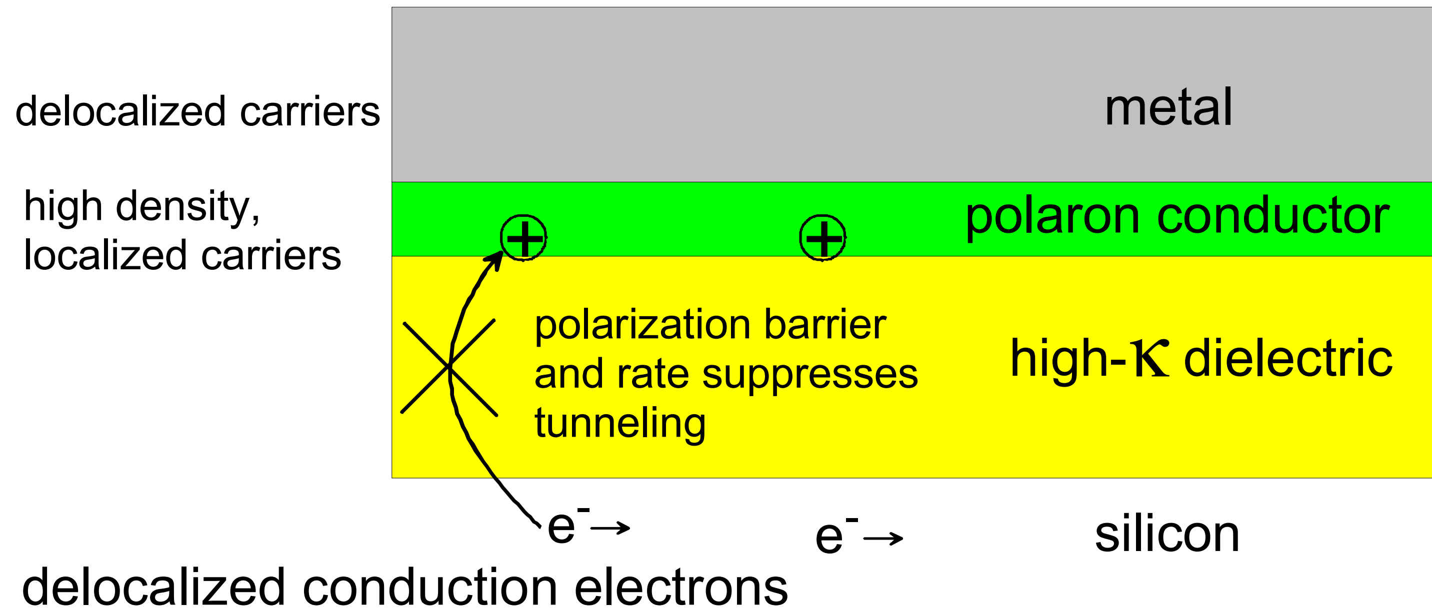
Schematic of Structural Activation Barrier



Consequences of Localized Carriers

- Localized charge $\rightarrow$ structural reorganization (polaron formation)
- Reorganization $\rightarrow$ activation barrier + limitation on barrier crossing rate

Detailed View of Gate Stack



Possible Magnitude of Effect

- Assume maximum allowable gate charging time is 10 ps
- Assume thermal velocities of atoms
- Leads to maximum allowable reorganization energy of 0.5 eV
- Should result in a 0.5 V shift in direct tunneling I-V curve

Possible Implementation

- Follow ALCVD of high-K dielectric with ALCVD of conducting oxide
- May require dopant profile of source and drain to be set prior to gate-stack formation
- If successful, may allow thinner high-K dielectric layer or thicker silicon dioxide passivation layer between channel and high-K material