Materials for Next Generation Lithography and Advanced Back-End-of-Line Interconnects – An Overview

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Outline

- Introduction
  - Technology & Business Directions
- MOSAIC (BEOL) Program
  - Cu, low κ, CMP, cleaning, integration
- Next Generation Lithography Program
  - 157nm, EPL, EUV, ...

Electronic Materials Business

Morton
- PWB

LeaRonal
- PWB
- Semiconductor Packaging
- Connector
- Industrial Finishing

Shipley
- PWB
- Industrial Finishing
- Semiconductor Fabrication

Rodel
- CMP
- Silicon Wafer
- Memory Disk

Rohm and Haas Electronic Materials

- Shipley Company
  - Shipley Ronal
    - GMF
    - Connector Semi-Pack
    - PWB
  - Shipley Microelectronics
    - Semiconductor Manufacturing
- Rodel
  - CMP
  - Silicon Wafer
  - Memory Disk

Electronic Material Sales: 1992-2000

$ MM

Year	'92	'93	'94	'95	'96	'97	'98	'99	'00	'05
Sales ($ MM)	217	231	269	335	358	400	400	750	1,200	2,000+

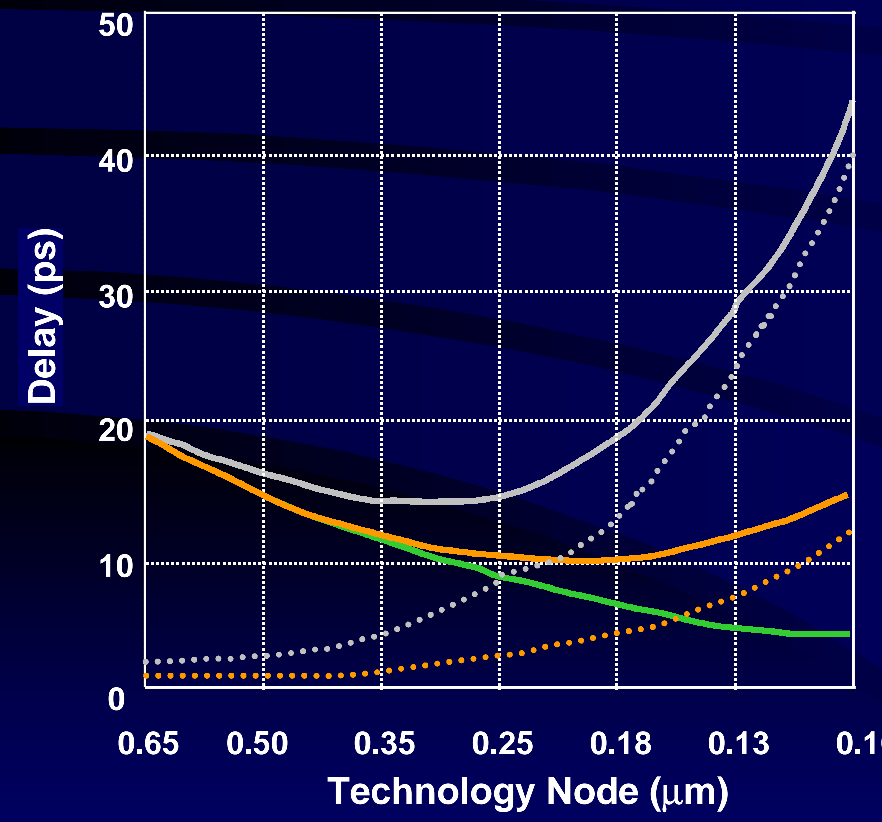
PWB - Connectors - Semiconductor Packaging

Microelectronics

Circuit Delay and Interconnect Materials

- The diagram below illustrates the problem of "RC time delay"- the physical effect which dominates as metal interconnects crowd closer together

☞ **Cu interconnects** and **Low-κ dielectrics** are required for smaller, faster devices

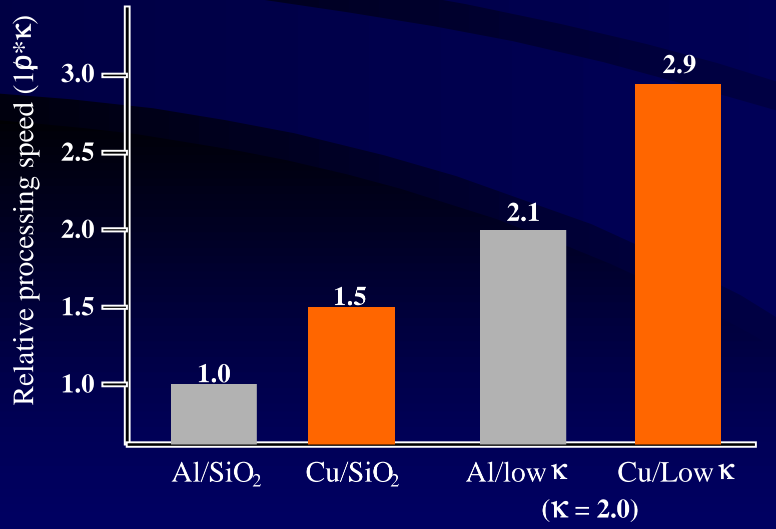


Gate Delay
Interconnect Delay, Al/SiO_2
Sum of Delays, Al/SiO_2
Interconnect Delay, Cu/Low κ
Sum of Delays, Cu/Low κ

Data from Mark T. Bohr, "Interconnect Scaling - The Real Limiter to High Performance ULSI"; Proceedings of the 1995, IEEE International Electron Devices Meeting; p 241-242.
Adapted from Sematech Update 9/96 - KA Monnig

Why Copper and Low κ Dielectrics?

- Processing speed is determined by the circuit delay
- Circuit delay (τ) is the inverse of resistance (R) x capacitance (C)
  - ❖ $\tau = 1/RC$
- Minimizing delay increases speed:
  - Decrease metal conductor resistivity (ρ) to decrease resistance:
    - **Aluminum** => **Copper**
  - Decrease insulator dielectric constant (κ) to decrease capacitance
    - Silica (glass) => **low κ dielectrics**



- Moving to Cu/low κ increases speed ~3x over Al/SiO_2
- Cu/low k technology enables the production of chips at 0.13 µm feature sizes and below

The Concept of MOSAIC

MOSAIC
PROCESS INTEGRATION

PHOTORESISTS
DUV, 193 nm,
Next Generation Lithography

CMP
(Rodel)

ELECTROPLATING
Copper,
Alternate Metals/Alloys

WASTE RECOVERY
of Shipley Products

PROCESS CONTROL
Bath Analyzer

ILD
Full Range of k,
Photo-ILD

SEED/BARRIER LAYERS
Solution,
MOCVD (UP Chem)

ANCILLARIES
Developers, Removers,
Rinses, Other

Copper Electroplating: *Bottom-Up Fill*

(a) 13 sec

(b) 20 sec

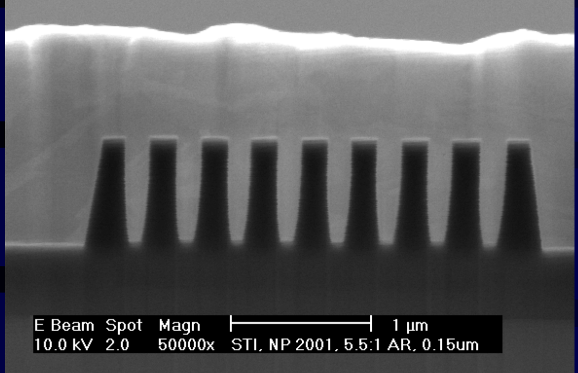
(c) 27 sec

(d) 33 sec

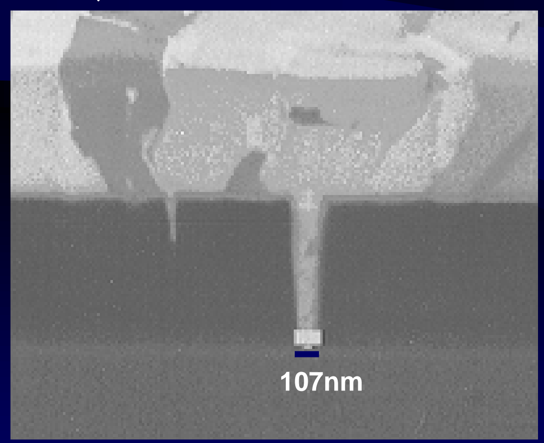
- Selection of additives in plating formulation determines conformal vs. “bottom-up gapfilling

Fabrication of Inlaid Copper Wiring by Electroplating

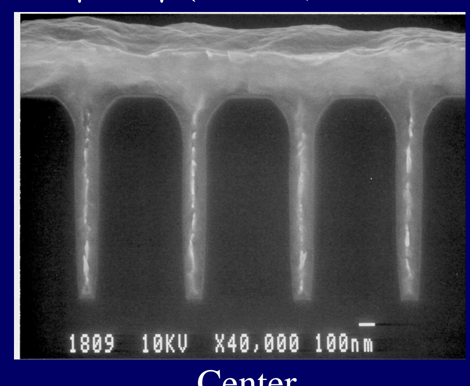
0.15µm dense trenches



0.11µm isolated trench



0.12µ x1.2µ (10:1 AR) trenches

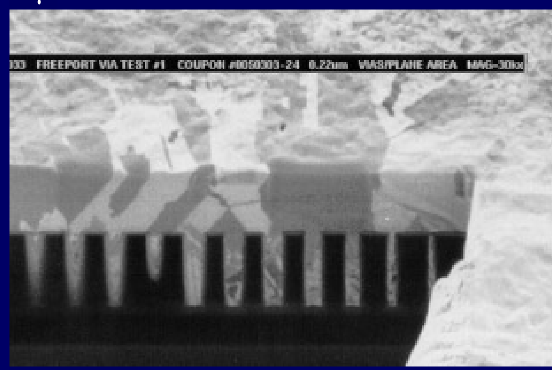


Center

1856 10KV X40,000 100nm

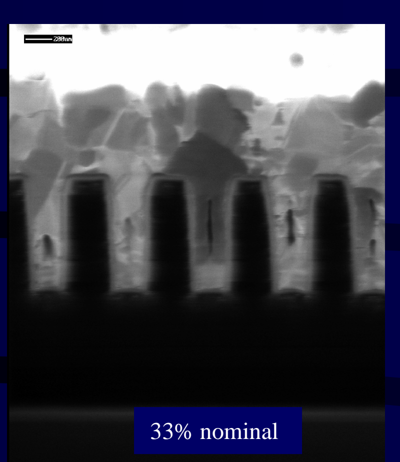
Edge

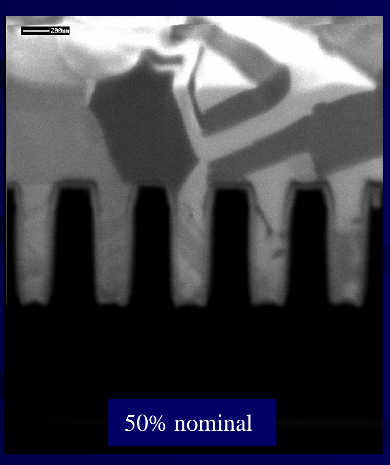
22µm dense vias

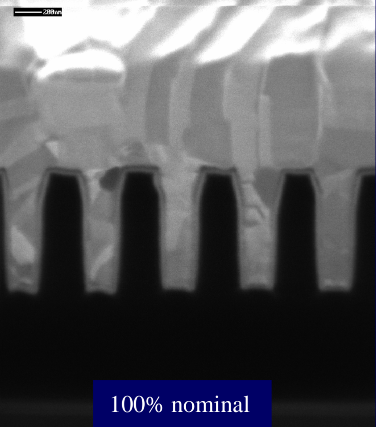


- High aspect ratio (10:1), 100nm structures filled using current generation EP Cu products

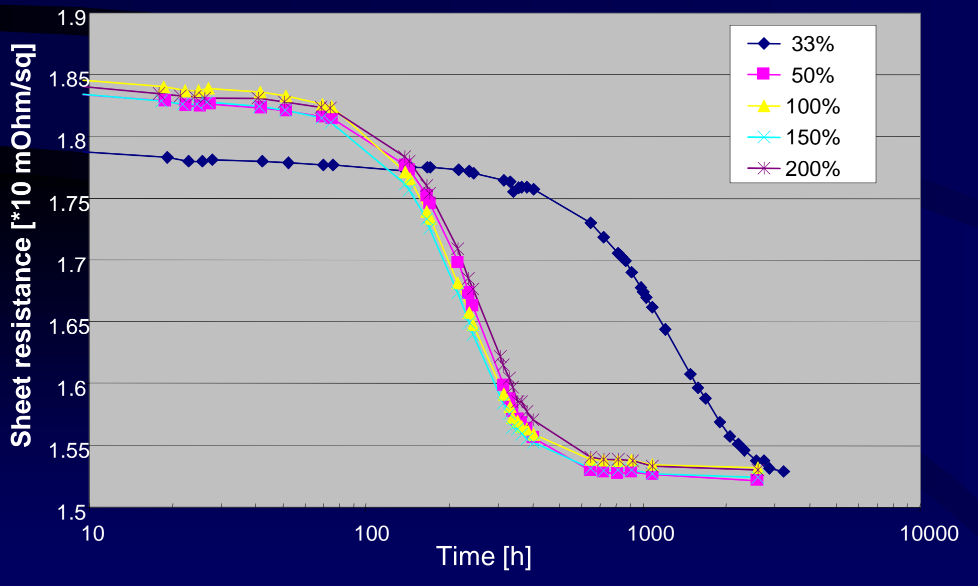
Effect of Additves on Cu Electrodeposition







- FIB microscopy shows void-free gapfill @ [Additive] $\geq$ 50% of nominal level

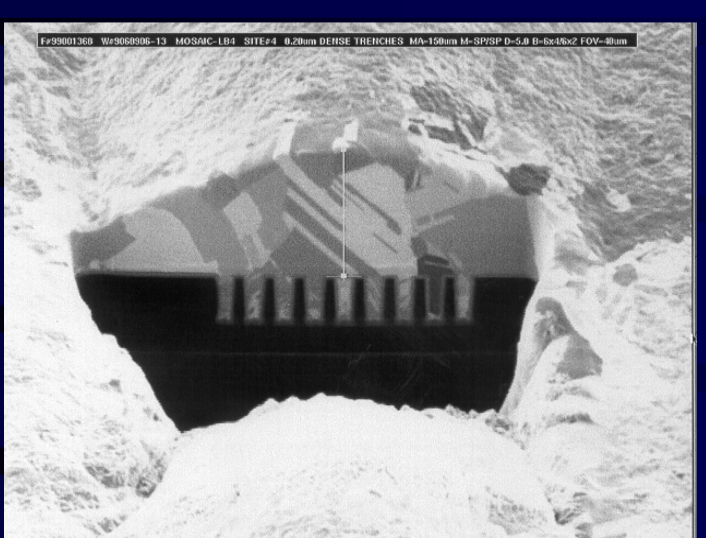


- Modulation of [additive] in bath increases time for self-annealing to reach minimum resistivity

Data obtained in collaboration with IMEC

Waveform Modification for Improved Uniformity

DC Waveform

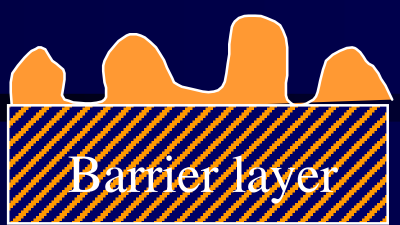


Reverse Pulse Waveform

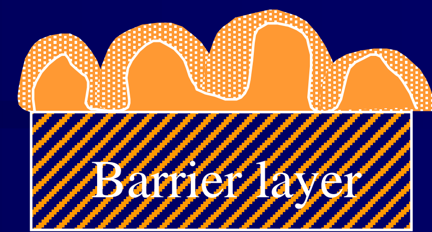
• 0.20µm trenches, AR 4:1, 250Å Ta barrier, 1000Å Cu seed, 1µm EP Cu

- Bottom-up fill mechanism leads to "bump" plating over dense features with standard POR
- Plating recipe incorporating a Periodic Pulse Reverse waveform polishes back high current density regions, improves within-die uniformity
- Improved uniformity is directly correlated with improved CMP performance

Seed Layer Enhancement

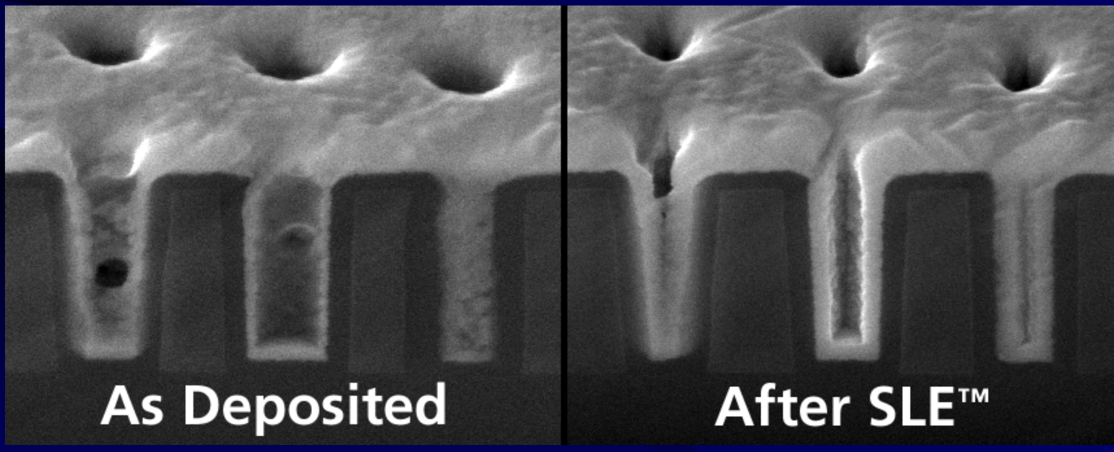


Seed Layer Enhancement



- Discontinuous seed layer (as-deposited, or due to etching of thinly plated areas) leads to patchy initiation of plating, resulting in poor gapfill (voids)

- Seed Layer enhancement deposits additional Cu on discontinuous base layer and makes adjacent regions of Cu seed contiguous. Uniform initiation of plating eliminates voids

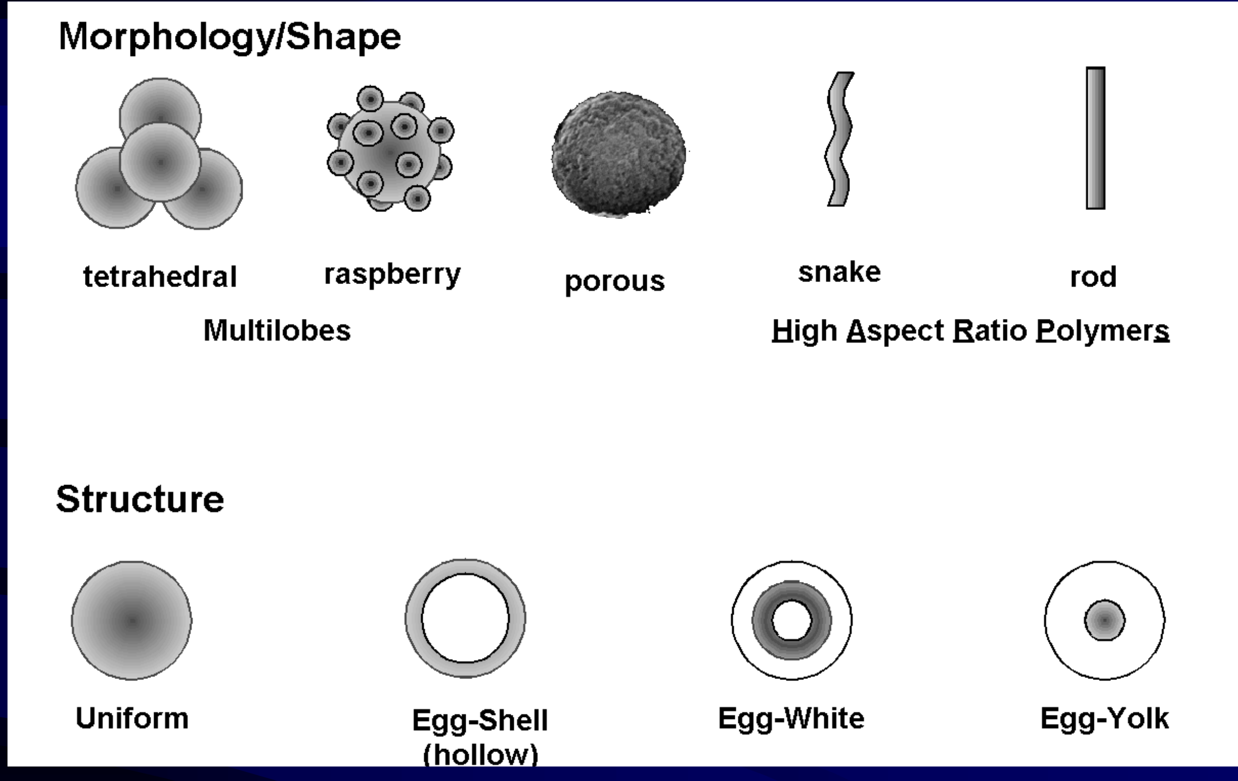


Courtesy of Semitool

Cu Electroplating:
Challenges for the Future

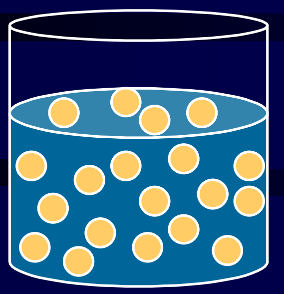
- Seed and barrier layer chemistries for 100nm node and below
  - Repair, make thinner, eliminate
- Co-optimization of EP Cu and CMP chemistries
  - Improved planarization and defectivity across 300mm
- Development of specialty Cu formulations for improved device electrical performance

Nanoparticle Fabrication for Porous ILDs



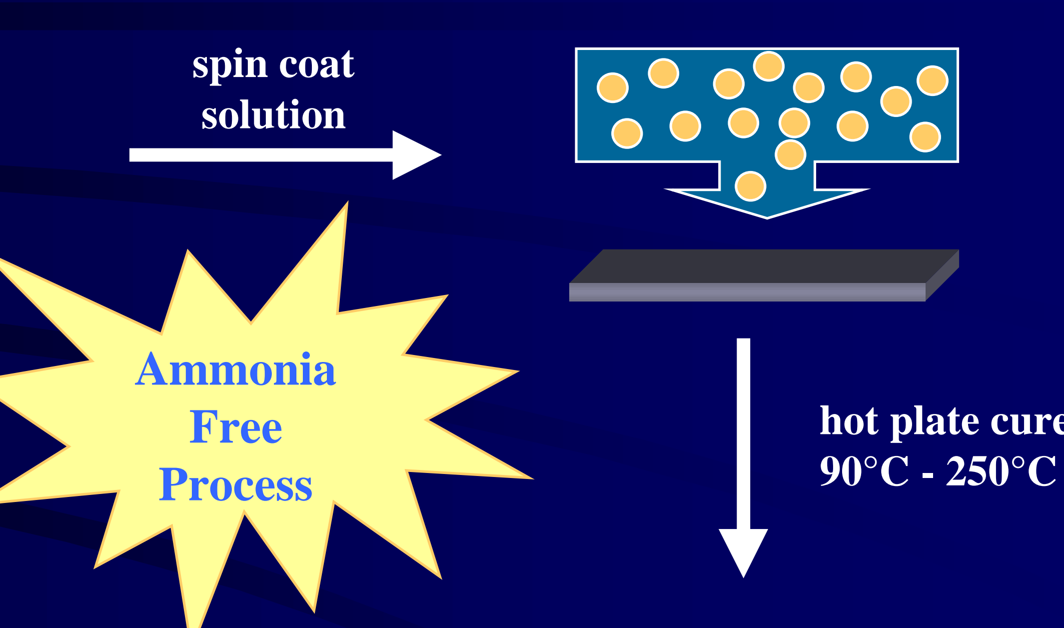
- Fabrication of structurally-tailored polymer particles is a core competency of R&H
- Particles are made in sizes ranging from µm to nm
- Particle dispersions are made in high purity and at scale

Porogen Approach to Formation of Nanoporous ILD Materials

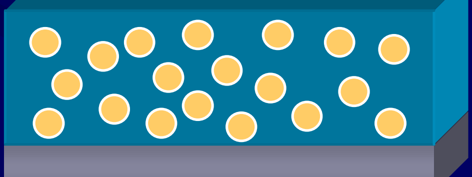


porogen matrix composite solution

spin coat solution

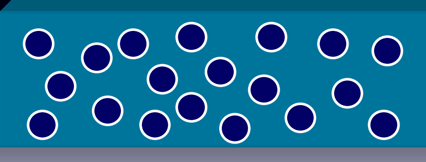


hot plate cure 90°C - 250°C



composite film

furnace anneal 400 - 425°C



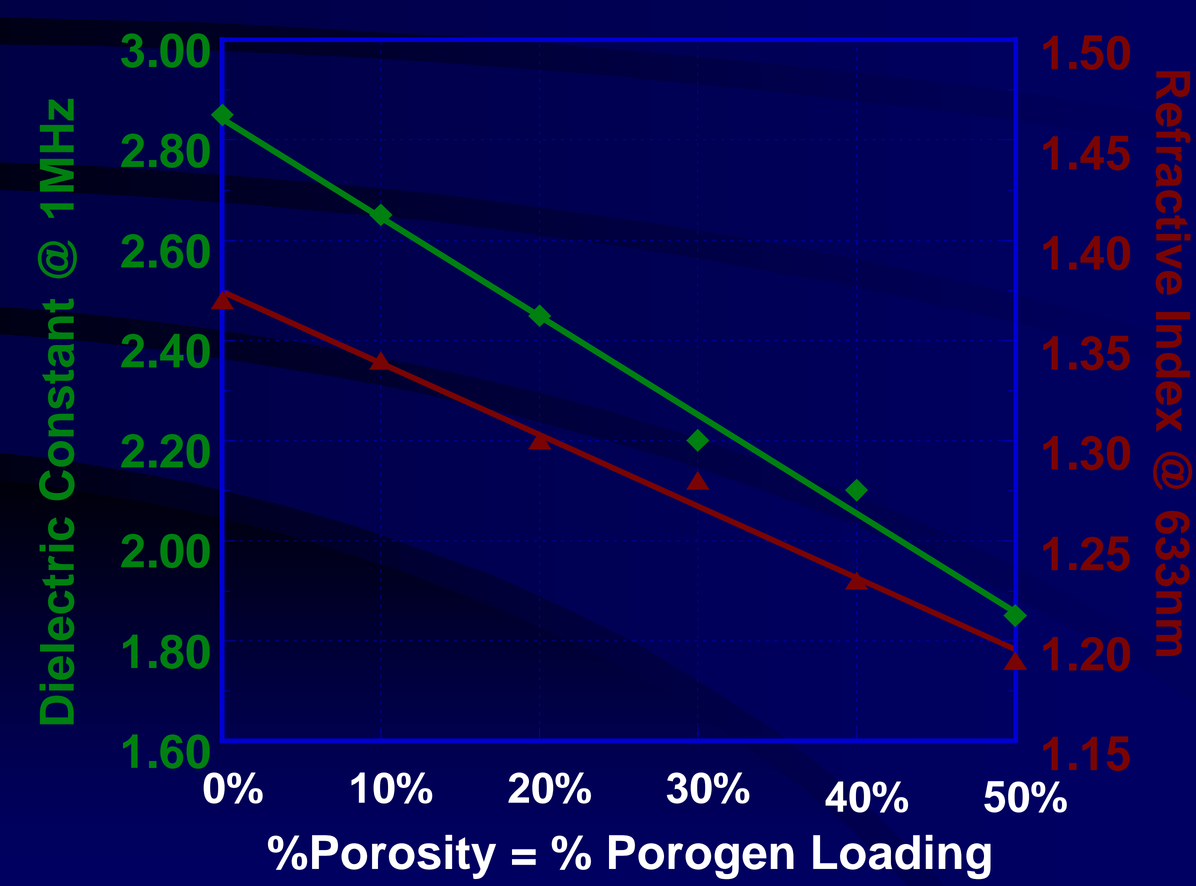
nanoporous ILD film

Polymeric Porogen Particles

- Transmission electron micrograph of a thin section of polymeric porogen nanoparticles embedded in a silsesquioxane matrix
- Average size of particles in TEM is 20 nm
- Modification of polymerization conditions can produce particles of 1-5nm diameter with narrow size distribution

Porous Organosiloxane Films

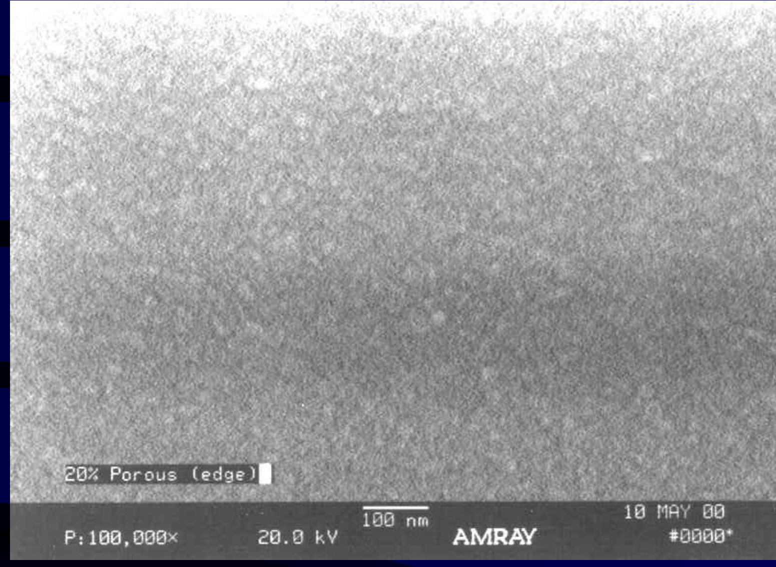
- Incorporation of porogen particles into organosiloxane matrix, followed by thermal decomposition of the porogens produces nanoporous films
- Dielectric constant and refractive index track porogen loading



Porous Low κ Dielectric Films from Polymer Nanoparticles

κ = 2.3 - 2.4

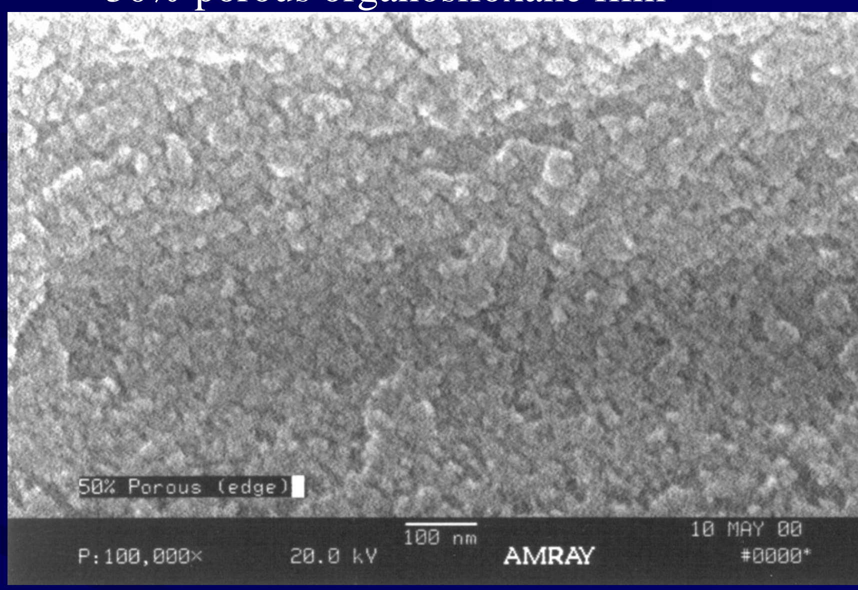
20% porous organosiloxane film



Average pore radius = 1.3 nm

κ = 1.8 - 1.9

50% porous organosiloxane film



Average pore radius = 4.8 nm

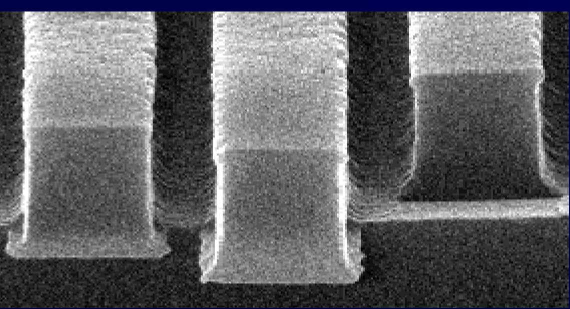
- Uniform pore formation equivalent to porogen particle size distribution
- Porogen compatibility with both inorganic (Si-O) and organic matrix materials

Standard processing, 200 mm wafer:

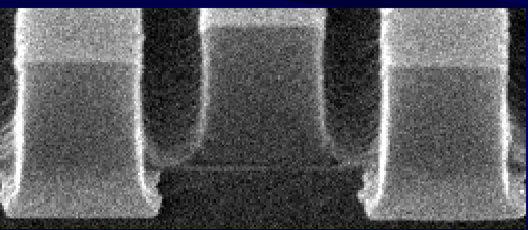
Spin speed	3000 rpm
Hot plate cure	90°C/60sec &150°C/60sec
RTP furnace cure	425°C/1 hr

Photoresist Patterning on Nanoporous ILD

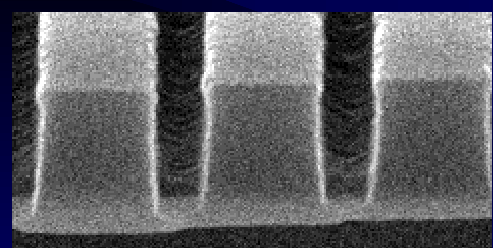
250 nm



230 nm



210 nm



30 mJ/cm²

Initial results:

(lithography not optimized!)

- Good pattern formation
- Interfacial profile control
- Adhesion

Process Conditions

Substrate:	200 mm 1-20 Ω silicon <100>
ILD Layer:	8,000 Å porous organosiloxane
Porosity:	30% porous (Est. k= 2.1)
ARC:	none
Resist:	UV210-0.6, 5766 Å
Soft BaKe:	130° C/60s
Expose:	ASML5500/300 (0.63NA, 0.850σ_o, 0.425 σ_i)
Post Exposure Bake:	130° C/60s
Develop:	MF CD-26, 60 sec. single puddle

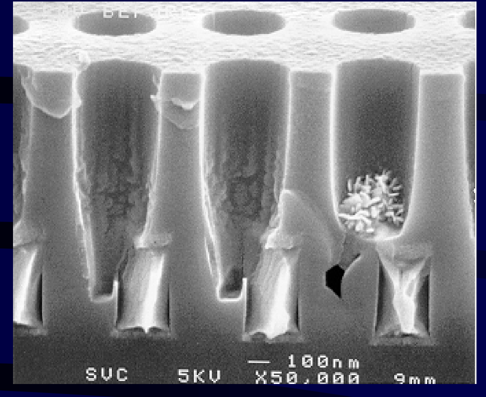
Low κ Dielectric: Challenges for the Future

- Demonstration of viable nanoporous organic ILD
- Highly porous ($\kappa < 2.0$) ILD capable of withstanding standard CMP and integration processing
- Ultra-low κ ILD ($\kappa < 1.7$) and beyond??
- Photoimageable ILD

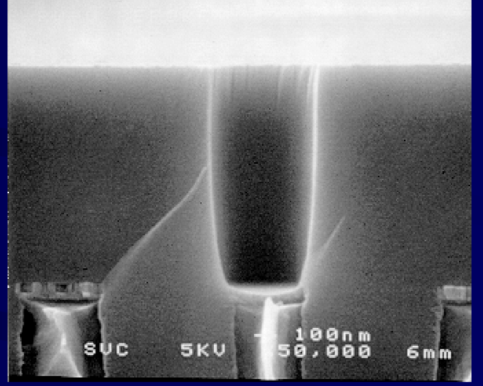
Shipley- SVC

PRX-417 Post-Etch Residue Remover

- PRX-417 completely removes polymers on the bottom and inner walls of high-aspect ratio vias without metal undercut

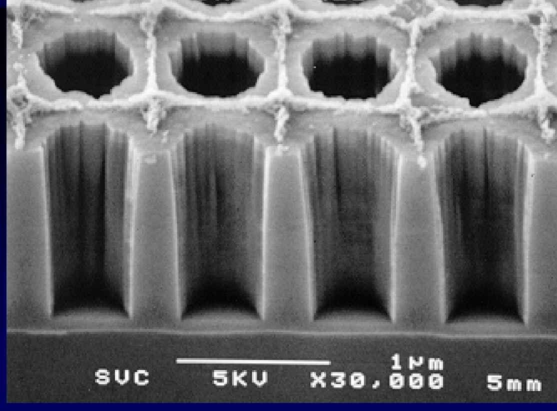


Before Clean



Via CD = 300 nm,
Aspect Ratio = 3:1

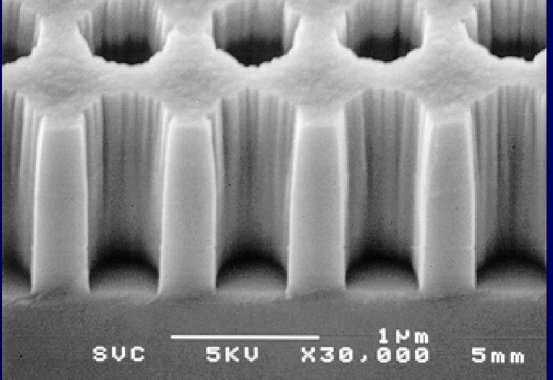
PRX-417, Static Bath, 5-10min., 23°C
DI Rinse, 5 min



CVD Doped Oxide

SiN

PECVD Un-doped Oxide

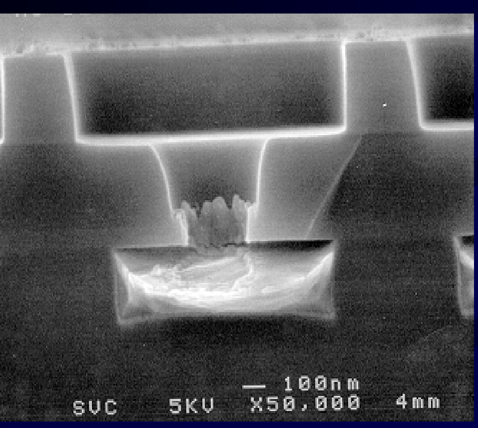


Via CD = 400 nm

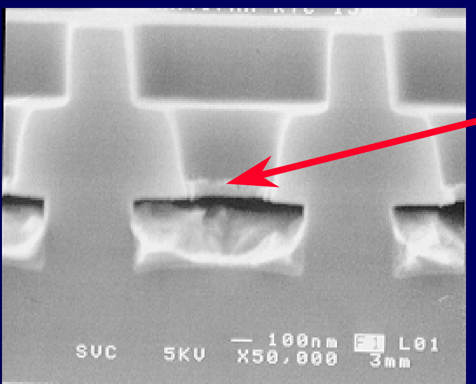
PRX-417 Post-Etch Residue Remover

- PRX-417 can remove low-k dielectric sidewall polymers without damaging or degrading low-k films or properties

Before Clean



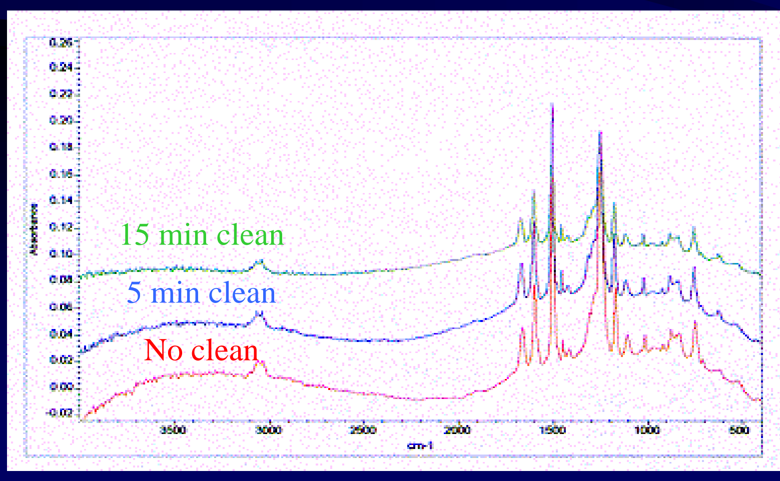
CVD Oxide
SiN
Cu/Low κ

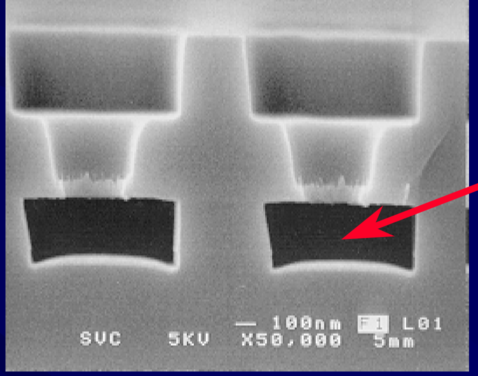


Clean removal of sidewall polymer; no Cu corrosion

PRX-417, Static Bath, 15min., 23°C
DI Rinse, 5 min

Compatibility with organic ILD (FLARE)



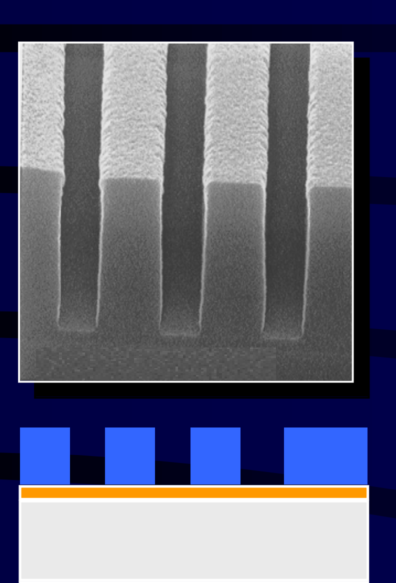


Note: all copper has been etched away

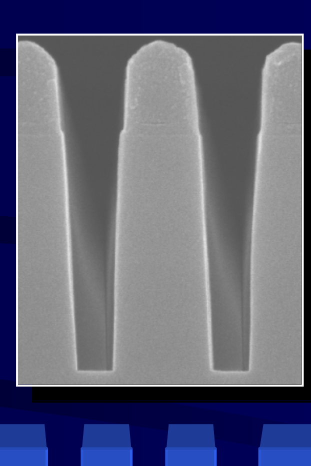
Hydroxylamine Formula

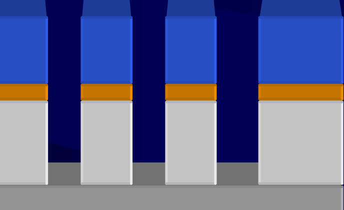
- **Short-term:** Non-hydroxylamine based photoresist removal and post-etch cleaning
- Effective aqueous or solventless cleaning chemistries
- Cleaners, EBRs, and related ancillaries for Cu-low κ Dual Damascene processing
  - Integration with complex stacks of multiple new materials
- Post-etch, post-CMP particle removal at 100nm node and below

Copper Damascene Integration

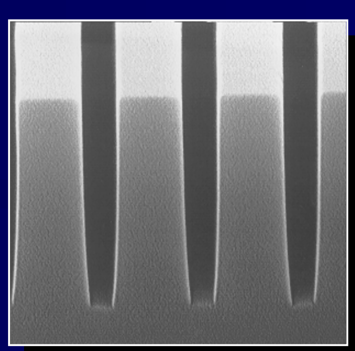


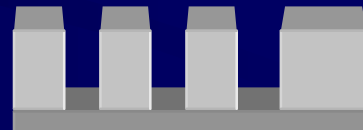
- Oxide/nitride stack
- AR3 coating
- UV210 photoresist coating
- ASML 5500/300 patterning
- LDD26 developer
- Low-κ porous ILD
- *AR7, ViPR*





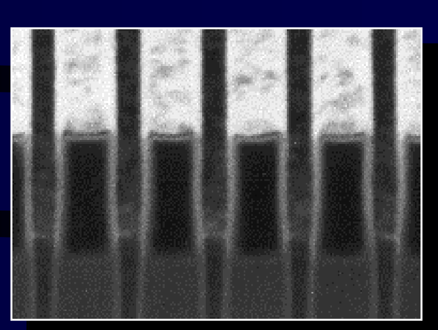
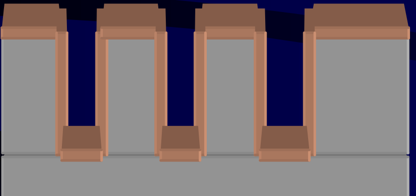
- AR3 etch
- Oxide etch
- *PERR*



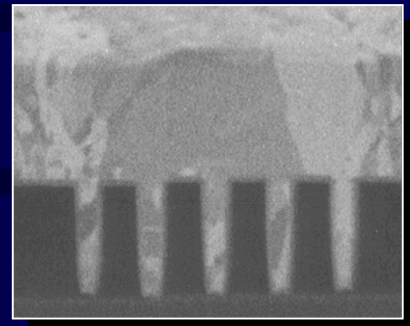
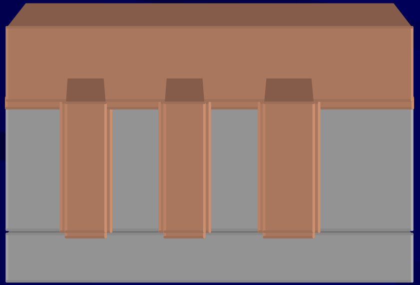


- Photoresist strip
- Post-etch strip
- SVC*strippers*

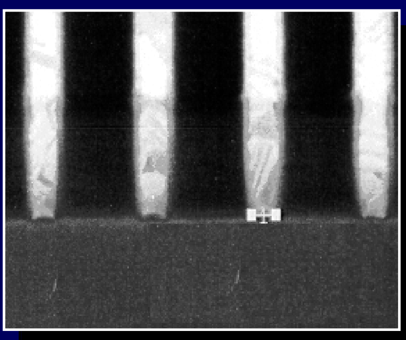
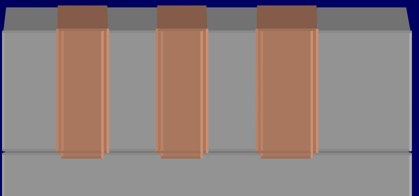
Copper Damascene Integration

- PVD Ta or TaN barrier
- PVD copper seed

- *Seed layer chemistries*
- EP Cu
- Waveform recipe

- Copper CMP RODEL
- Barrier CMP RODEL
- *Post- CMP cleaners*