Microelectronics Packaging

Processing Overview, Industry Trends and ESH Issues

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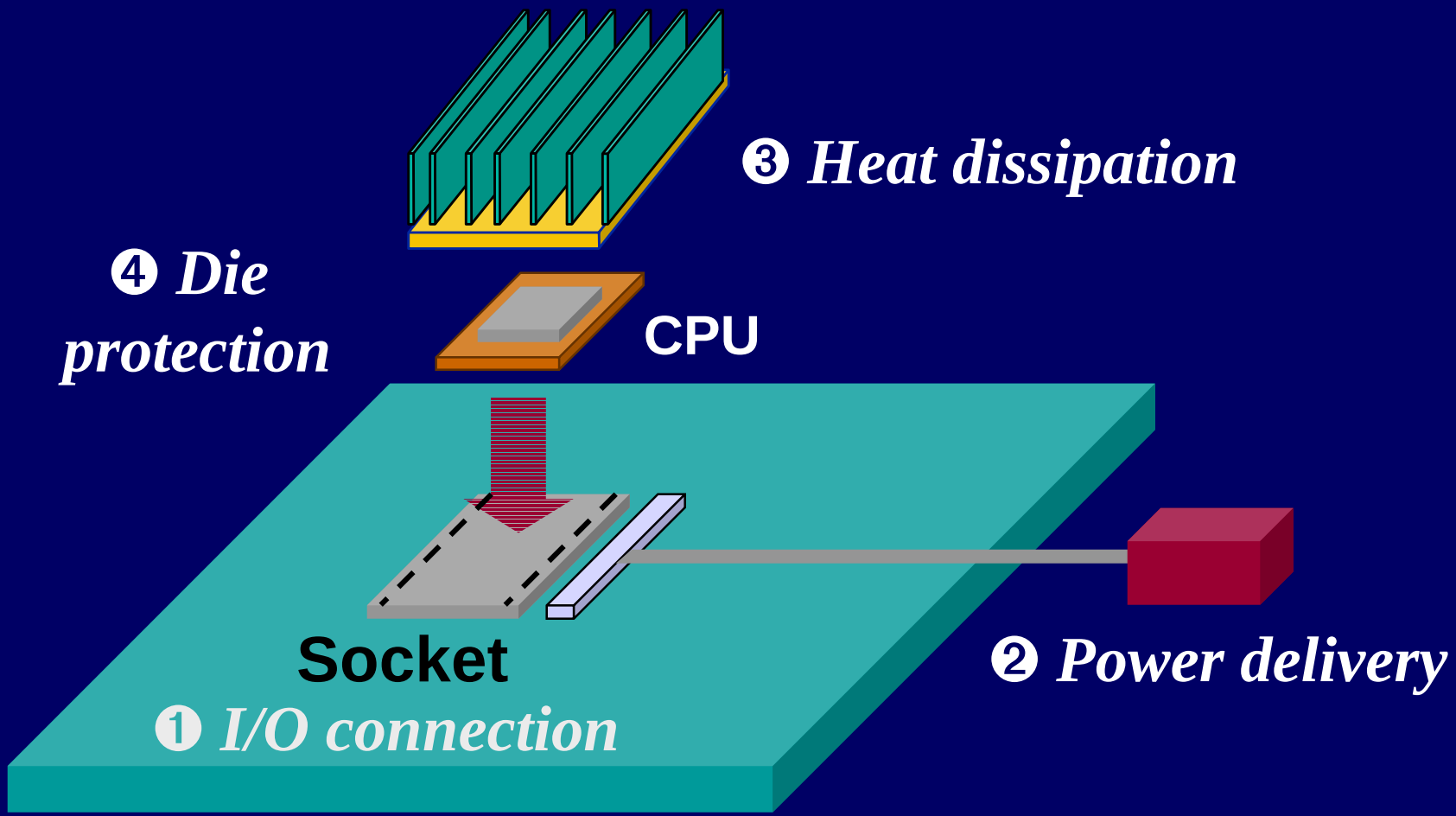
Outline

- **Major packaging functions and key issues**
- **Wire bonding and wireless bonding process flows**
- **Industry trends in packaging processes**
- **ESH issues**

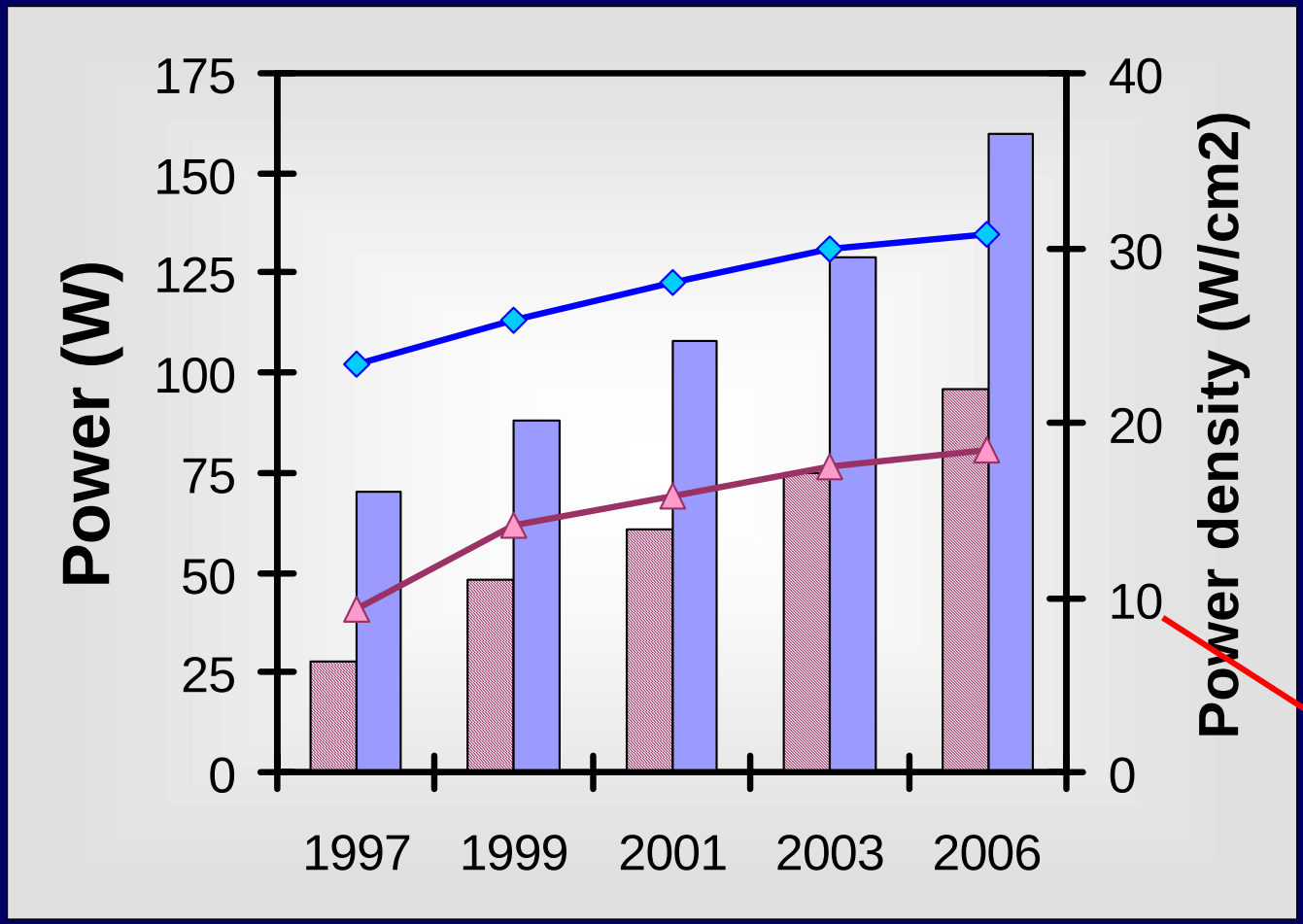
Key Packaging Functions



Critical Packaging Functional Issues

- **Heat dissipation: increase in transistor density causes increased power density**
- **I/O: number of terminals continues to rise even as package size decreases**

Technology Roadmap
Heat Dissipation Requirements



Key:

Server

Desktop

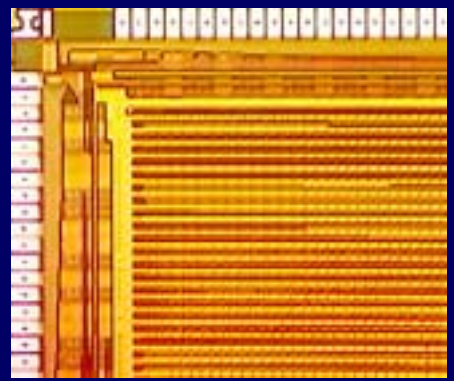
Bars ➜ W

Lines ➜ W/cm²

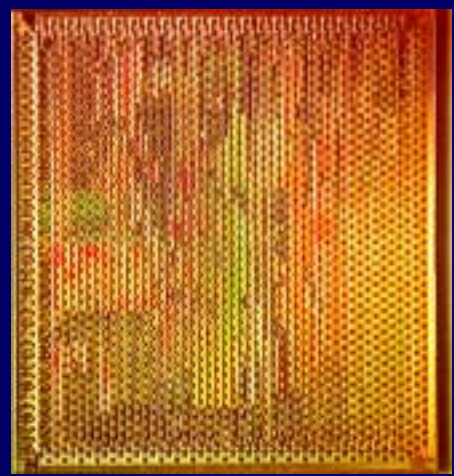
10^5 W/m²

I/O Solutions

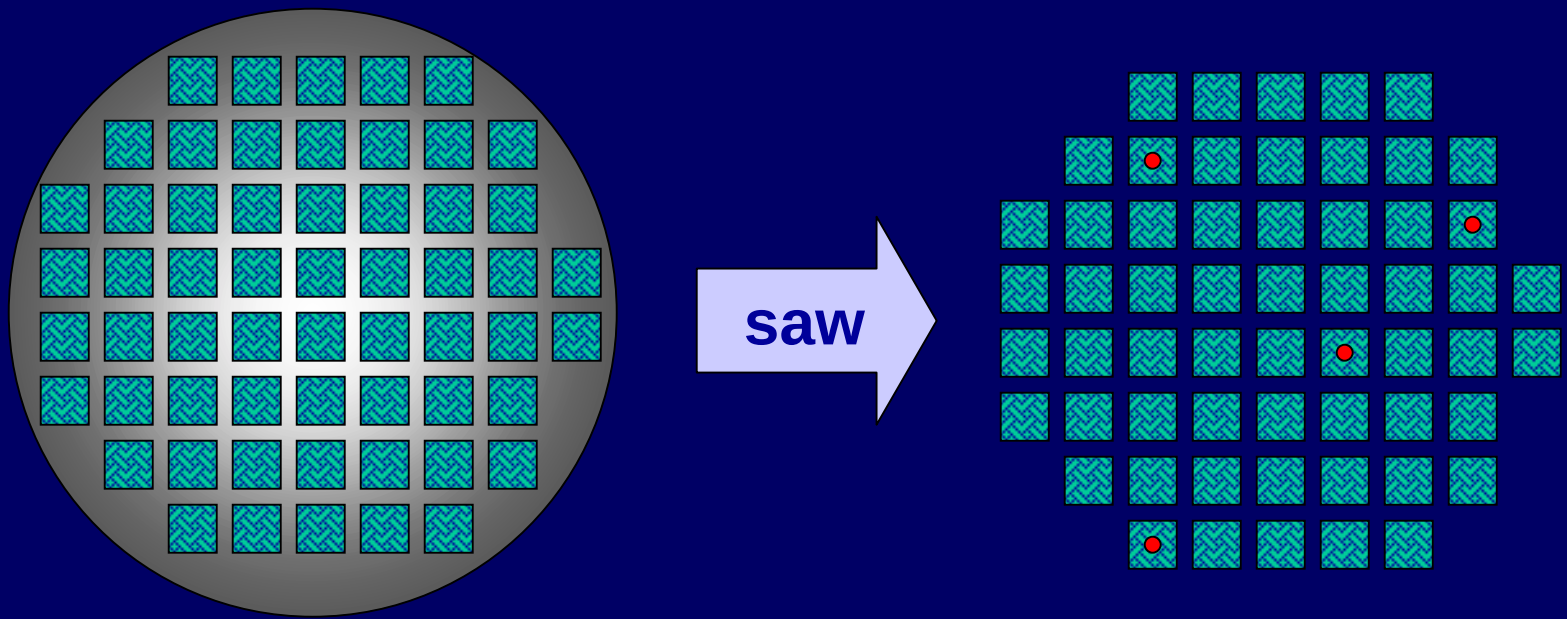
- **Wire bonding: number of terminals limited by pad density at perimeter**



- **Wire-less bonding: no perimeter limitation -- terminals limited only by areal density (or pitch) of solder bumps**

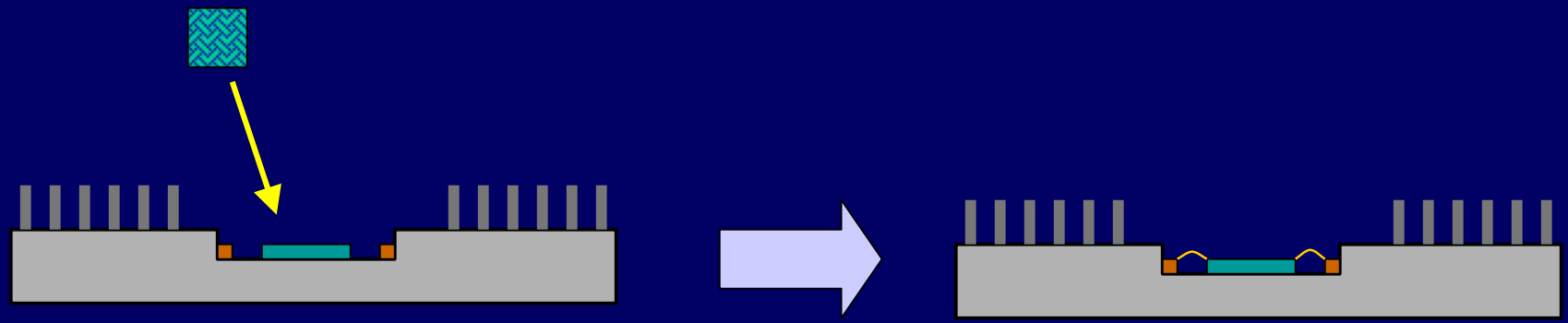


Packaging Process Flow: Saw wafer into individual die



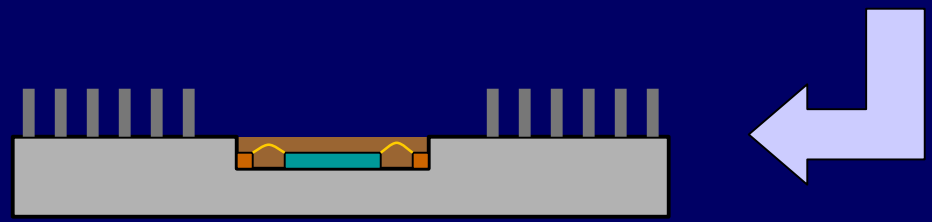
- **bad die**

Wire bonding packaging process



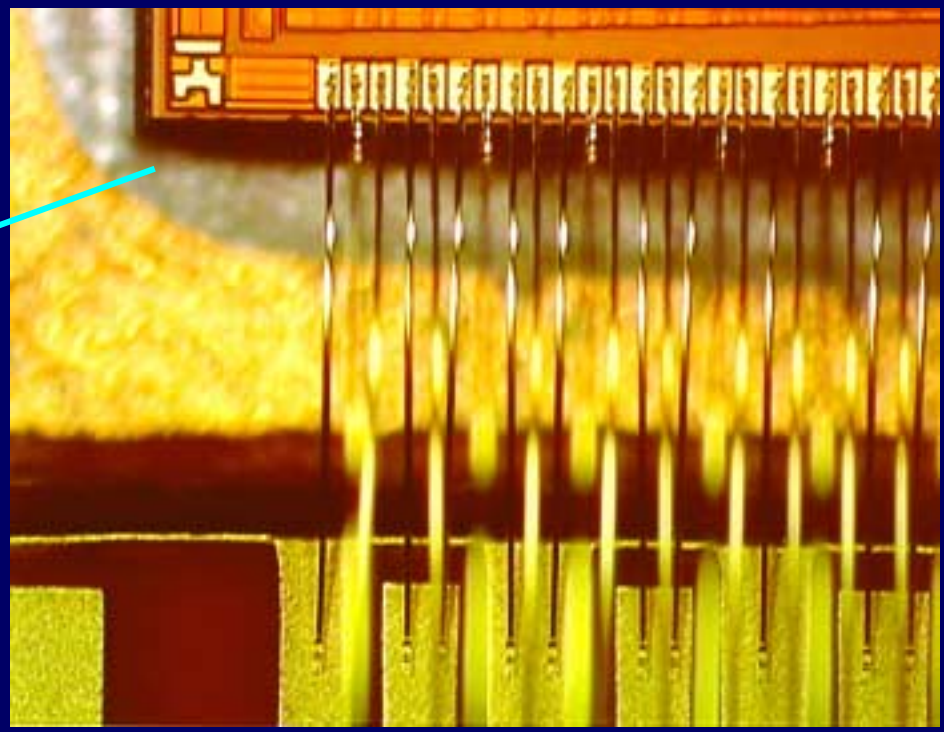
attach die to package with adhesive

wire bond pads to package shelves

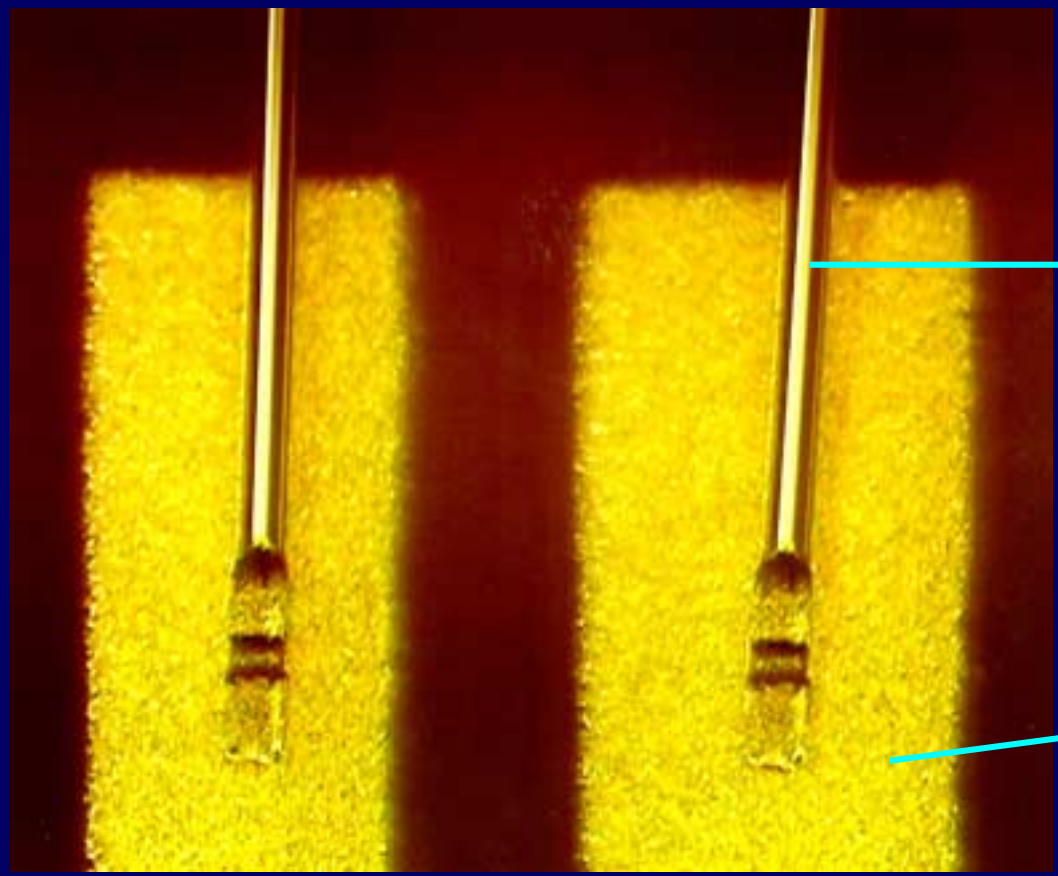


seal package

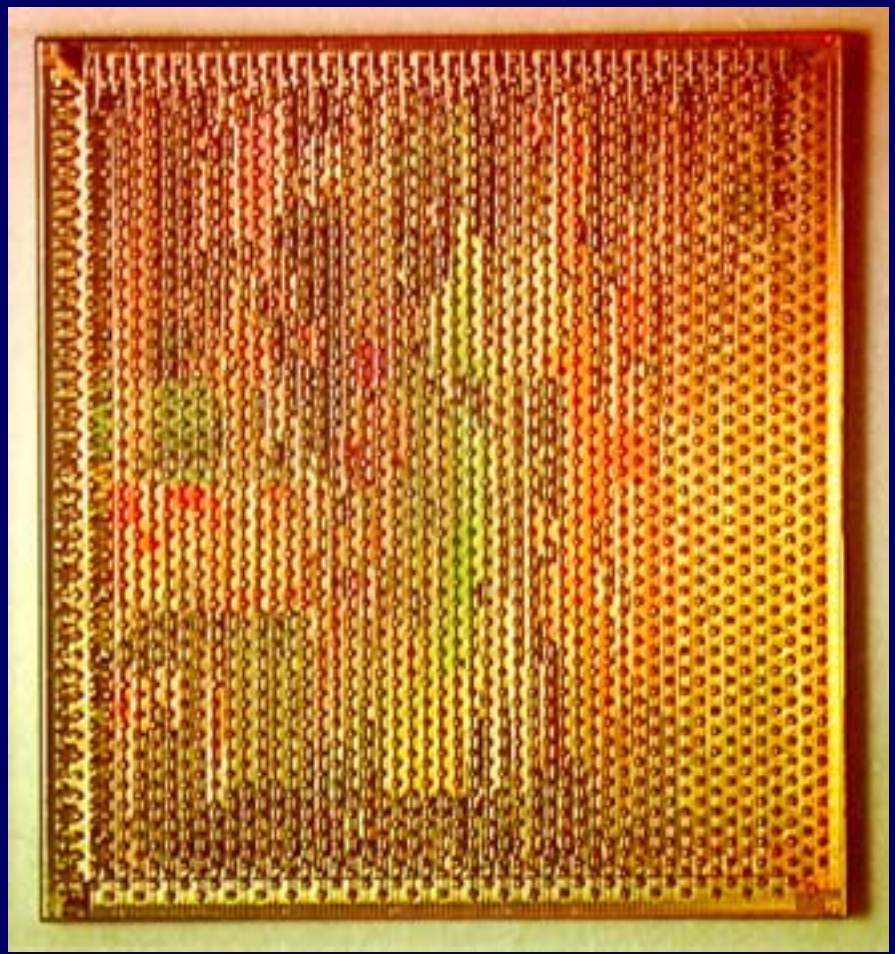
Wire bonded die (one corner shown)



Wire bonding
wedge bond closeup



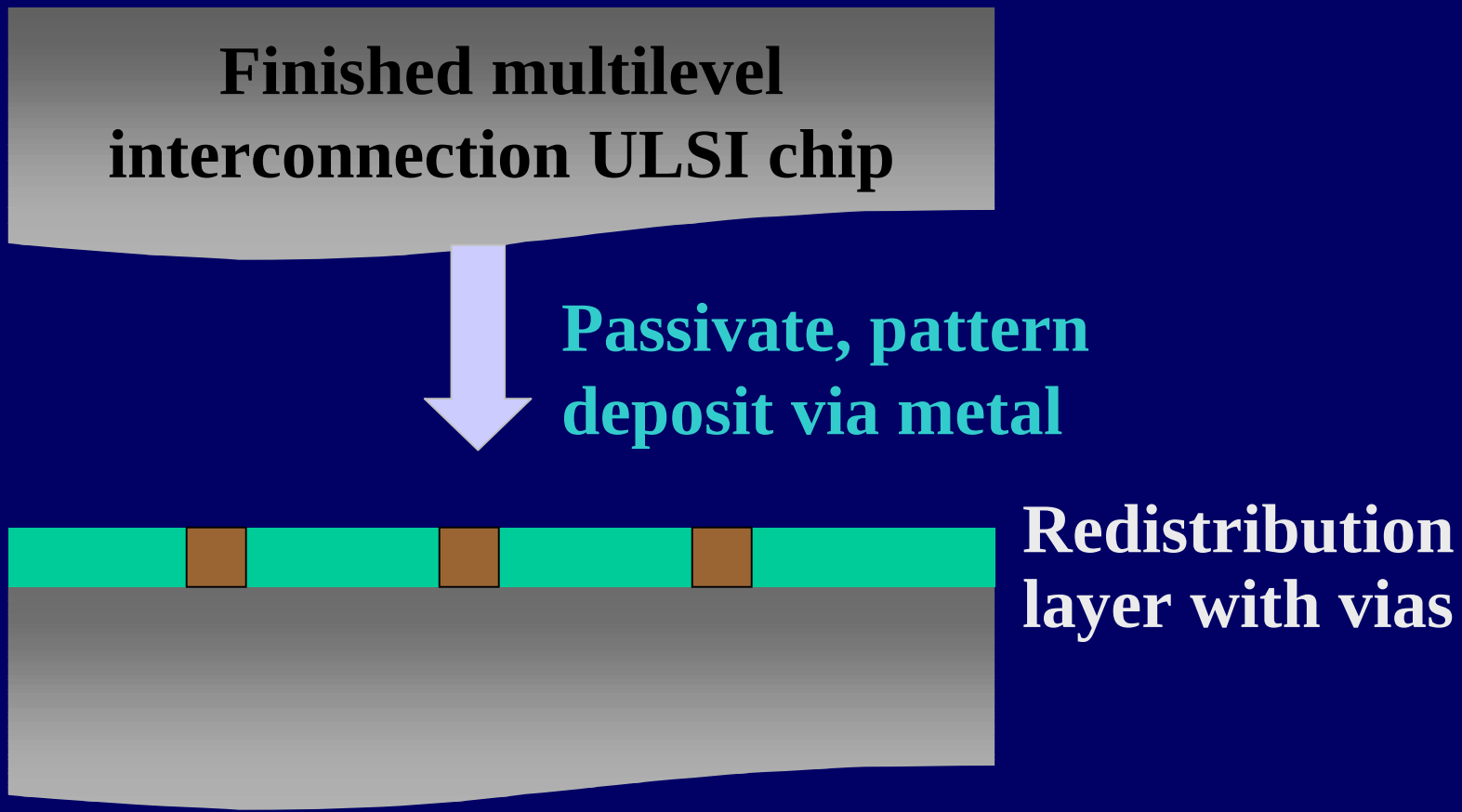
Wireless bonding solder bumps



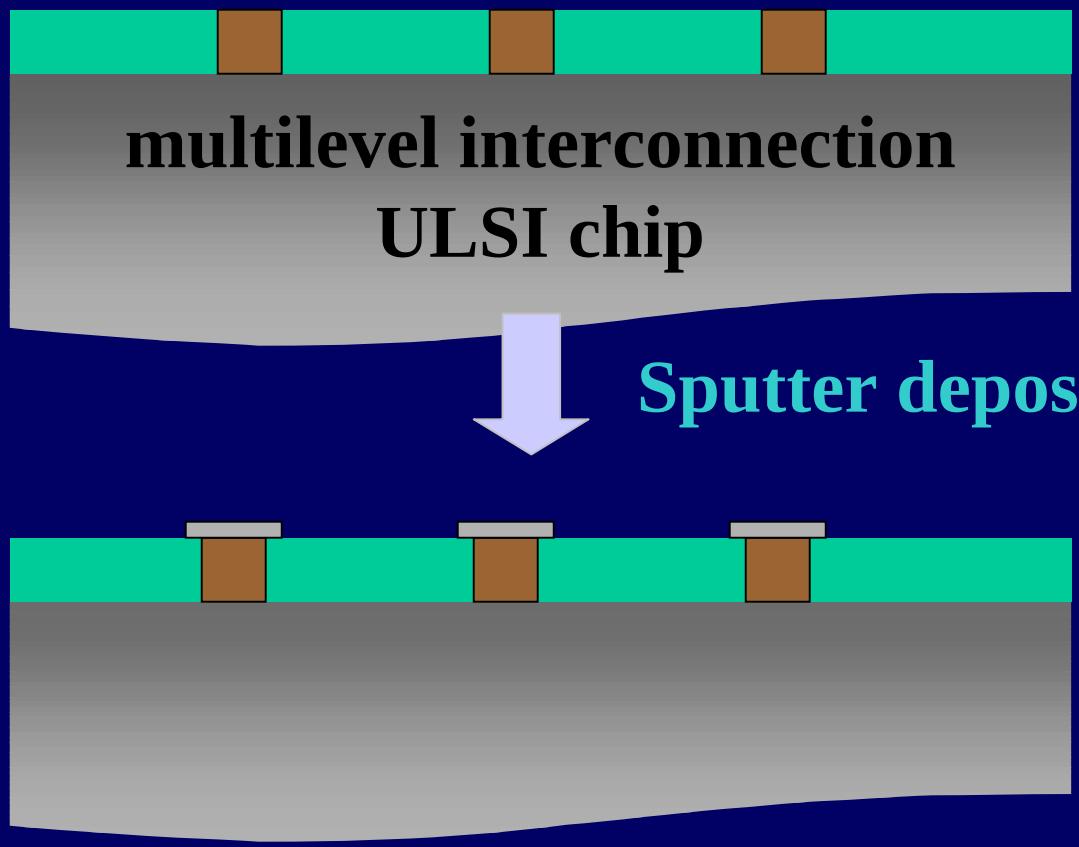
Test chip showing bumps completely covering surface of chip

Connections not limited by die perimeter

Wireless bonding: redistribution layer fabrication



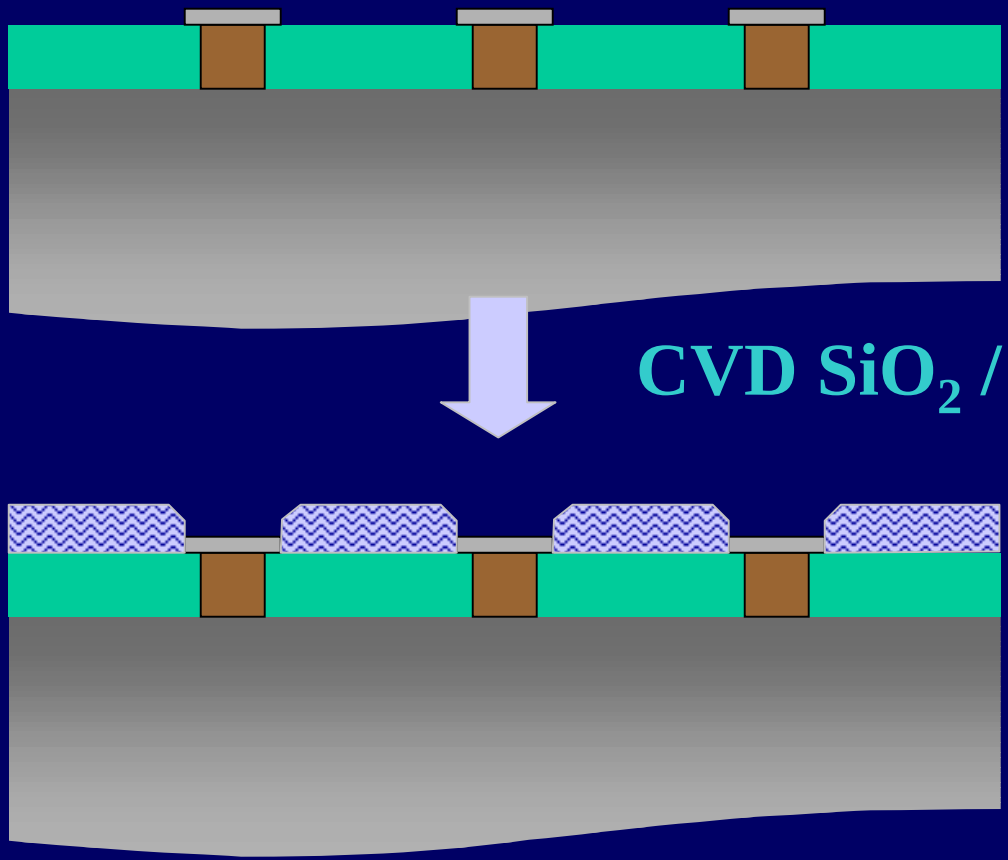
Wireless bonding: bonding pad fabrication



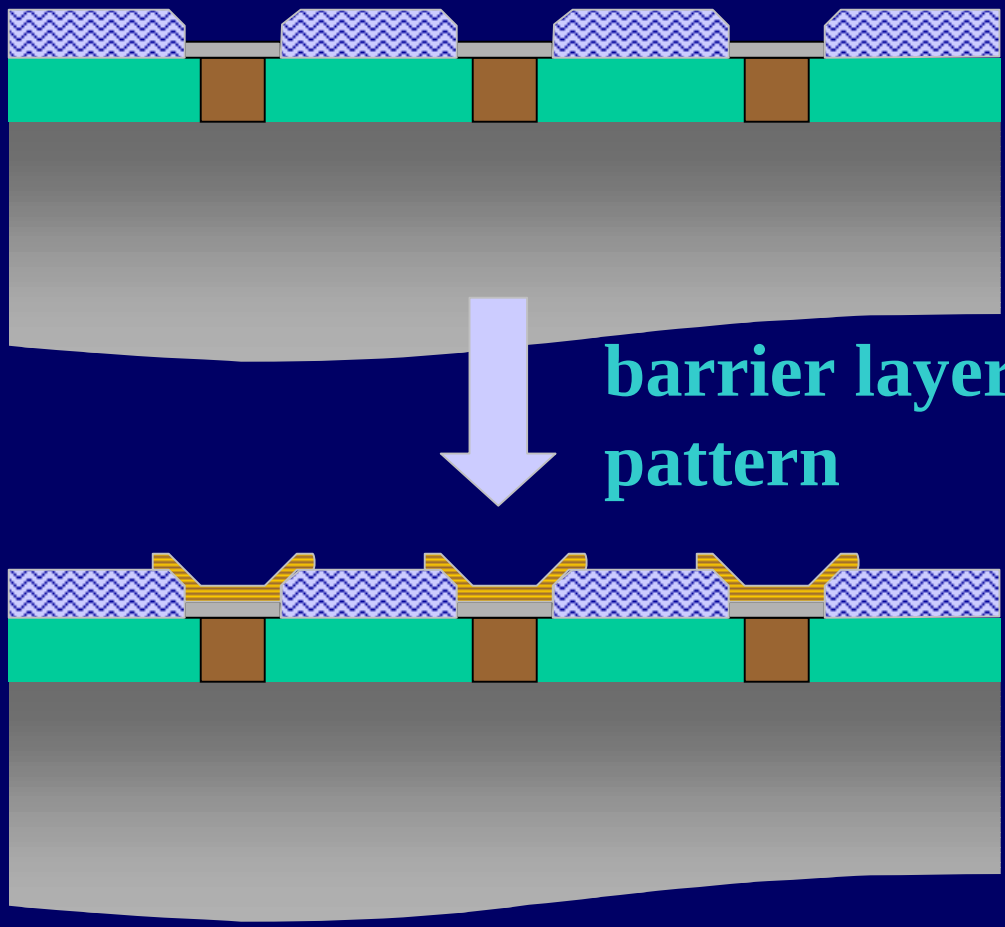
Redistribution layer with vias

Sputter deposit Al / pattern

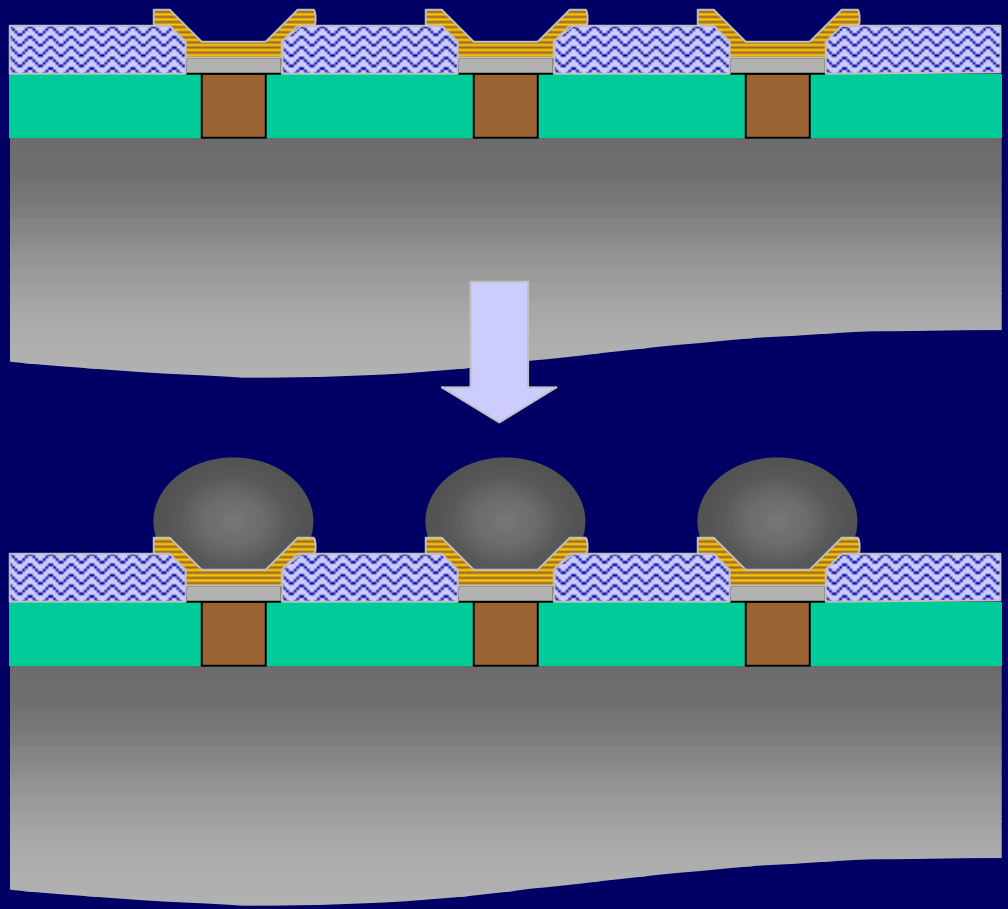
Wireless bonding: bump via fabrication



Wireless bonding: barrier layer fabrication

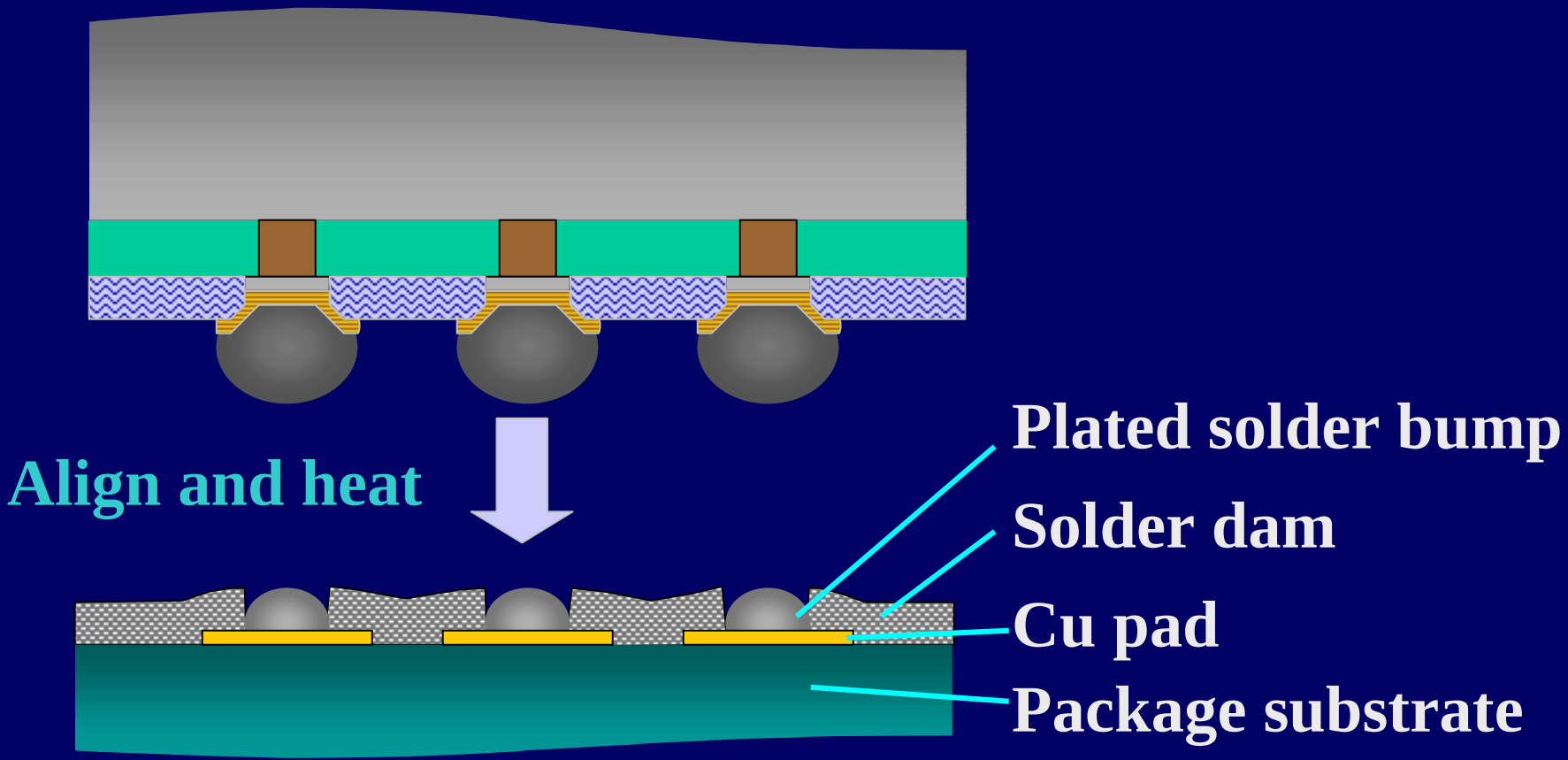


Wireless bonding: solder bump fabrication

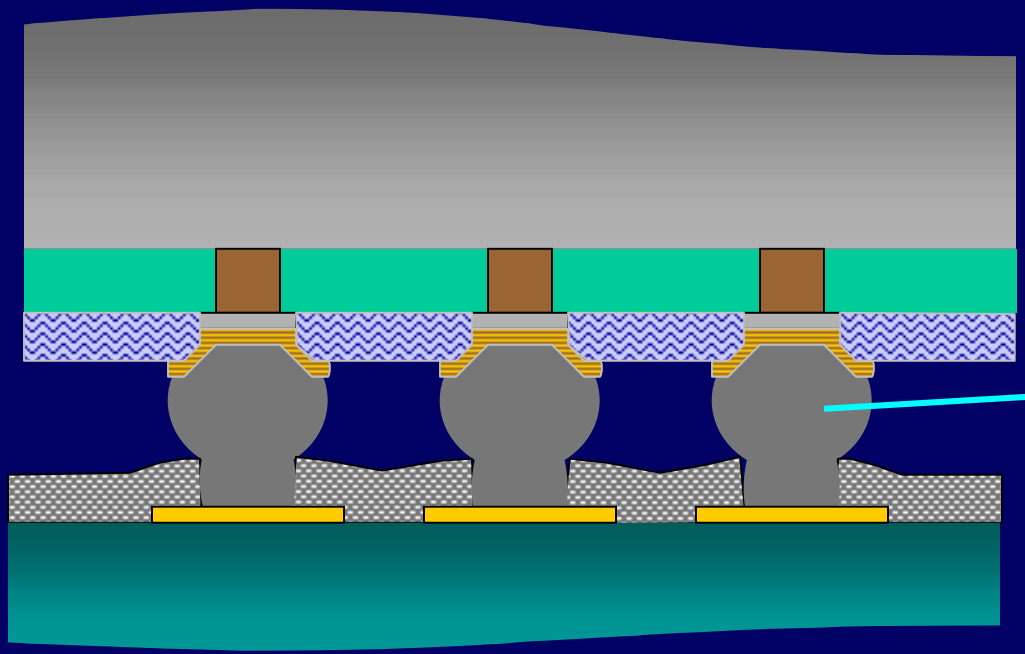


deposit solder through mask or plate

Wireless bonding: flip-chip bonding

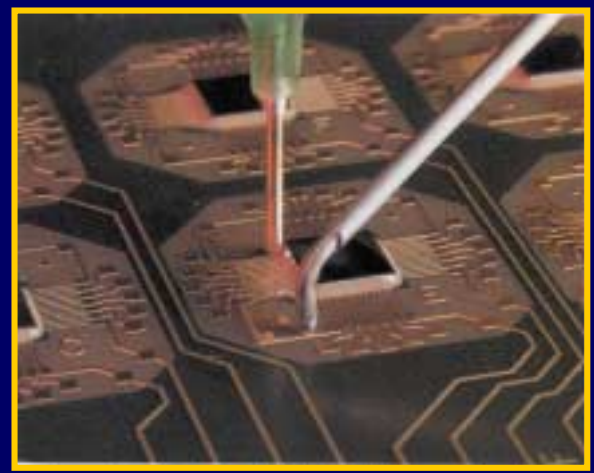


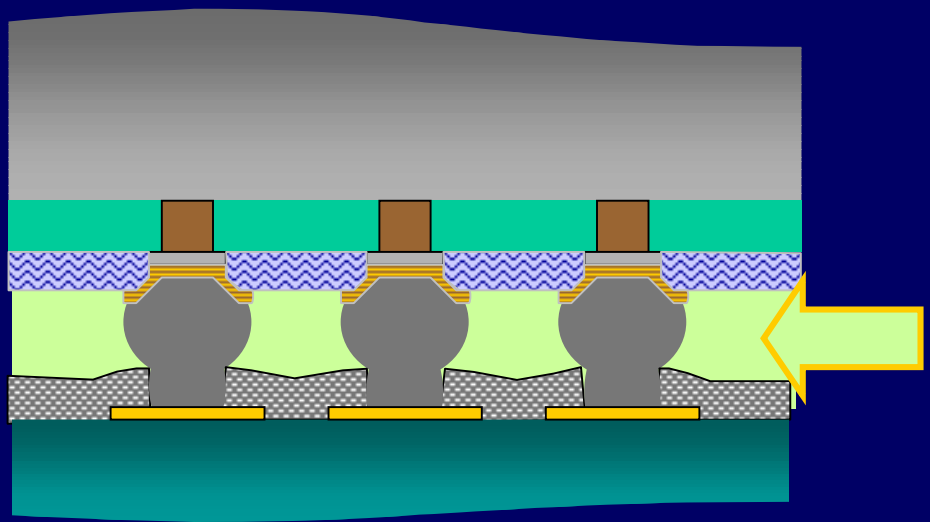
Wireless bonding: bonded package



Wireless bonding: underfill

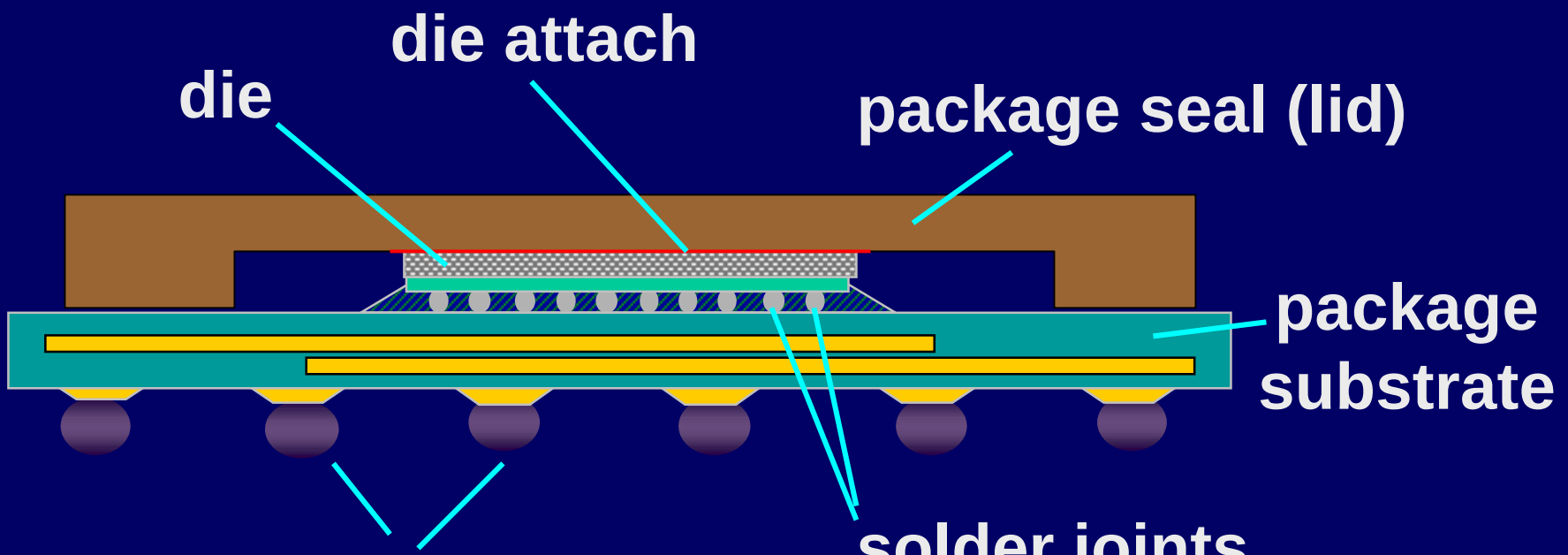
Purpose: **minimize induced stress**
enhance mechanical integrity
encapsulate



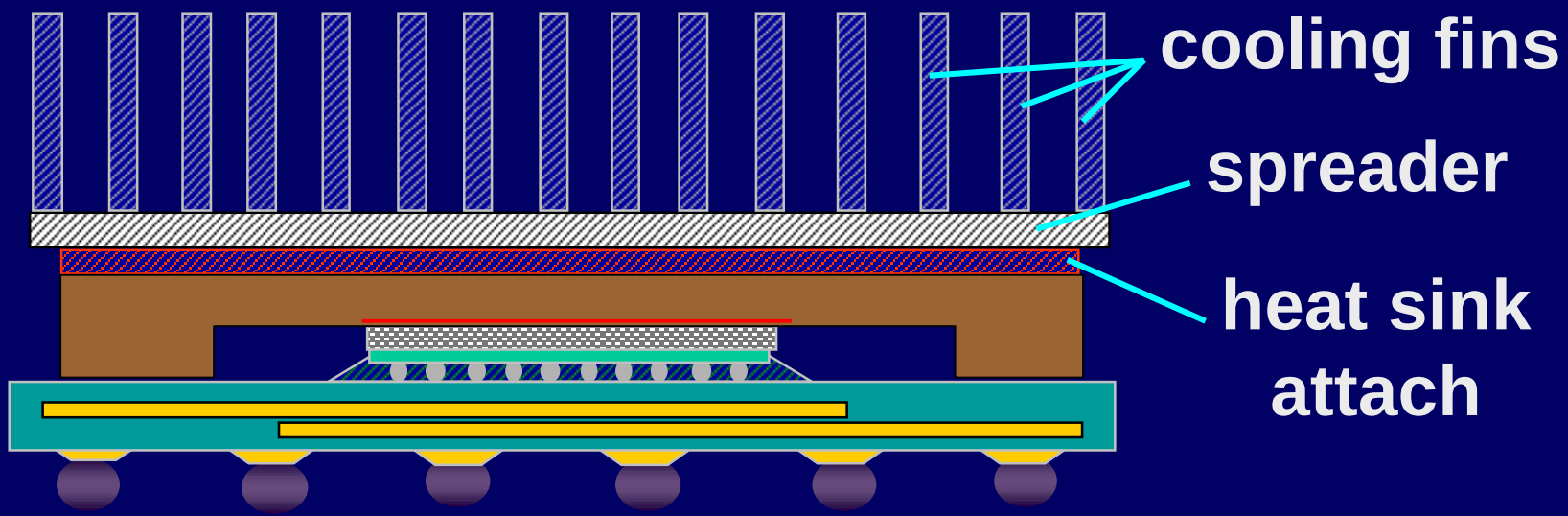


Self-filleting capillary flow
Liquid epoxy encapsulant

Package Cross Section



Package with Heat Sink Cross Section



“New” Packaging Process Directions

- **Wafer Scale Packaging (WSP)**
  - ✔ IC packaging performed on wafer
  - ✔ low-to-moderate I/O density applications
- **System-on-a-Chip (SOC) Packaging**
  - ✔ multiple chips in single package
  - ✔ multiple functions
    - » RF and mixed signal (incl. embedded passives)
    - » MEMS
    - » bio-chips

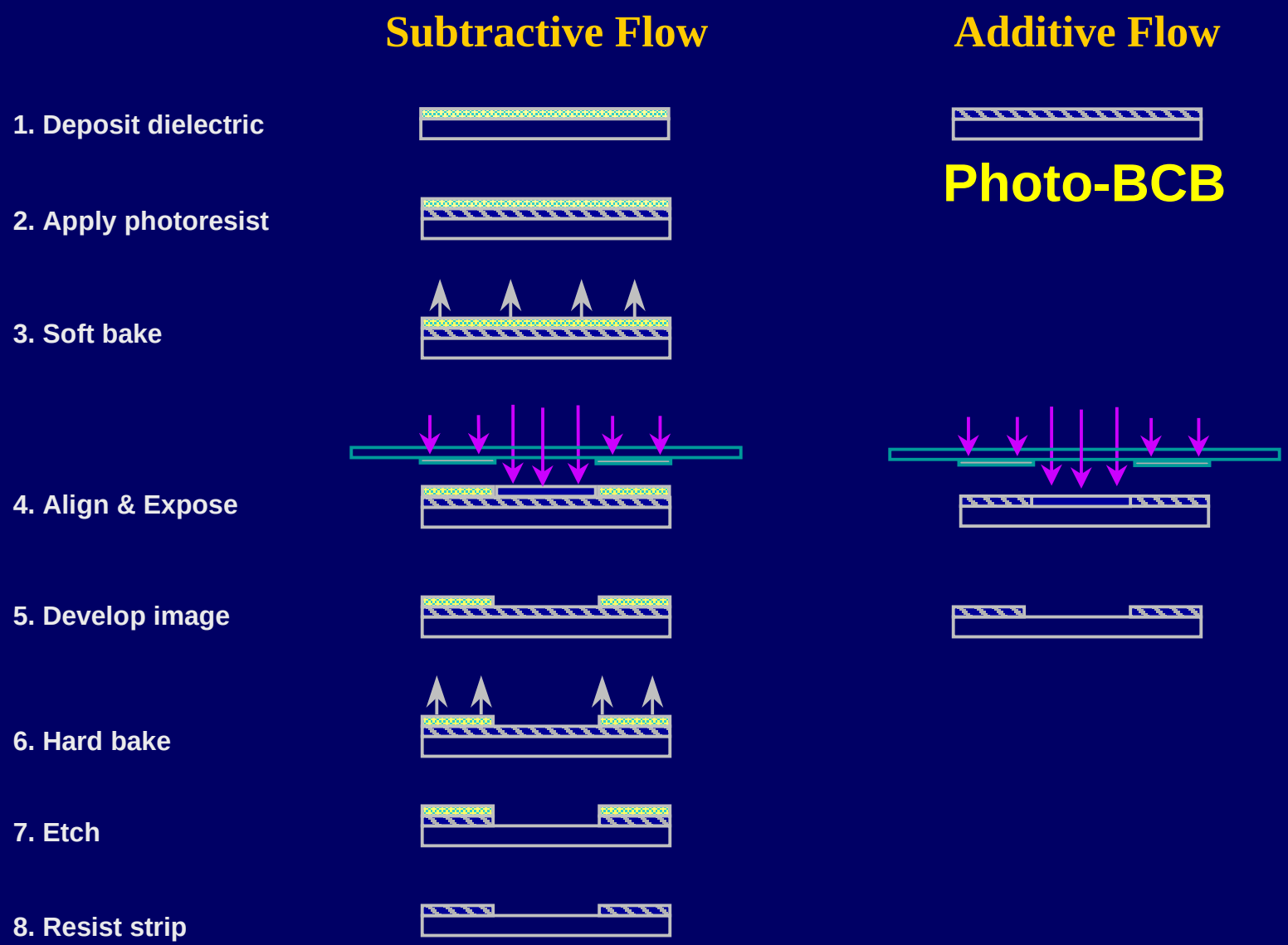
WSP Implications

- **Known-good-packages *vs.* known- good-die**
- **Economics of wafer-scale interconnect processing**
- **Blurring of the boundaries between chip manufacture and packaging**
  - **Cu / Ag ECD metallization**
  - **Barriers**
  - **CMP**

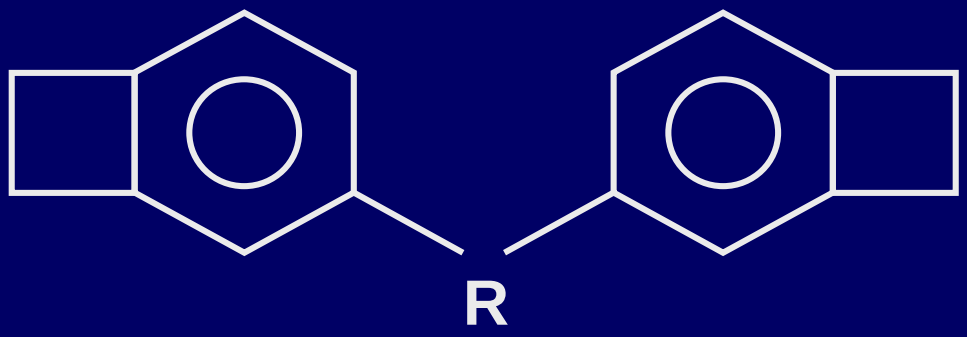
Principal ESH Issues

- **Pb-free solders**
- **Pb-free lead frames**
- **ECD baths (Cu, Ni, Au, Ag, Co)**
- **Flame retardants**
  - **Bromine-containing**
  - **Antimony trioxide**
- **Water use (plating)**
- **Energy use**
- **Heat sink attach materials**

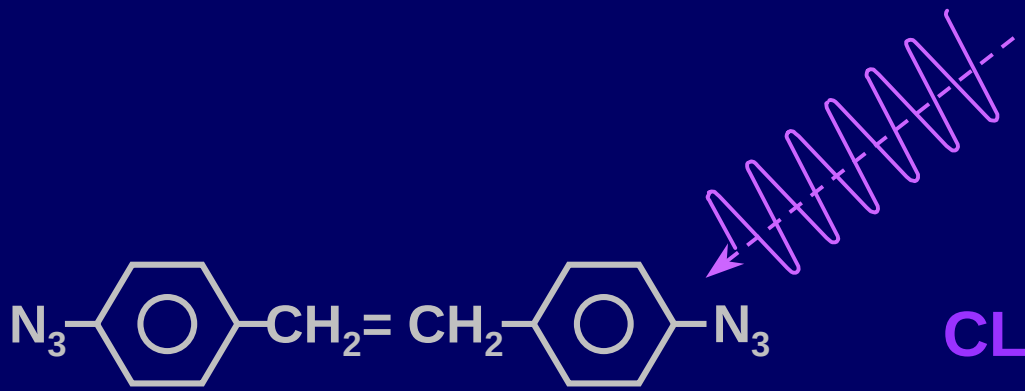
Wireless bonding: bump via fabrication



Photosensitive Benzocyclobutene

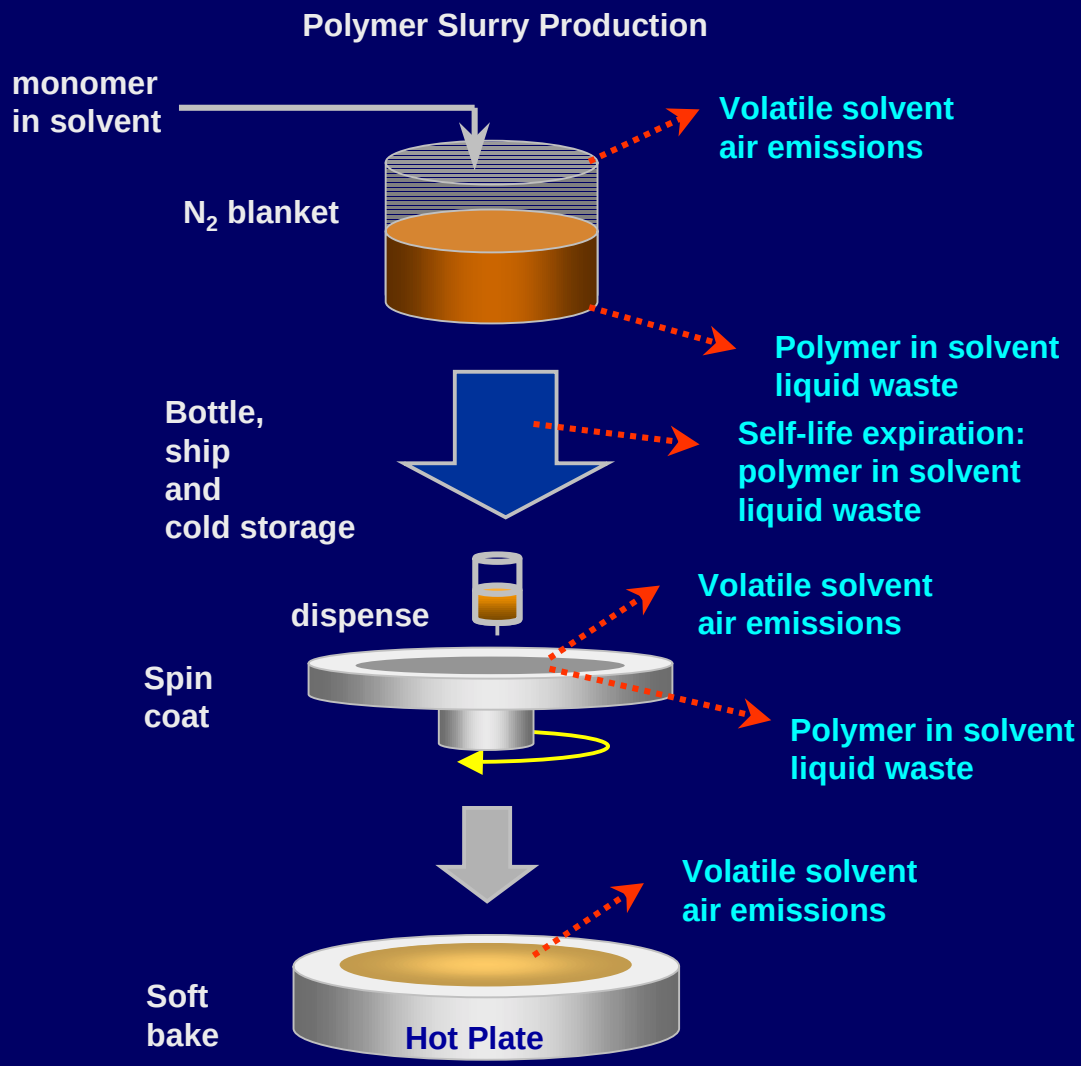


Single-step, low T cure
Moisture resistant
Thermal stability
Film retention
Low dielectric constant

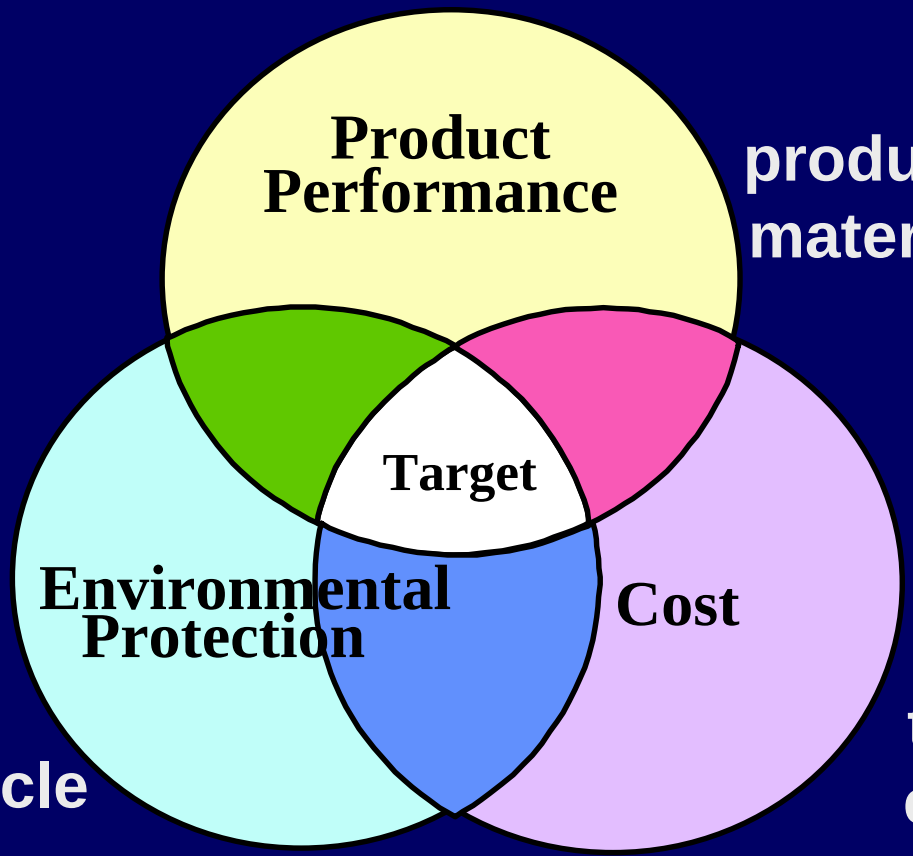


CLA photosensitizer

Spin Coat ESH Liabilities



Overlapping Performance Metrics

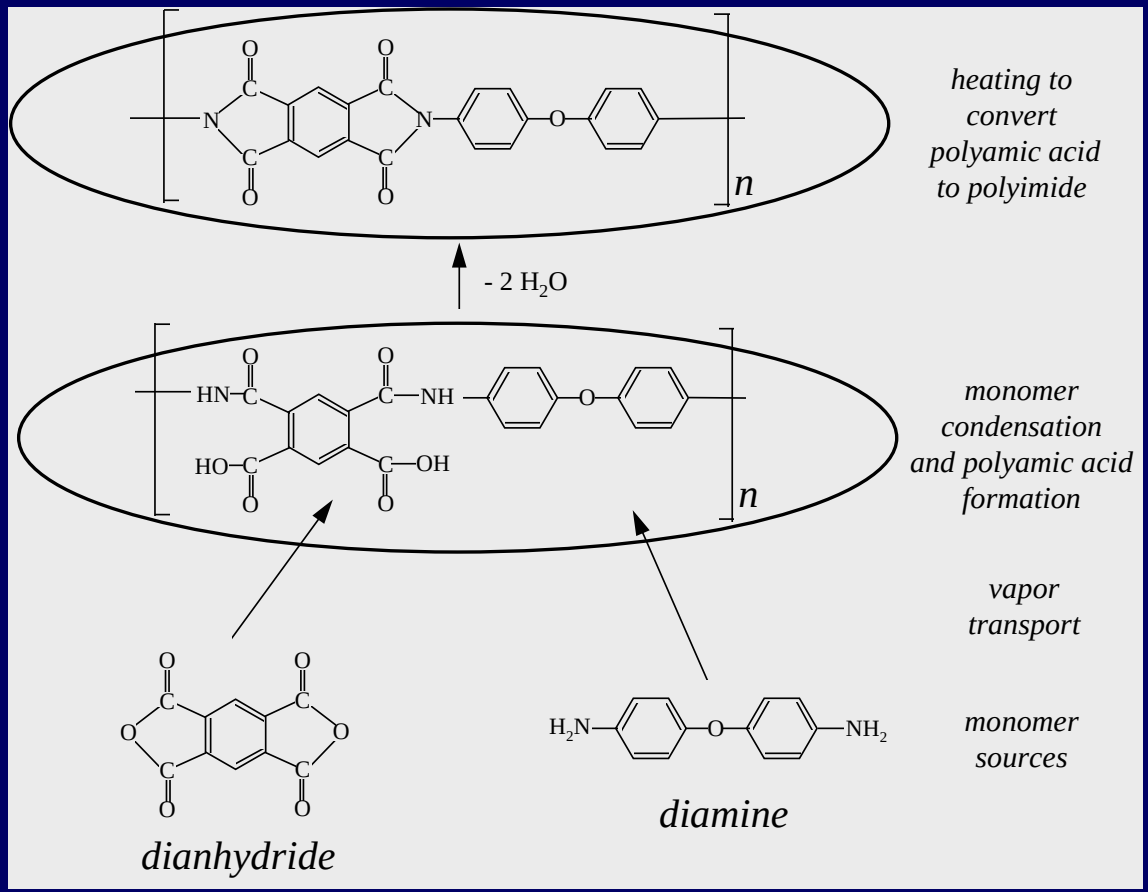


product architecture
materials properties

emissions
energy use
water use
product life-cycle

yield
scale-up
throughput
efficiencies

Autophotosensitive Photoimageable Polyimide Vapor Deposition



Environmentally Benign Pb-free Solders for Microelectronics Packaging Applications

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