Environmentally Benign Deposition of Photoresist and Low-k Dielectrics

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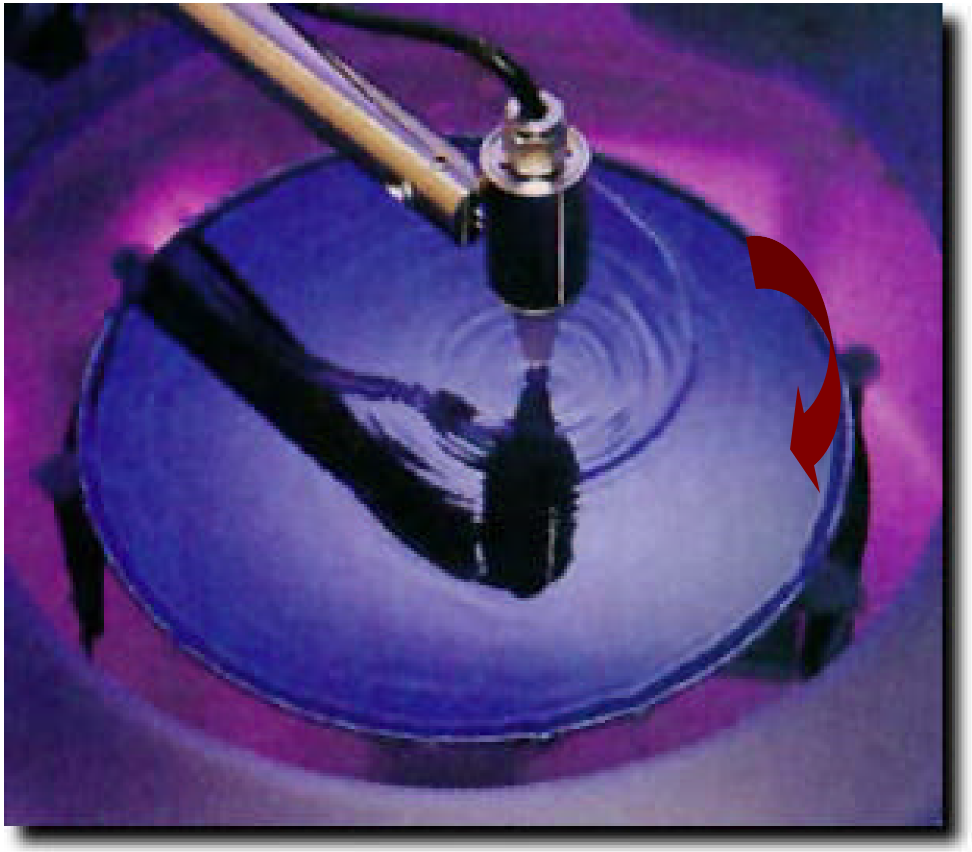
Outline

- Motivation
- Objective
- Approach
- FEM Analysis of the micro-machined ejector
- Previous 6-month research
  - Experimental setup
  - Ejection
- Problems
- New fabrication process
- Conclusions
- Future Research

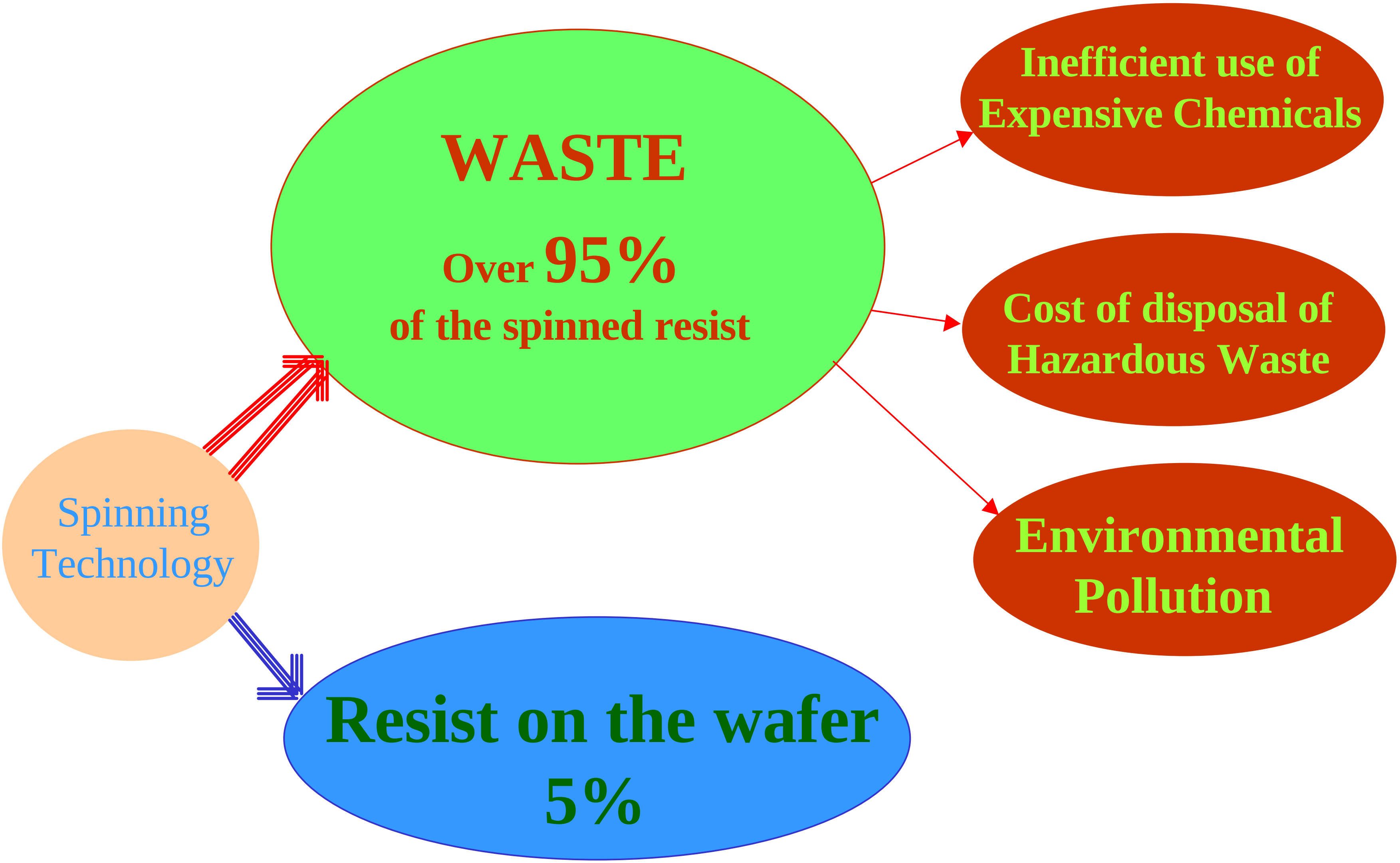
Motivation: Current Best Technology

- Current best coverage technology:

  Photoresist or Low-*k* dielectric wafer coverage by spinning



Motivation: Waste



WASTE

Over 95%

of the spinned resist

Inefficient use of Expensive Chemicals

Cost of disposal of Hazardous Waste

Environmental Pollution

Spinning Technology

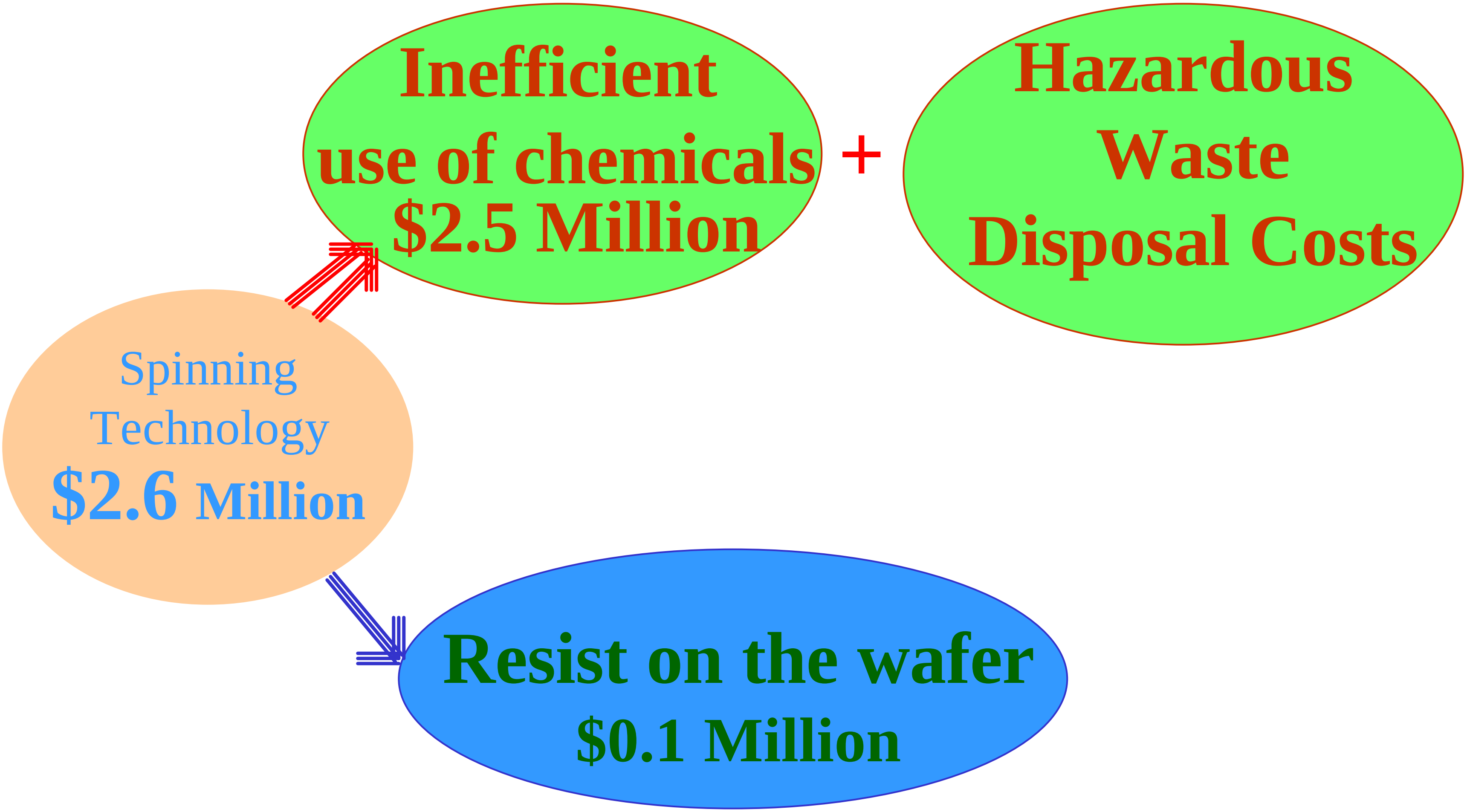
Resist on the wafer

5%

Motivation: Cost

- **DUV resist costs $5000 /gal**
- **Throughput per year for a four inch wafer track**

(60 wafers/hr) (360 days/year)(0.90 track utilization)=466,560 wafers/year



Inefficient use of chemicals $2.5 Million

+

Hazardous Waste Disposal Costs

Spinning Technology **$2.6 Million**

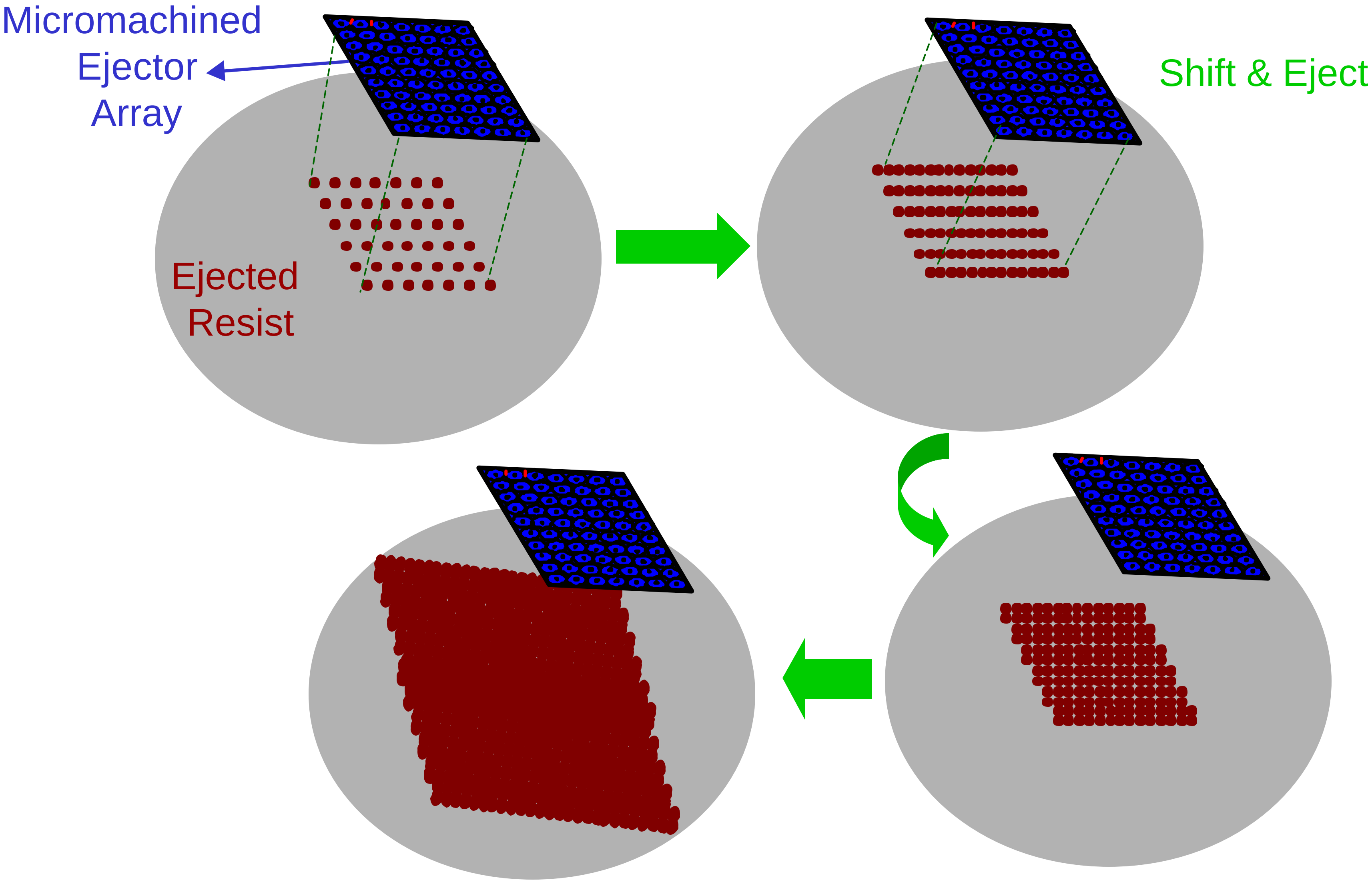
Resist on the wafer $0.1 Million

Objective

- Since a large amount of photoresist, low-*k* and high-*k* dielectrics is wasted during spin coating,

  our aim is to **reduce the waste**.
  - Develop a fluid ejection system capable of depositing fluids with a minimum of waste.
  - Develop a system capable of drop on demand and continuous ejection.
  - Develop a coating system to demonstrate waste reduction with full coverage of wafers.
  - Demonstrate photoresist and low-*k* and high-*k* dielectric coating of 20 cm and 30 cm silicon wafers.

Approach: Full Device



Micromachined Ejector Array

Ejected Resist

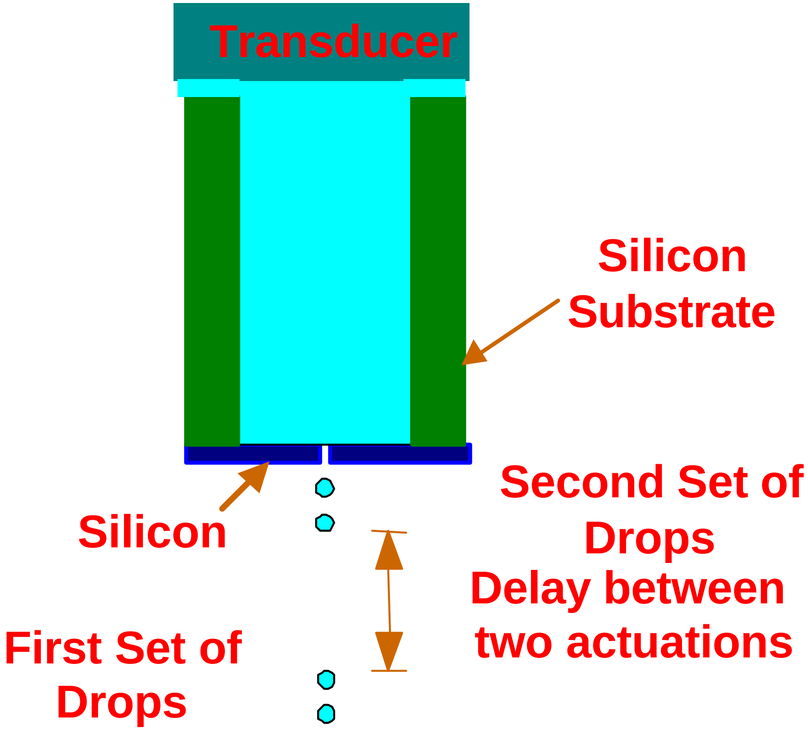
Shift & Eject

Approach: Design Requirements

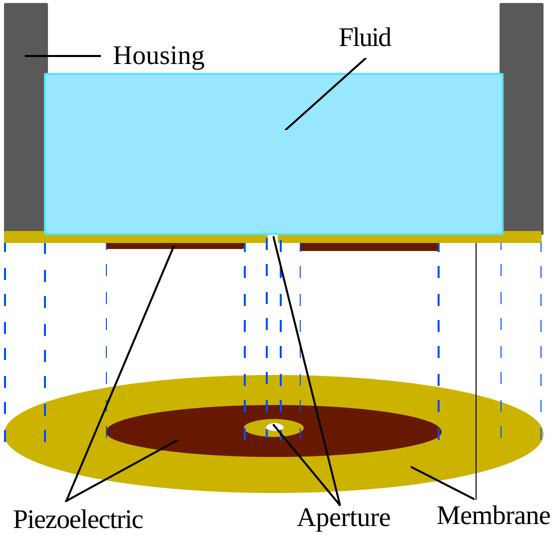
- Use flex-tensional ejectors for deposition
  - Design and implement micro-machined ejector arrays with either single or multiple piezoelectric drivers
- Ejector requirements
  - Able to deposit low and high viscosity fluids
  - No damage caused to the ejected fluids
  - High flow rate
  - Compatible with most chemicals
  - Can be made using IC process technology

Approach: A Unit Cell of the Device

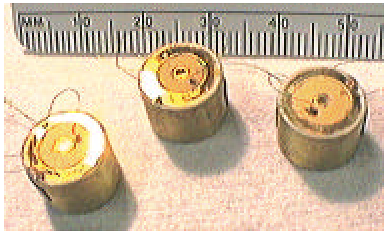
- Flex-tensional ejectors for deposition
  - Design and implement micro-machined ejector arrays with either single or multiple piezoelectric drivers



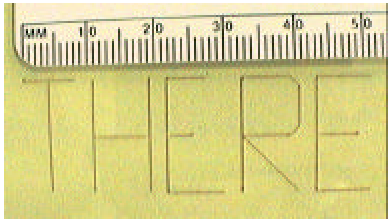
Large Scale Single Ejector



Side view



Front view



Membrane : brass, steel

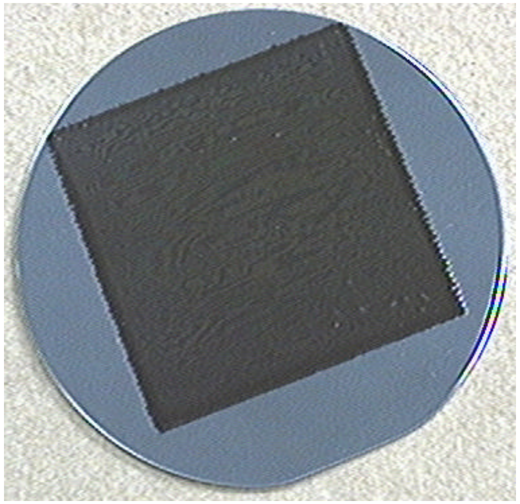
Diameter : 9 mm

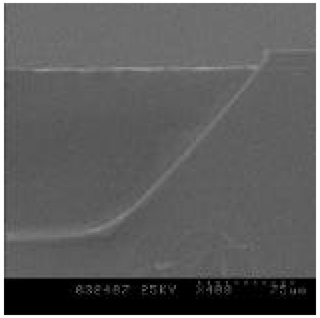
Membrane thickness : 25 µm

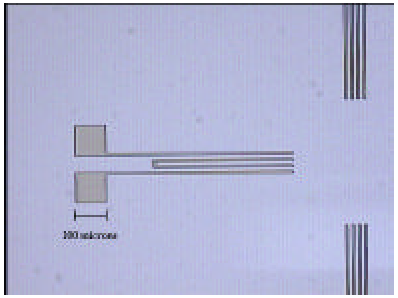
Orifice size : 50-200 µm

Operating frequencies:

9.5 kHz, 16.4 kHz, 19.0 kHz





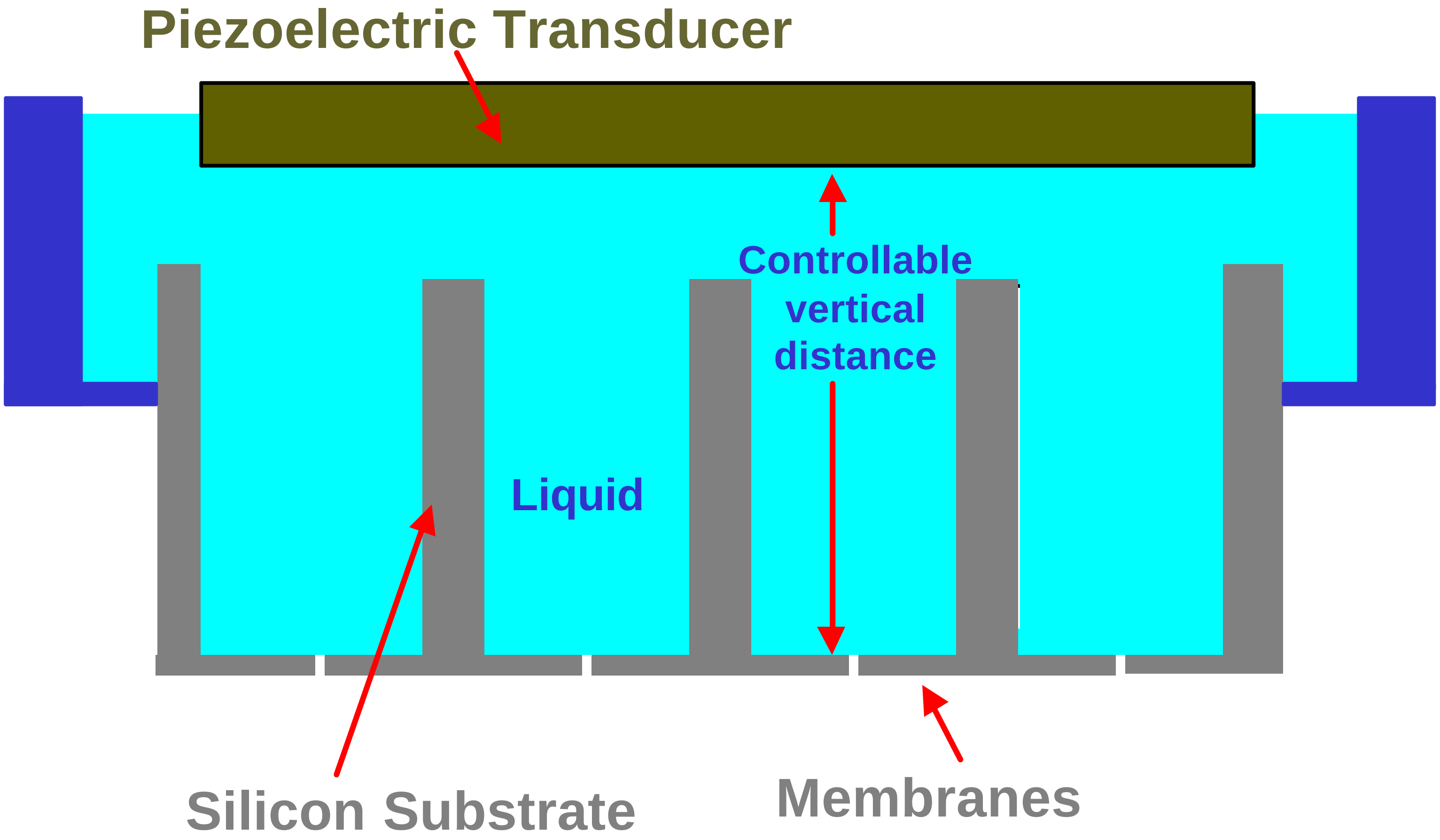


- Photoresist covered deep trench
- Deposited Photoresist Thickness :

  3.5 µm ± 0.15 µm
- Direct write with resist:

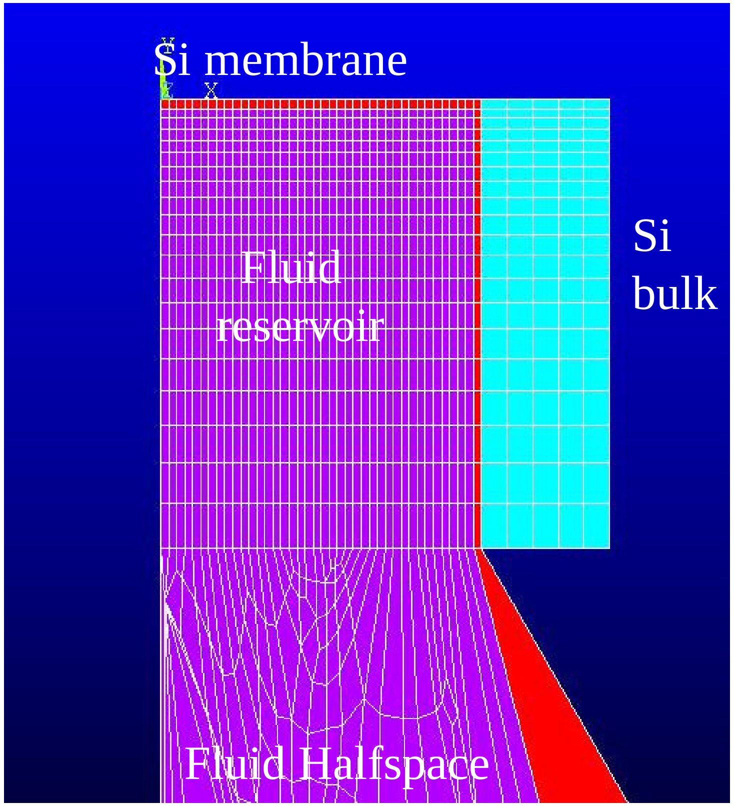
  350 µm-wide lines

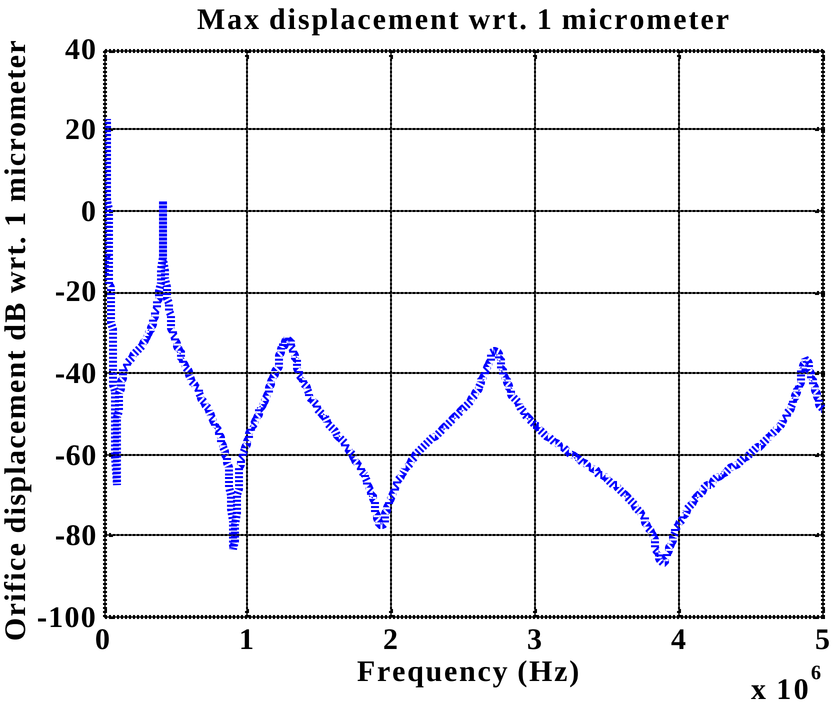
Micromachined Device Configuration



Finite Element Modeling of Ejector

FEM modeling of a Silicon membrane that is 1 µm thick and 100 µm in diameter. Membrane and cavity resonance govern operation at resonance for ejection.





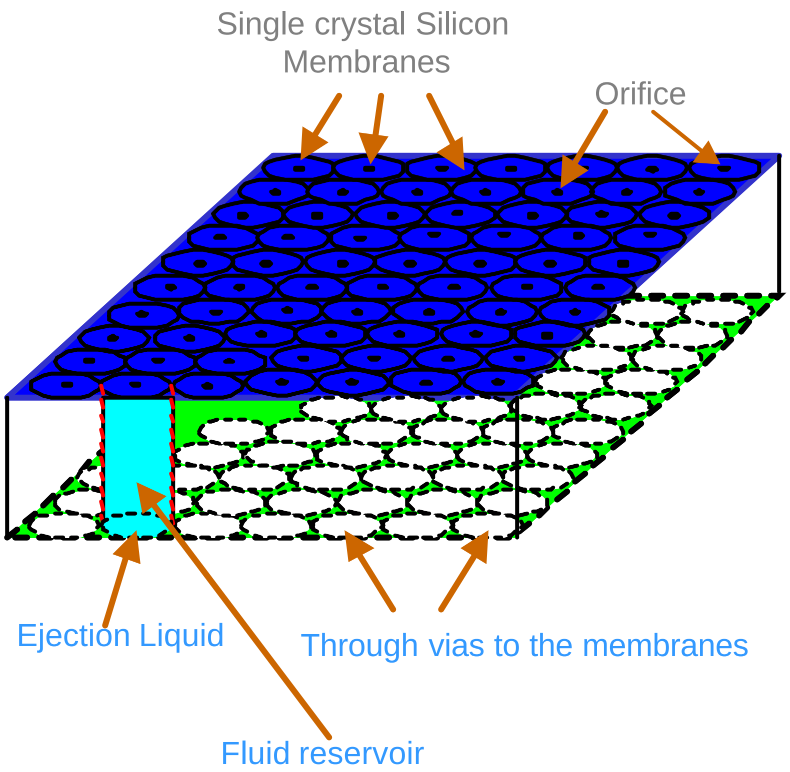
FEM: Membrane Diameter vs. Frequency

Resonance Number

Membrane diameter	0	1	2	3	4
200 µm	382 kHz	1.49 MHz	3.34 MHz	5.91 MHz	
	78 kHz	480 kHz	1.33 MHz	2.72 MHz	
500 µm	61.26 kHz	238.3 kHz	533.5 kHz	946.9 kHz	1.479 MHz
	11.4 kHz	66.4 kHz	187.6 kHz	388.1 kHz	677.1 kHz

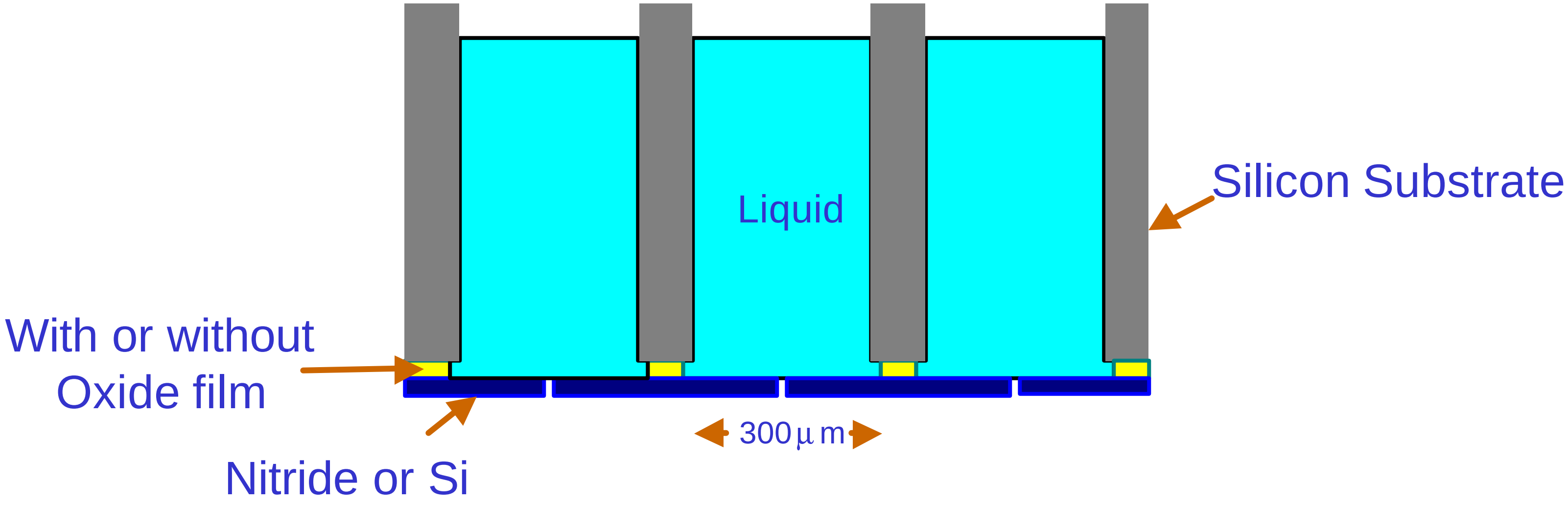
Vacuum
Water

2D Micro-machined Ejector Array



- 2D array of ejectors
- Membrane actuation by a transducer through the fluid reservoir
- Thin single crystal silicon uniform membrane
- Deep reactive ion etched reservoir
- High frequency operation for high flow rate (MHz)
- Drop-on-demand and continuous modes of operation

2D Micro-machined Array: Dimensions



Device Properties

Membrane material : Single crystal silicon, Si_3N_4

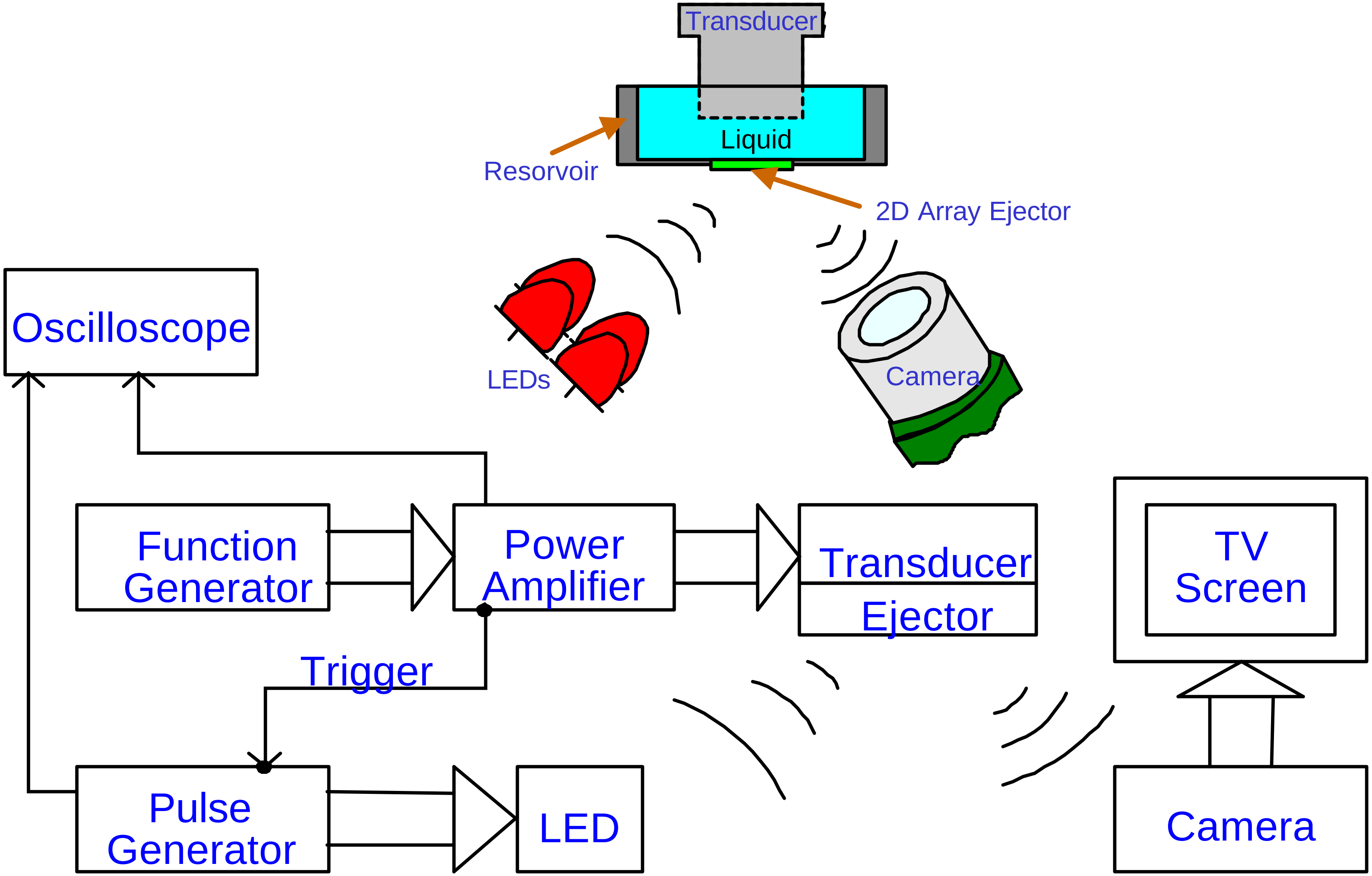
Membrane Diameter : 100 µm, 200 µm, 300 µm, 500µm, 1 mm

Membrane thickness : 1 µm for Si, 2.1 µm for Si_3N_4

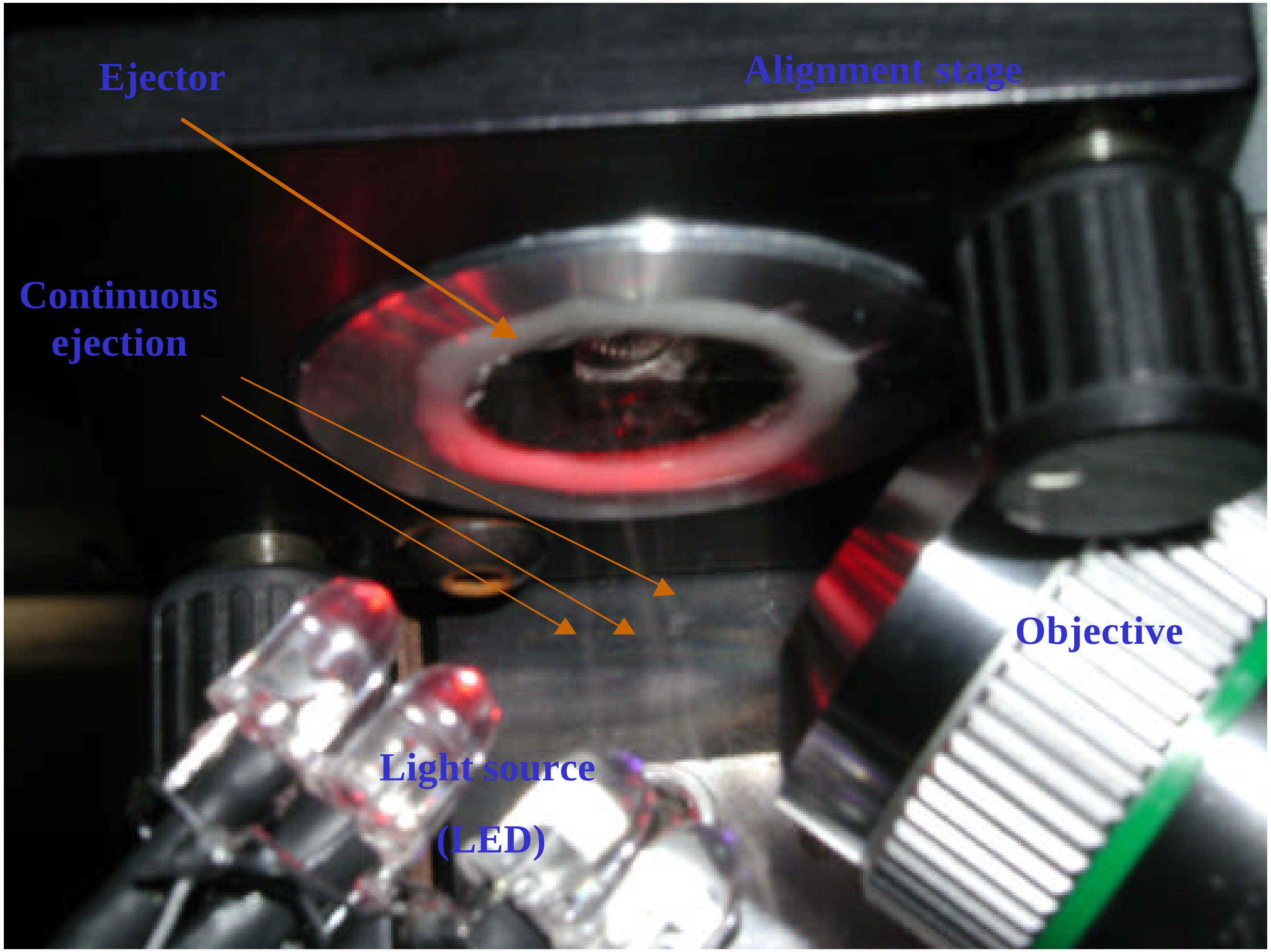
Orifice diameter : 4 µm, 10 µm, 14 µm

Operating frequencies: 470 kHz, 1.24 MHz, 2.26 MHz for Si_3N_4

Experimental Setup

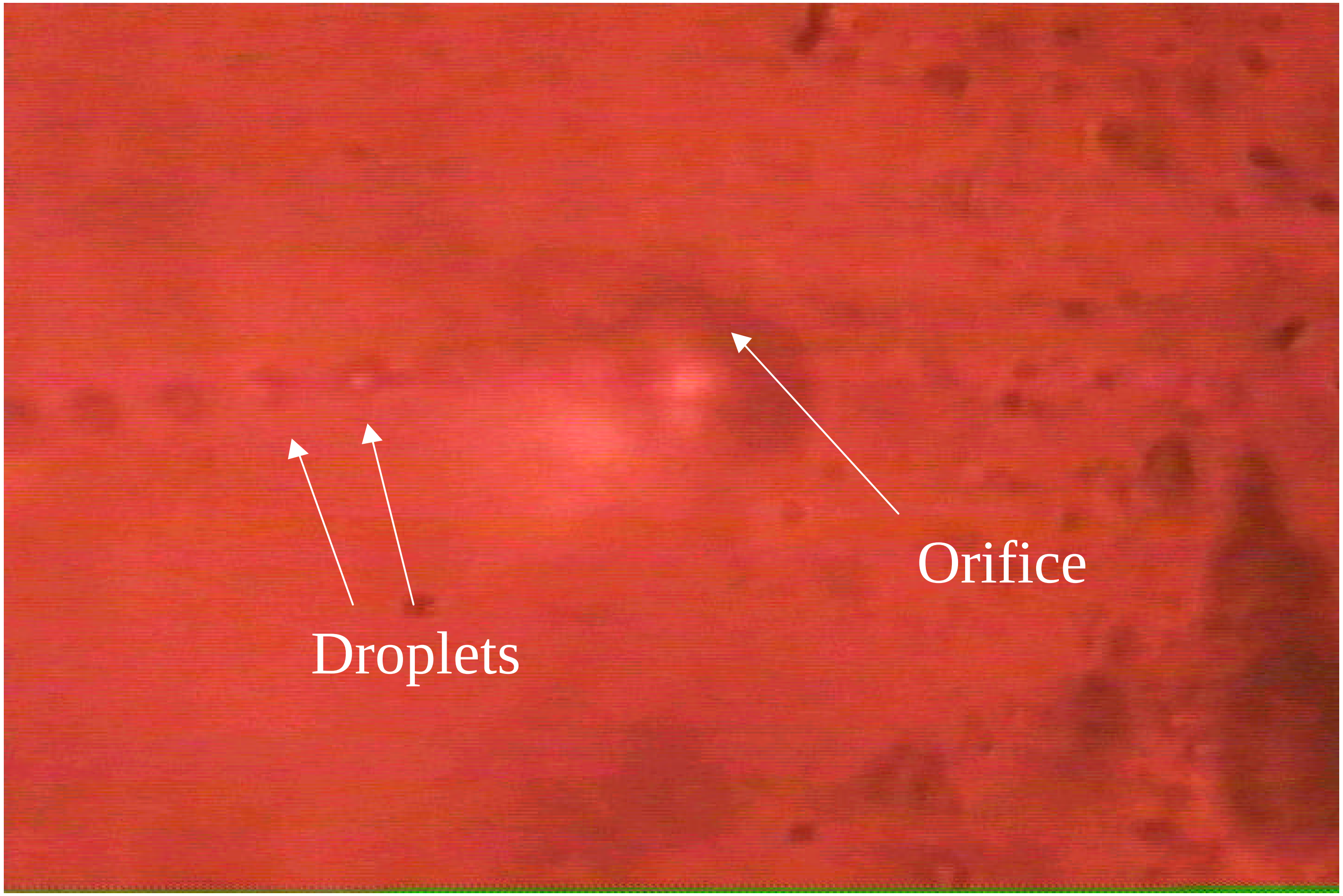


Experimental Setup: Ejecting Device



- Ejection is difficult to see due to very small droplets

1. 24 MHz Droplet Ejection

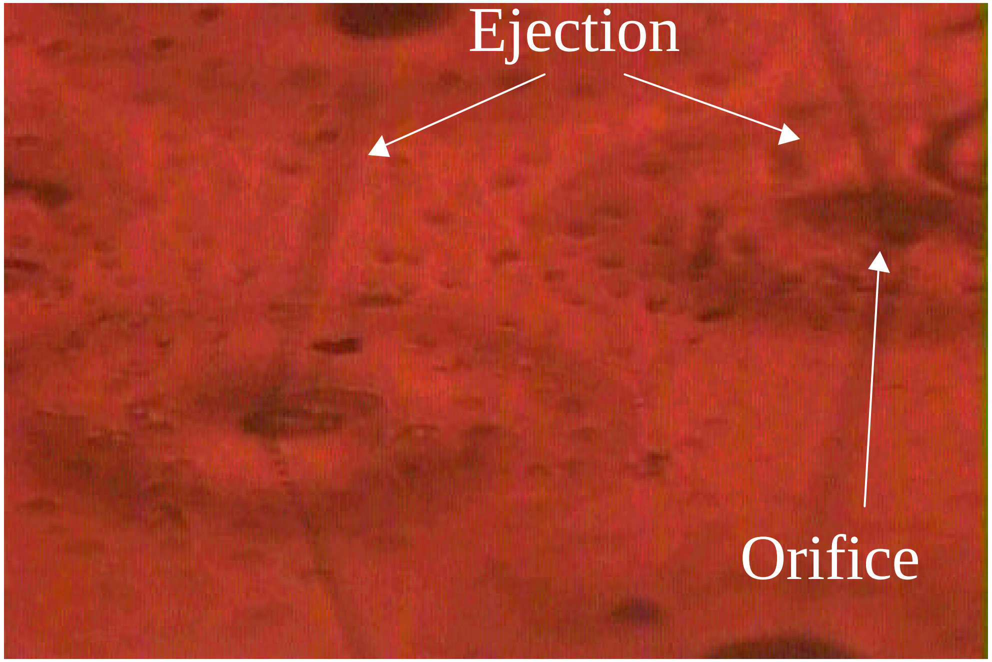


Water Ejection at 1.24 MHz
(5 mm in diameter droplets)

Ejection Summary

	470 KHz	1.24 MHz	2.26 MHz
Droplet Diameter	6.5 um	5 um	3.5 um
Center to Center Distance	14.8 um	14.1 um	9.2 um
Droplet Speed	6.9 m/sec	17.5 m/sec	20.8 m/sec

Two Membrane Ejection at 1.24 MHz

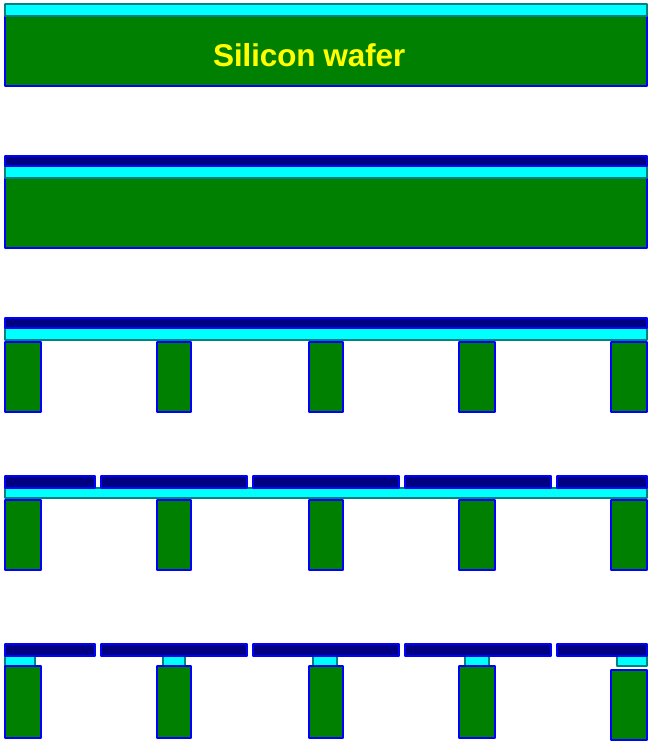


Two neighboring membranes ejecting simultaneously

- Observed 20 ejecting membranes out of 400

Fabrication Process: SOI Wafer Bonding

Previous



Oxide film deposition

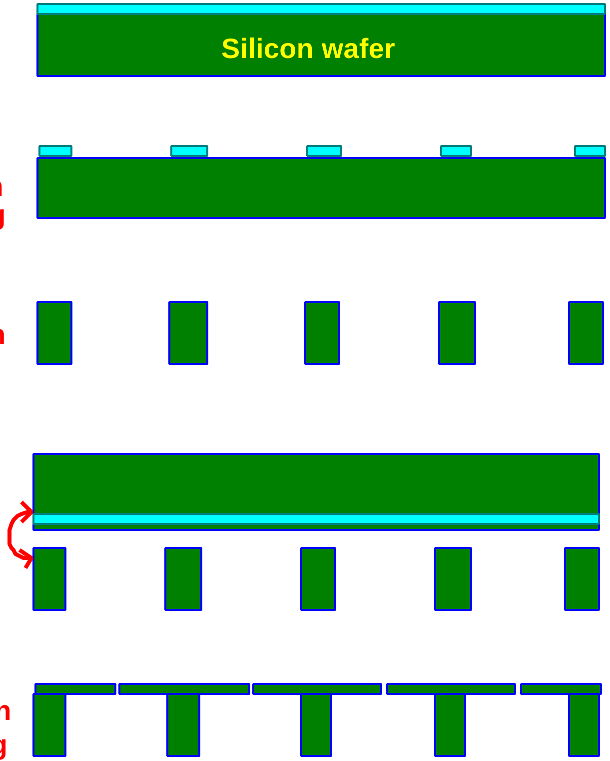
Nitride film deposition

Silicon bulk etch

Orifice formation with dry etching

Oxide etching

New



Oxide film deposition

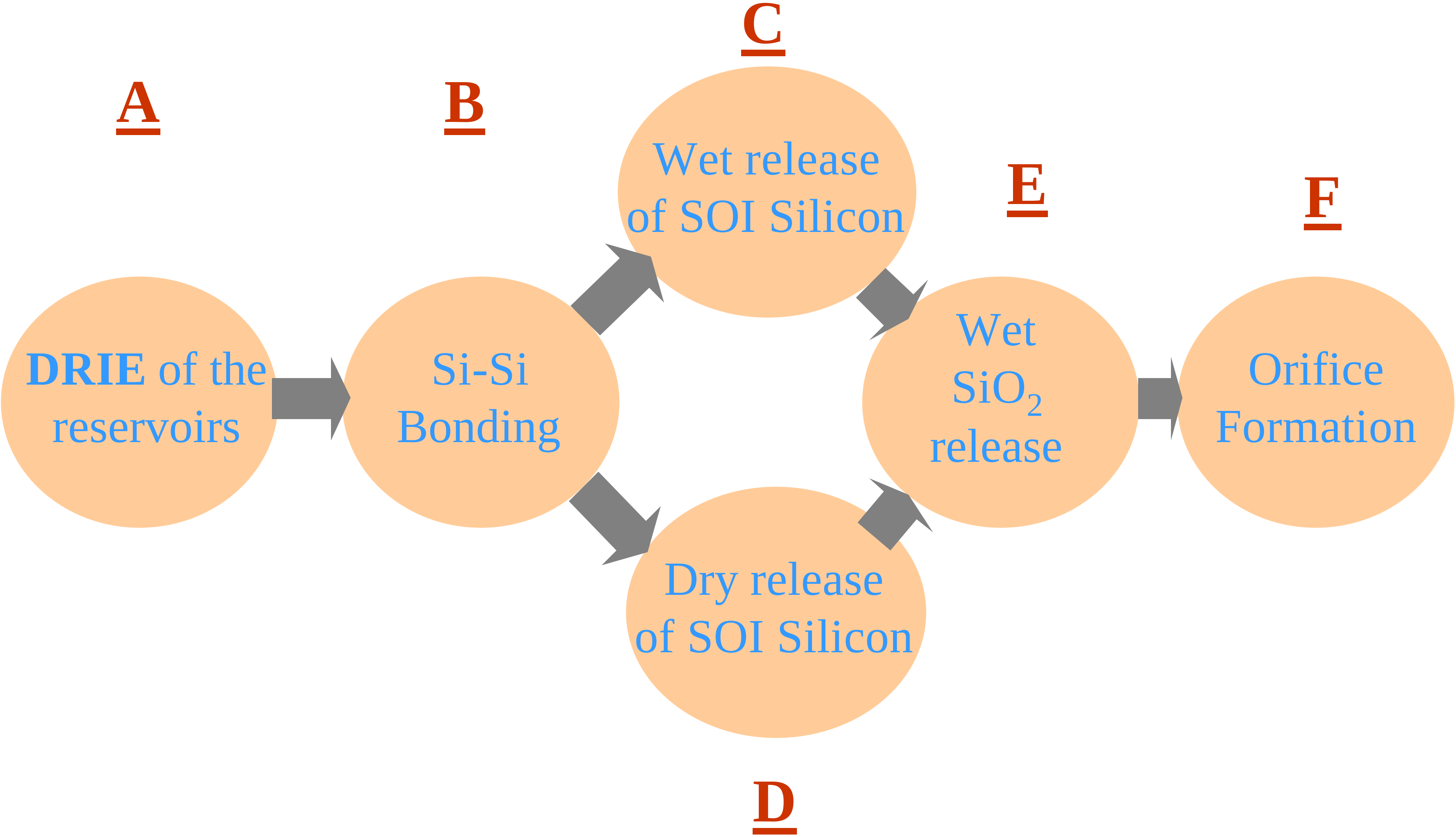
Oxide film patterning

Silicon bulk etch
Oxide removal

SOI wafer bonding

Wet Oxide etch
Orifice formation with dry etching

New Process Flow: Key Step Analysis



A

DRIE of the reservoirs

B

Si-Si Bonding

C

Wet release of SOI Silicon

D

Dry release of SOI Silicon

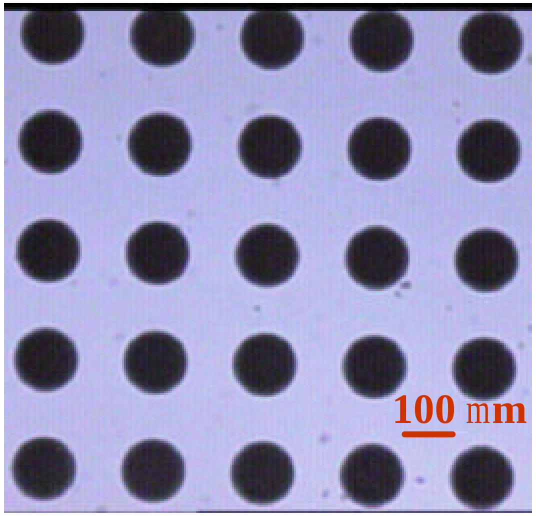
E

Wet SiO_2 release

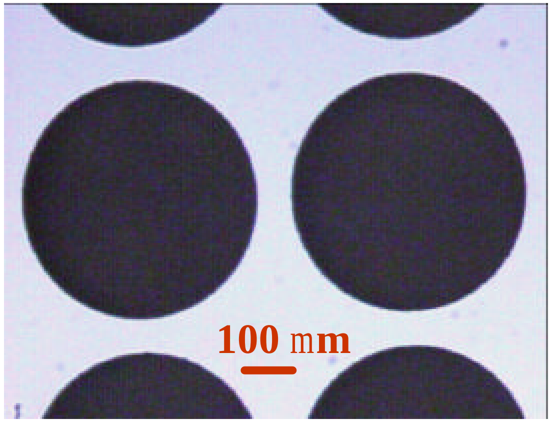
F

Orifice Formation

A) DRIE of the Reservoirs



100 mm wide etched holes in silicon wafer.



500 mm wide etched holes in silicon wafer.

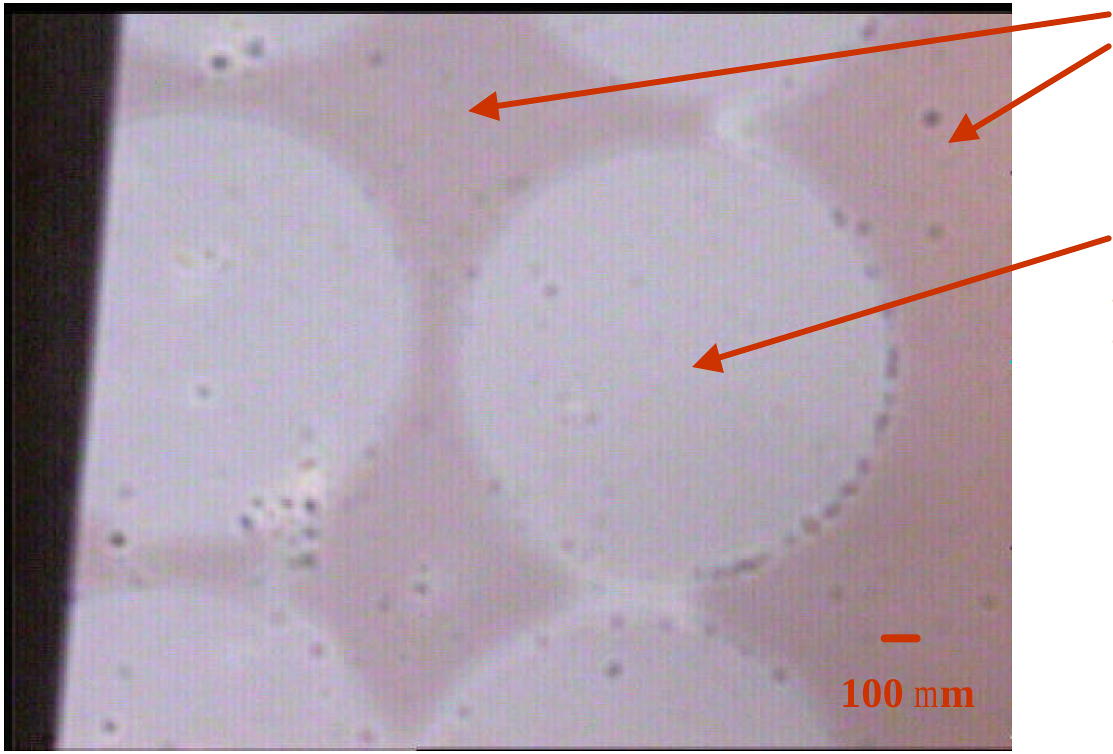
Device

5x5 STS etched silicon wafer ready to be bonded to a SOI wafer for membrane formation.

Benefits

- •Uniform 1 µm thick single crystal silicon membrane.
- •Membrane radius does not depend on the wet oxide etch rate.
- •Uniform membrane radius with Deep Reactive Ion Etching (DRIE).
- •Uniform membrane orifice with dry etching.

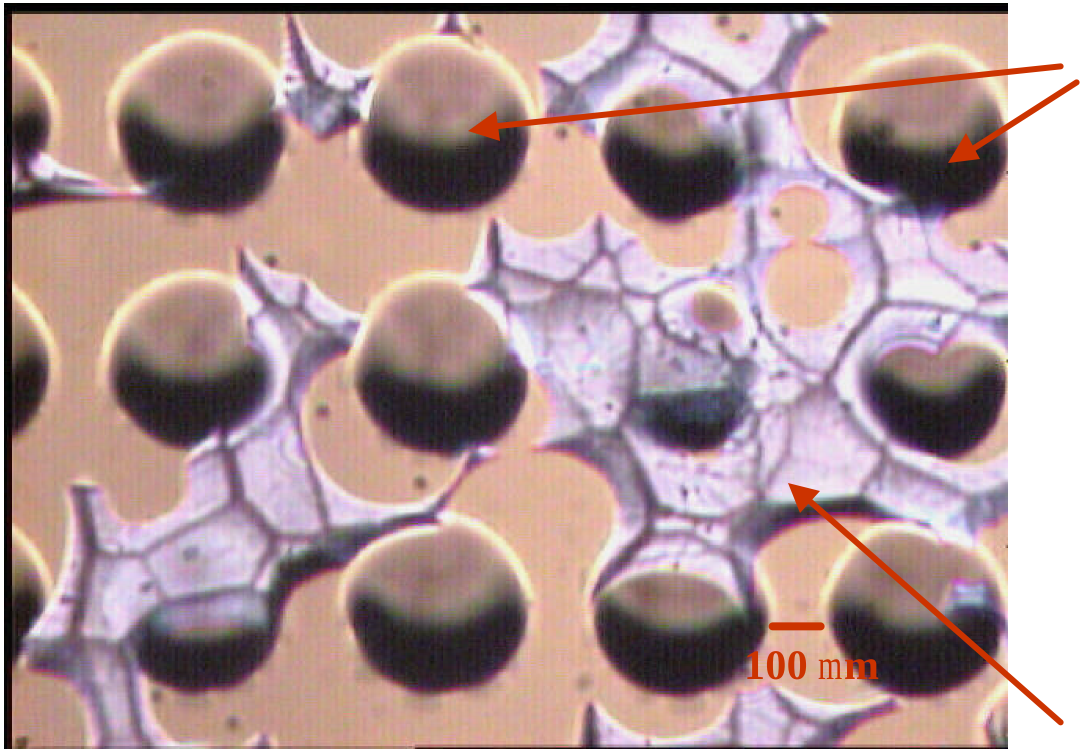
B) The Bonding Quality Test:
Si to Si Bonding



SOI SiO2 .

Single Crystal Silicon protected under a thin 800 Angstrom thick dry oxide layer.

C) Wet Membrane Release: Micro bubble masking



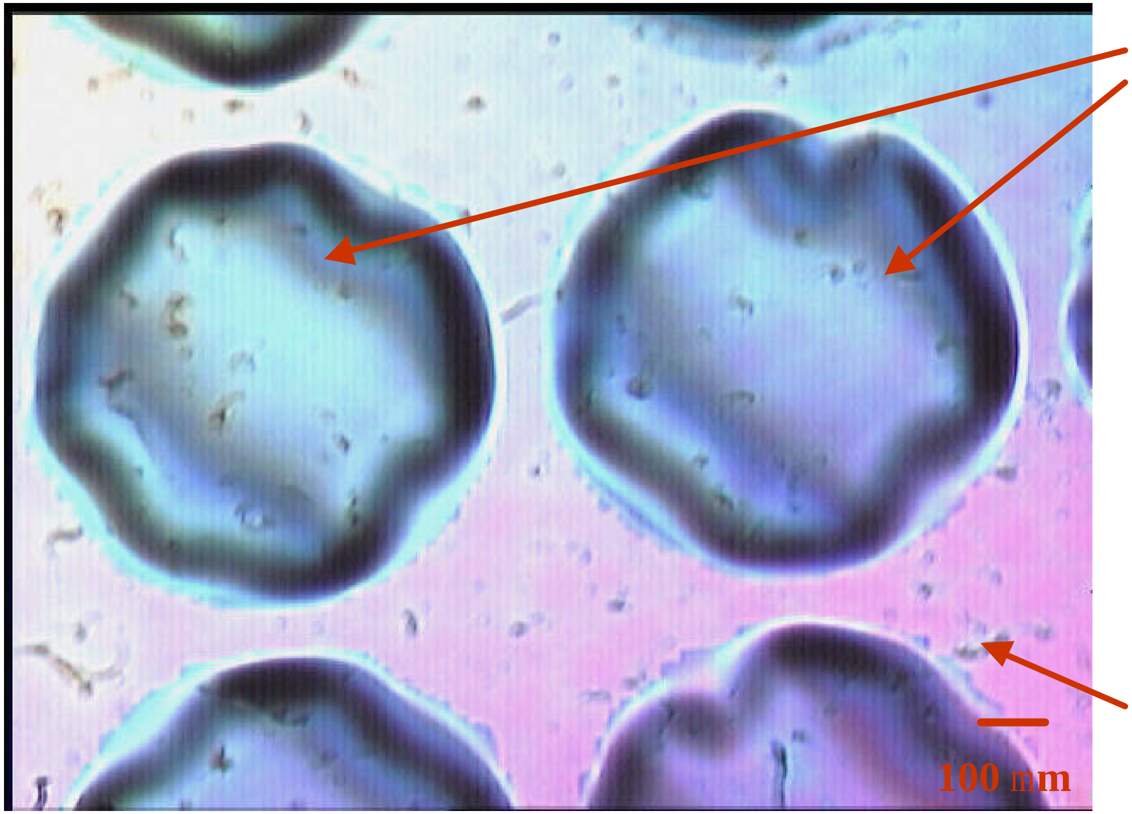
- Single Crystal Silicon membranes covered with SOI SiO_2 as wet etch stop.

- The ripples on the membranes are due to SiO_2 stress.

- SOI wafer silicon is etched to release the single crystal Silicon membranes.

Single Crystal Si Membrane Release with wet-etch is halted before the etch is totally finished.
Very good selectivity for Si vs. SiO_2 .

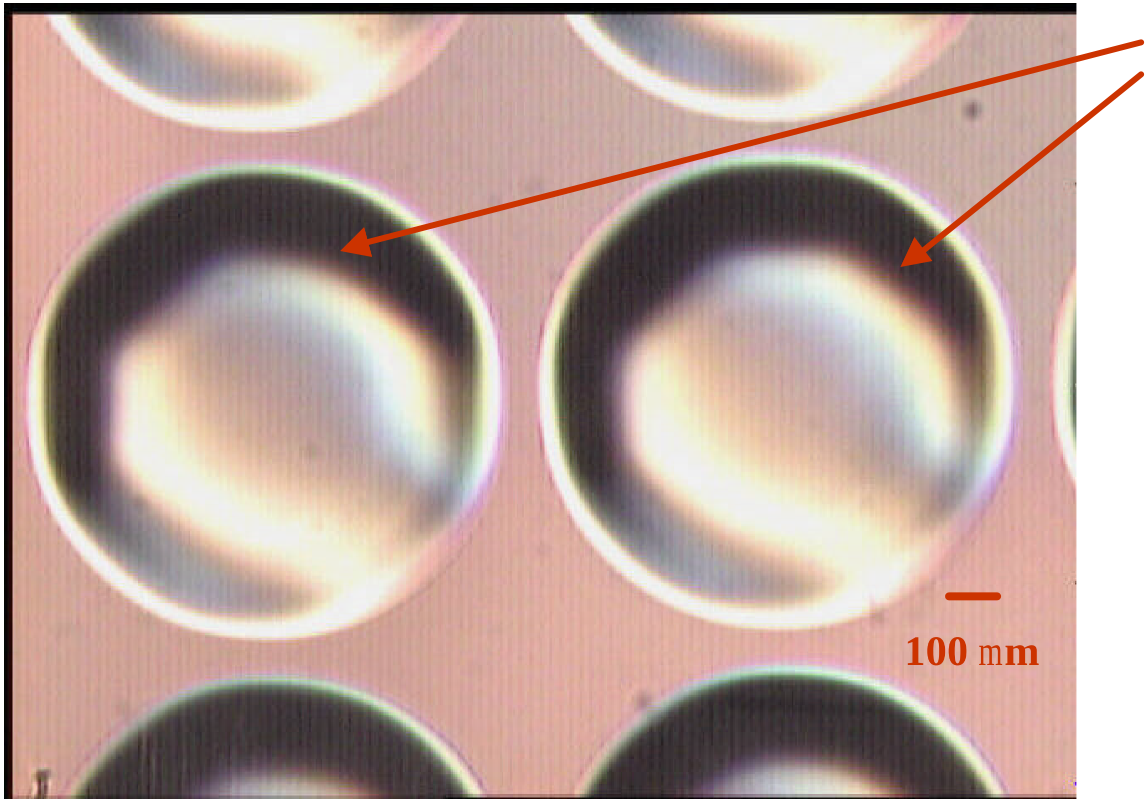
D) Dry Membrane Release:
Polymer residue



- Single Crystal Silicon membranes covered with SOI SiO_2 as a wet etch stop.
- The ripples on the membranes are due to SiO_2 stress.
- Polymer residues remain on the SiO_2 . They can be removed.

Single crystal Si membrane release with dry-etch is non-uniform. Due to low selectivity the protective SiO_2 may be etched as well.

E) Wet SiO_2 Release



- 1 µm thick uniform Single Crystal Silicon membranes.
- The ripples on the membranes have disappeared.
- Very clean membrane formation.
- No polymers are left on the single crystal silicon .

Single crystal Si membrane release with wet-etch is completed.

F) Orifice Formation

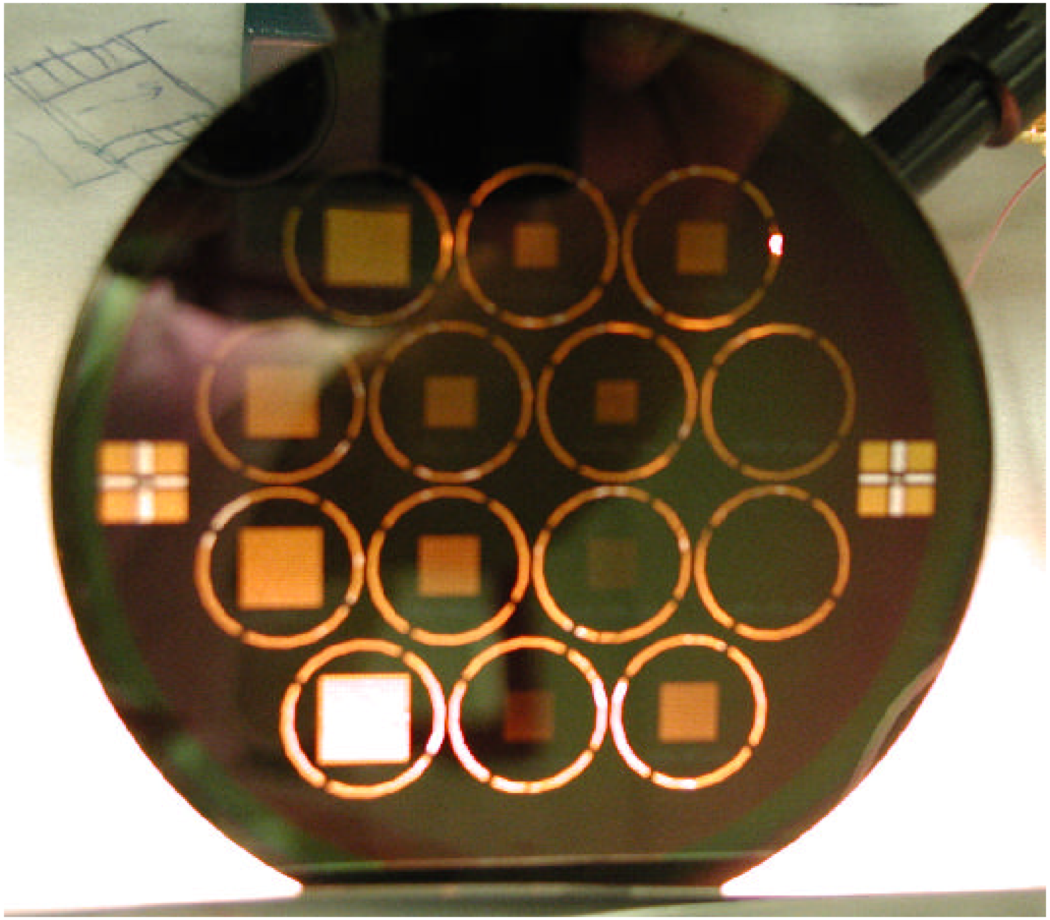
- The orifice should be located in the exact center of the membrane to benefit from maximum membrane displacement.

- The lithography must be very accurate.

- Alignment marks must be well protected during all process steps.

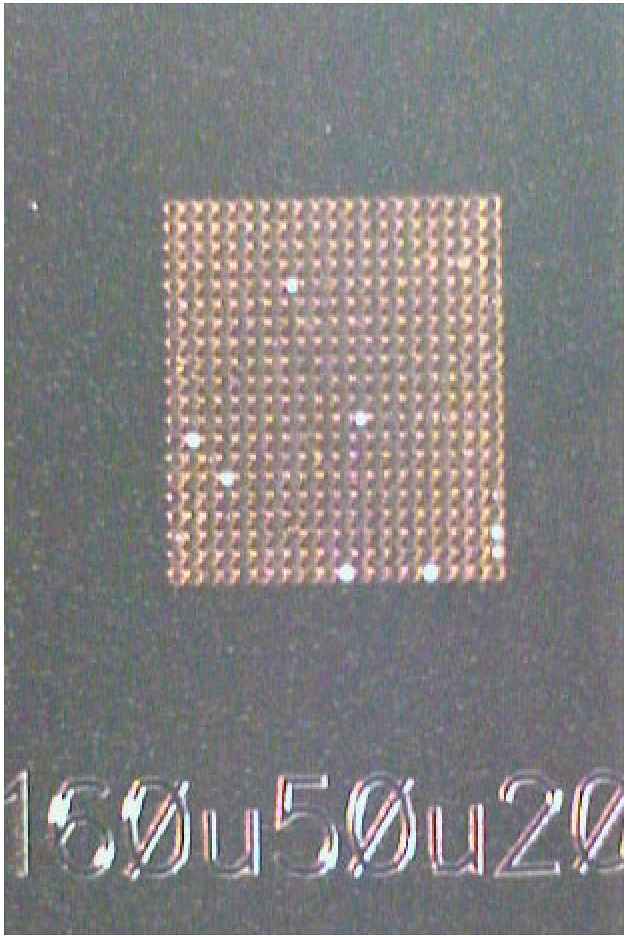
- Orifices are uniform size as a result of good lithography and dry etching.

2D Micro-machined Array: Old Process



Various membrane radii and device sizes on a Silicon wafer

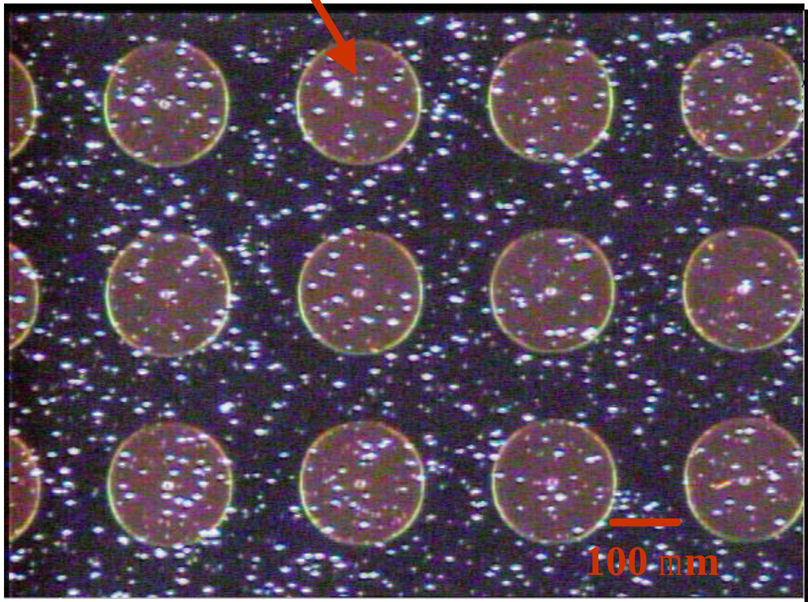
2D Micro-machined Array: Actual Device



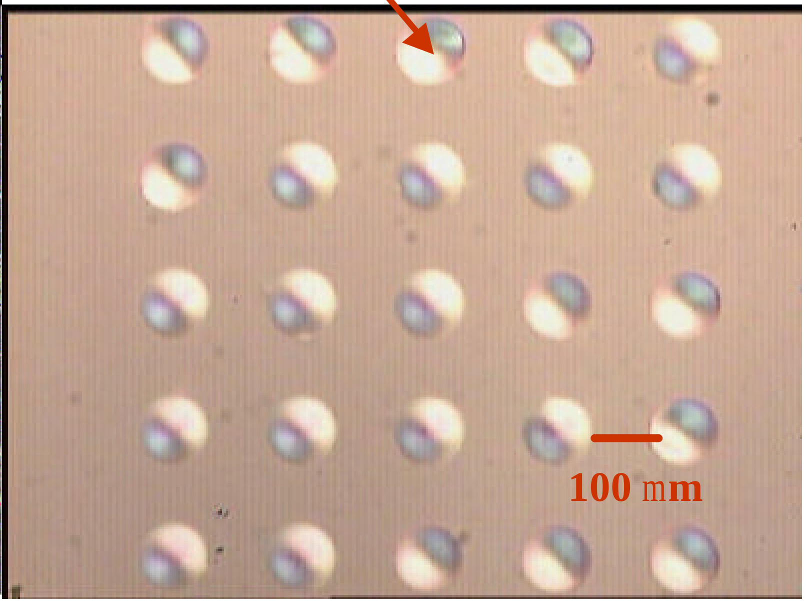
- 2D array of ejectors (20x20)
- The membrane diameter is 160 μm
- Orifice size is 10 μm
- Thin silicon nitride membrane
- Deep reactive ion etched reservoir

Old Process vs. New Process
Si_3N_4 vs. Single Crystal Si Arrays

Silicon-nitride membrane



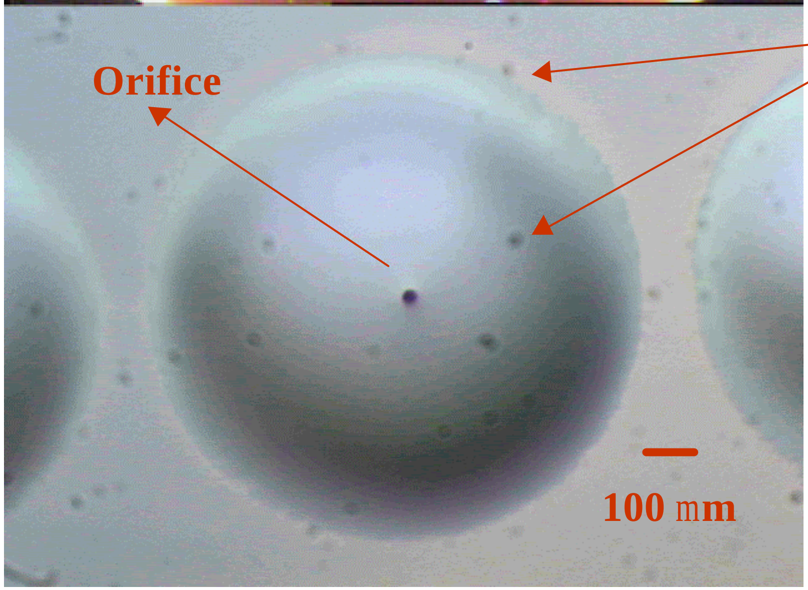
Single Crystal Si membrane



Membrane diameter : 160 µm
Orifice diameter : 10 µm

Membrane diameter : 100 µm
Orifice diameter : 14 µm

Old Process vs. New Process:
Si_3N_4 vs. Single Crystal Membrane



Silicon-nitride membrane:

Membrane diameter : 160 µm
Orifice diameter : 10 µm

The black marks are on the camera lens **not** on the membrane surface.

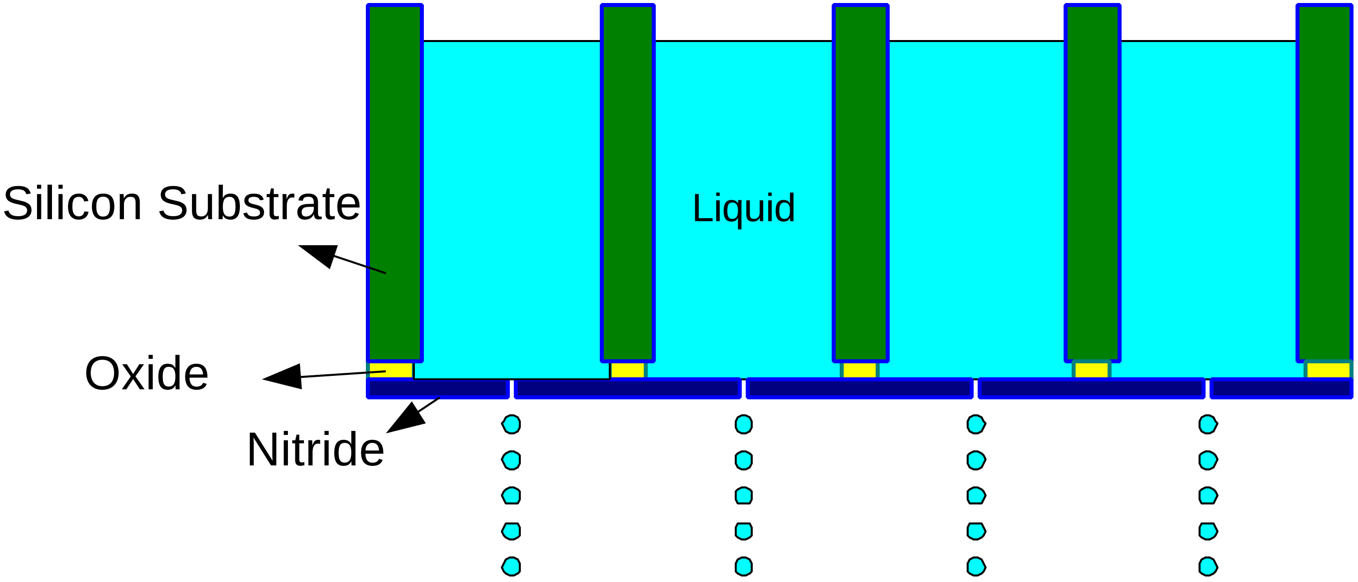
Single Crystal Si membrane:

Membrane diameter : 100 µm
Orifice diameter : 14 µm

Desired Good Ejection by 2D Arrays

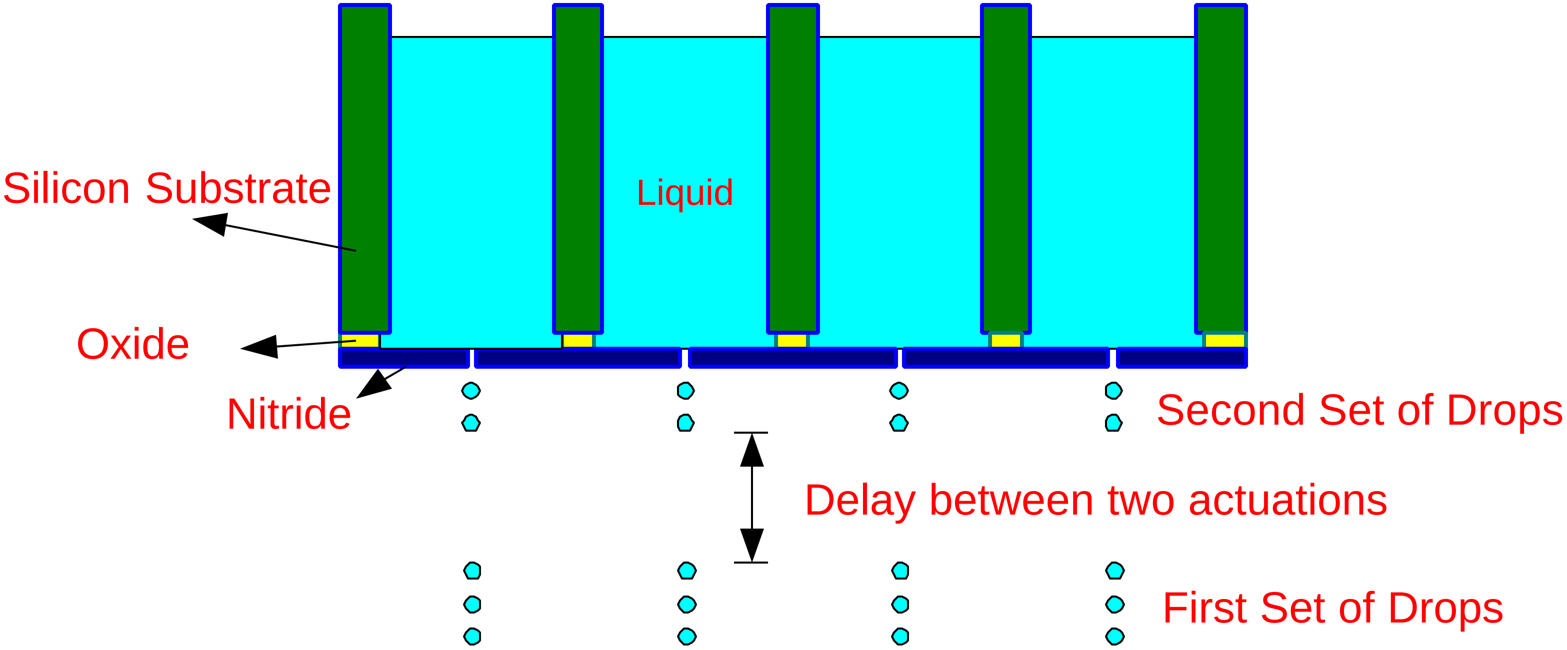
- All membranes should be ejecting simultaneously
- Ejection should be perpendicular to the device surface
- Drop on Demand Ejection should be possible
- Droplet size and ejection speed should be controllable

Simultaneous Ejection



- Continuous Wave actuation
- All membranes eject simultaneously
- The droplets eject perpendicularly to the device surface

Drop on Demand Ejection



- The aim is to be able eject
  - a desired number of droplets
  - at a desired time

Conclusions

- A new ejector fabrication process has been developed that provides
  - Uniform membranes
  - More control on material properties
  - Stress free membranes (no membrane buckling)
- Demonstrated **single crystal silicon** membranes in a 2D Array of micromachined ejectors.

Future Work

- Test the fabricated single crystal silicon membranes and compare their operating features with FEM predictions.
- Fabricate single crystal silicon membranes, where the orifice is formed by wet etching.
- Perform FEM simulations to understand cross-talk issues and model the devices.
- Use the new fabrication process to build ejectors capable of better controlled ejection
  - Drop on Demand ejection
  - All array membranes active at a given time

Future Work

- Test silicon nitride membrane devices and single crystal silicon devices for ejection of fluids with higher viscosities than water, i.e. photoresist, low-*k* and high-*k* dielectrics.
- Upgrade the experimental setup for the new experiments.
- Demonstrate full photoresist coverage of a wafer using micro-machined 2D ejector arrays.