Chip-Scale Modeling of Pattern Dependencies in Copper Chemical Mechanical Polishing (CMP) Processes

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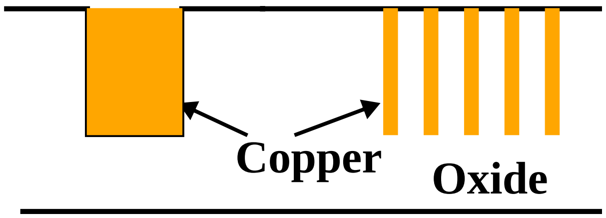
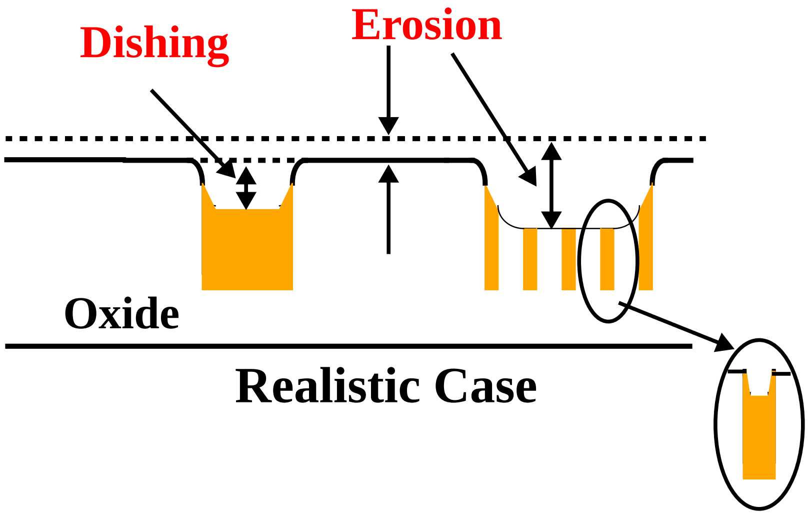
http://www-mtl.mit.edu/Metrology/Publications.html

Problem Statement: Dishing and Erosion

Single Level

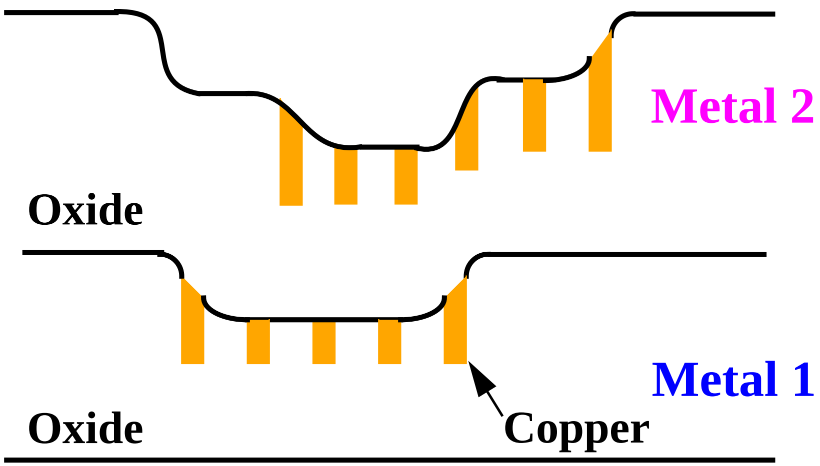


Ideal Case



Realistic Case

Multi Level



- Increased line resistance
- Within-die surface non-uniformity
- Cumulative non-uniformity on higher metal levels

Contributions

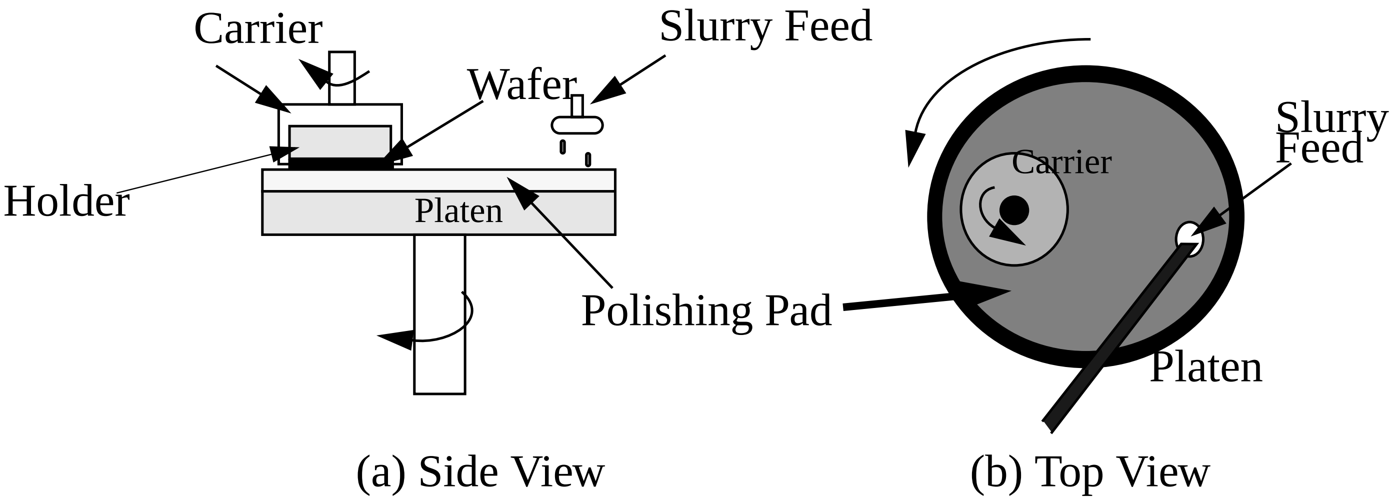
- Development of a semi-physical chip-scale pattern dependent model (with calibration/characterization methodology) for copper CMP processes.
    - ❑ Accounts for temporal evolution of bulk copper polishing and pattern dependencies in bulk copper polishing
    - ❑ Accounts for temporal and pattern dependencies of dishing and erosion
    - ❑ Framework is flexible and extendable to account for effects in all copper CMP processes

- Development of a simulator (based on model equations) that can:
    - ❑ Predict dishing and erosion across an entire chip, for a random layout
    - ❑ Capture the temporal evolution of bulk copper polishing across an entire chip, for a random layout
    - ❑ Assess the effectiveness of dummyfication in minimizing within-die non-uniformity
    - ❑ Identify bulk copper clearing problems in multi-level metallization schemes
    - ❑ Aid in the generation of smart interconnect design rules

Outline

- ✔ **Introduction to Copper CMP**
  - ❑ What is Chemical Mechanical Polishing?
  - ❑ Copper CMP Process
- ■ Copper CMP Model Development
- ■ Chip-Scale Simulation
- ■ Conclusion and Future Work

What is Chemical Mechanical Polishing?

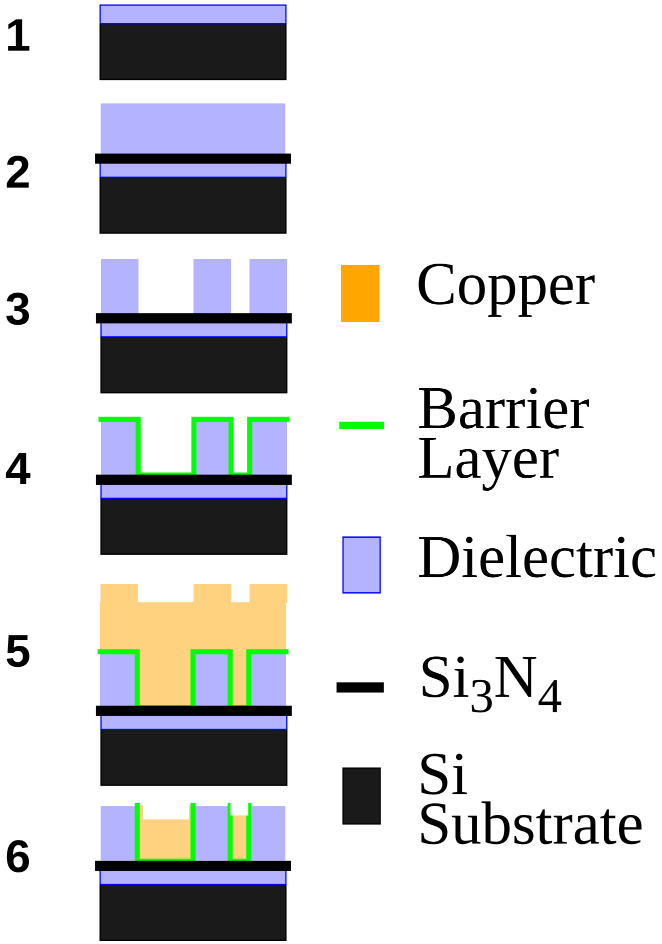


(a) Side View

(b) Top View

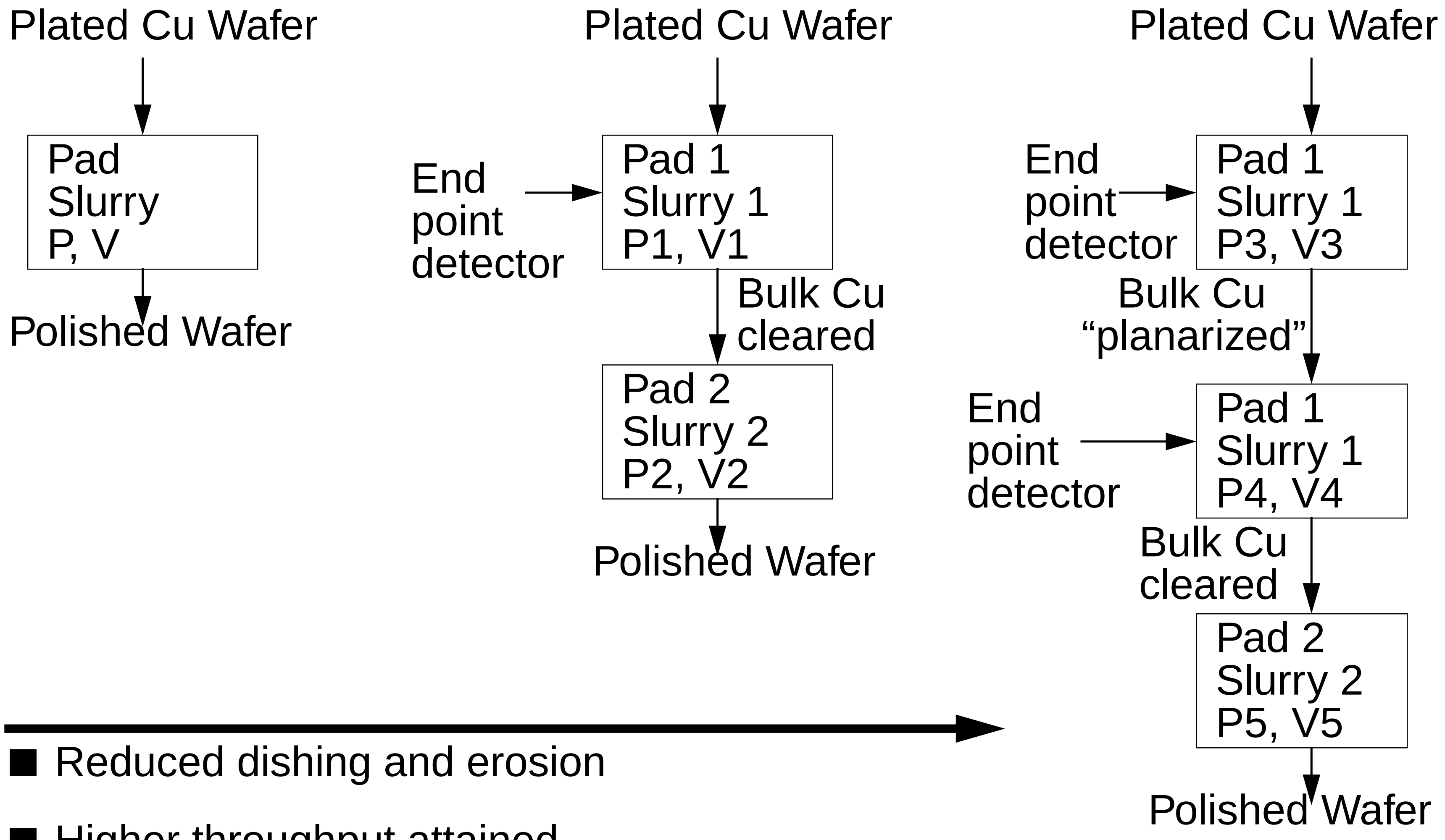
- **Slurry**:
  - An abrasive held in chemical solution
  - A chemical solution with no abrasives
- **Pads:**
  - Porous pad transports slurry and supplies mechanical energy to surface
- **Material removed by a combination of**
  - Mechanical action -- relative movement and pressure necessary
  - Chemical action -- slurry solution enhances or inhibits material removal

Copper Damascene Process



- Deposit dielectric
- Deposit silicon nitride (to act as etch stop), and deposit dielectric on top of the nitride
- Etch the dielectric to form trenches for the copper interconnects
- Deposit a barrier layer to act as an adhesive and a diffusion barrier
- Deposit a thin seed copper film by PVD, followed by a thicker copper film by electroplating.
- Use CMP to clear copper overburden and barrier layer between trenches

Copper CMP Process: Single-Step vs Multi-Step



Plated Cu Wafer

Pad
Slurry
P, V

Polished Wafer

Plated Cu Wafer

End point detector

Pad 1
Slurry 1
P1, V1

Bulk Cu cleared

Pad 2
Slurry 2
P2, V2

Polished Wafer

Plated Cu Wafer

End point detector

Pad 1
Slurry 1
P3, V3

Bulk Cu “planarized”

End point detector

Pad 1
Slurry 1
P4, V4

Bulk Cu cleared

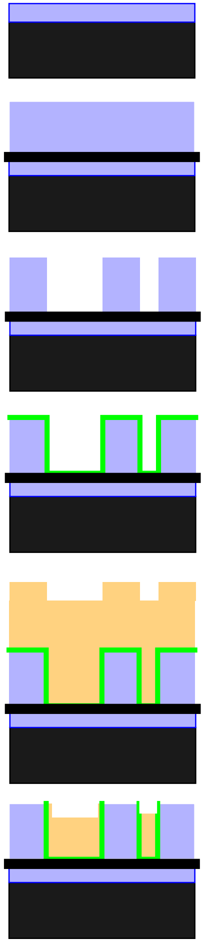
Pad 2
Slurry 2
P5, V5

Polished Wafer

- Reduced dishing and erosion
- Higher throughput attained

Copper CMP Process (cont.)

Damascene Process



🟧 Copper

— Barrier Layer

▨ Dielectric

— Si_3N_4

■ Si Substrate

Multi-Step Copper CMP Process

Plated Copper Wafer

↓

Step 1 Process: High DF, High Speed, Slurry 1 ← Endpointing with iScan: Targeted Cu Thickness

↓

Step 2 Process: Low DF, Moderate Speed, Slurry 1 ← Clearing Endpointing plus Fixed Time Polish

↓

Step 3 Process: Moderate DF, Moderate/High Speed, Slurry 2 ← Fixed Time Polish

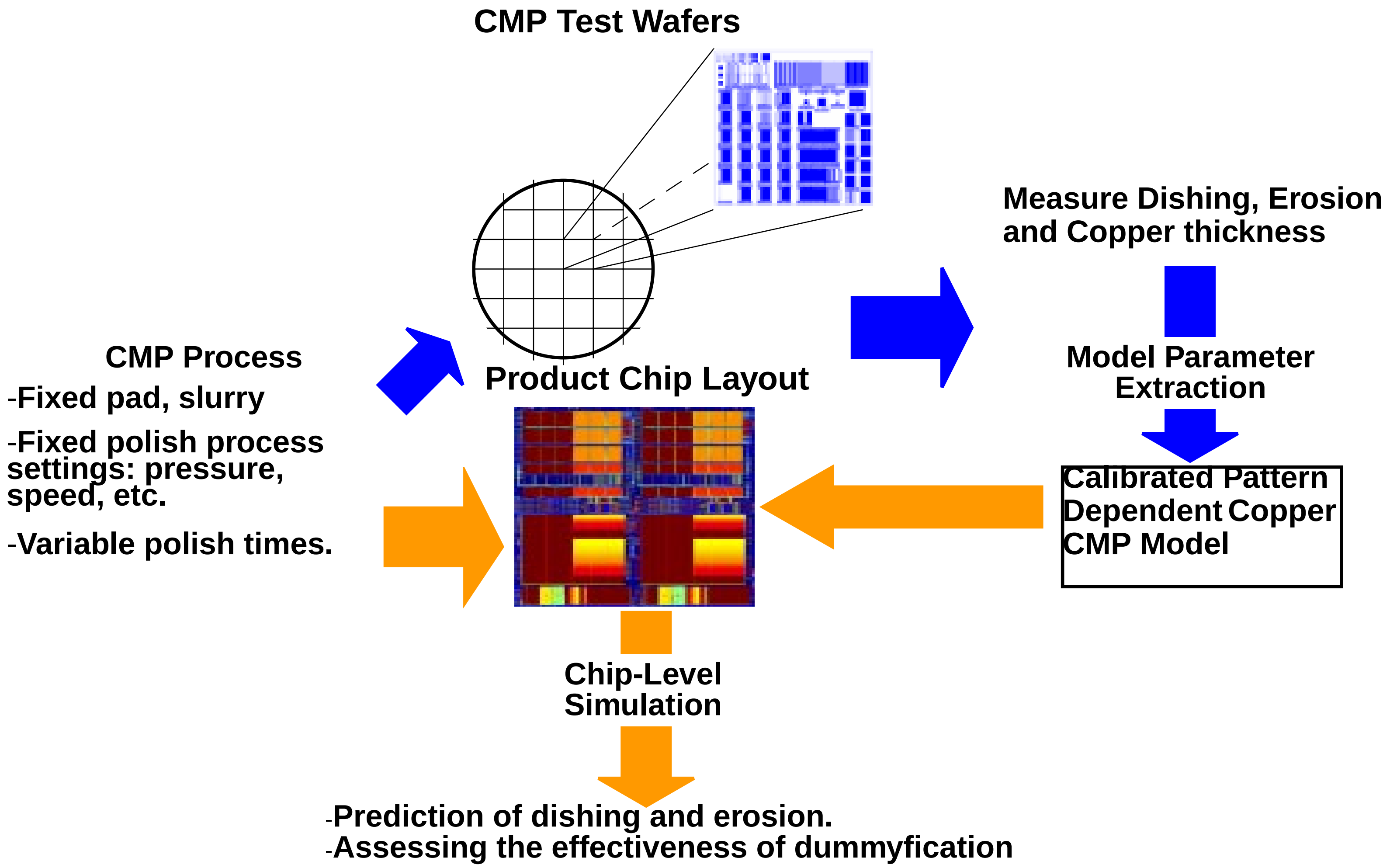
↓

Cleaning

Outline

- ■ Introduction to Copper CMP
- ✔ **Copper CMP Model Development**
  - ❏ Integrated Copper CMP Characterization and Modeling Methodology
  - ❏ Intrinsic Stages in Copper CMP
  - ❏ CMP Test Mask Design
  - ❏ Metrology
  - ❏ Dishing and Erosion Dependencies
  - ❏ Density-Step-Height Model
  - ❏ Integrated Contact Mechanics and Density-Step-Height Model
- ■ Chip-Scale Simulation
- ■ Conclusion and Future Work

Integrated Copper CMP Characterization and Modeling Methodology



CMP Test Wafers

CMP Process
- **Fixed pad, slurry**
- **Fixed polish process settings: pressure, speed, etc.**
- **Variable polish times.**

Product Chip Layout

Measure Dishing, Erosion and Copper thickness

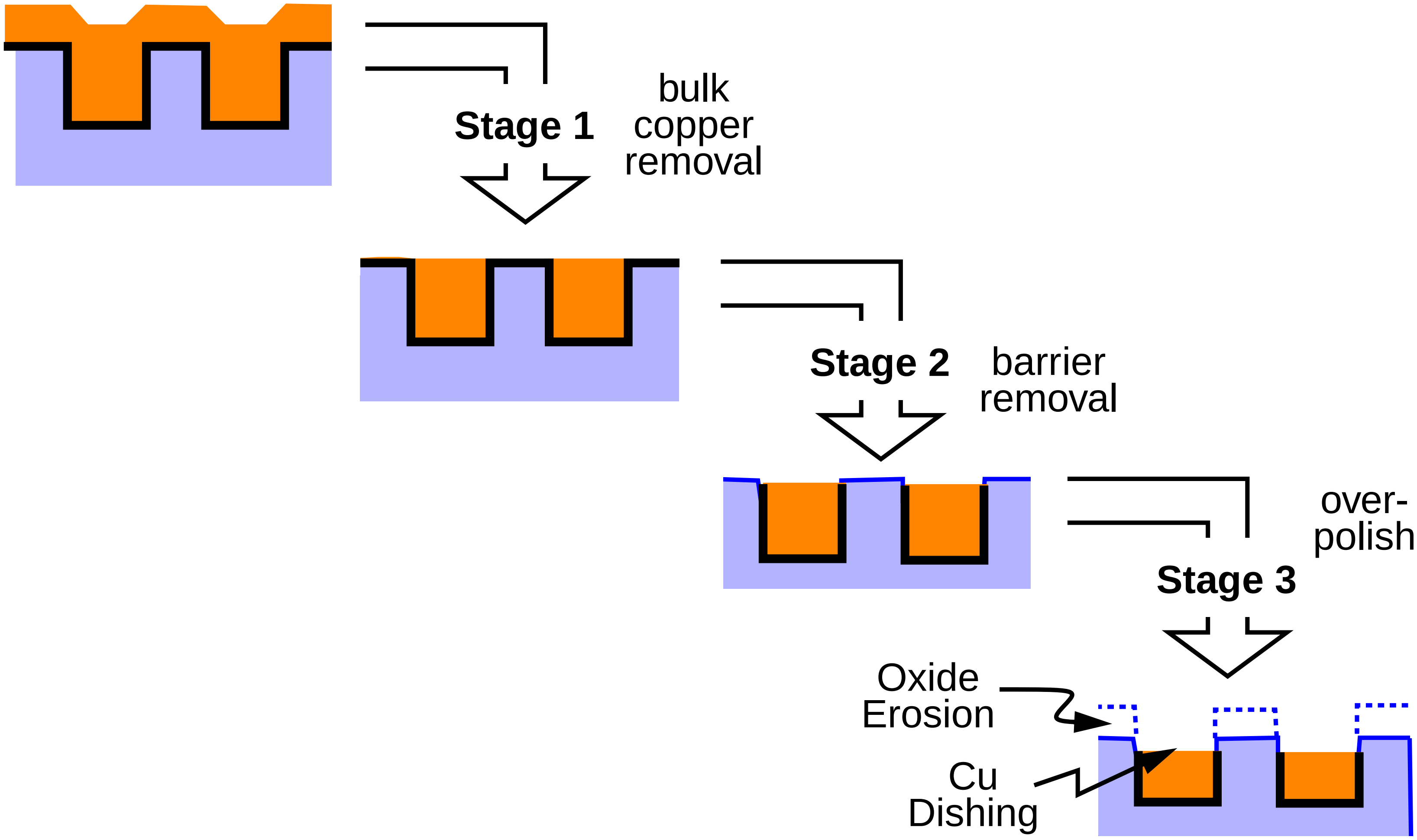
Model Parameter Extraction

Calibrated Pattern Dependent Copper CMP Model

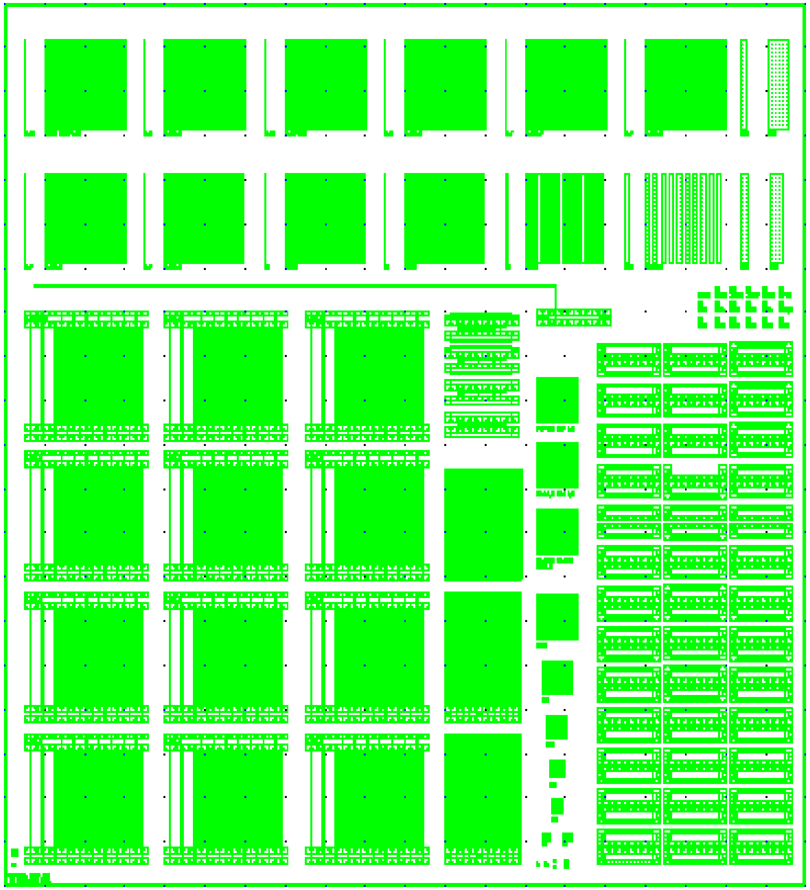
Chip-Level Simulation

- **Prediction of dishing and erosion.**
- **Assessing the effectiveness of dummyfication**

The Three Intrinsic Stages in Copper CMP



CMP Test Mask Design



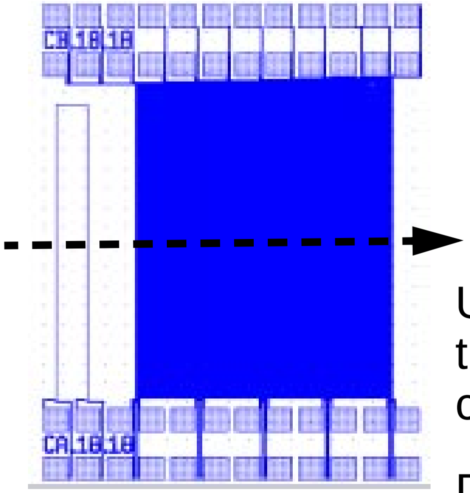
Mask 931 - Version 1.2

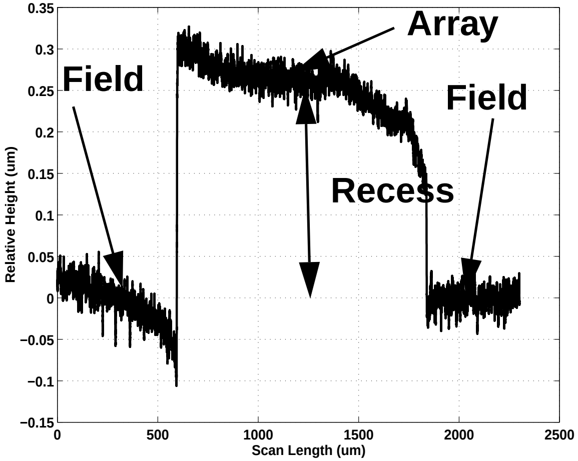
- Single level mask with electrically testable and physically testable structures.
- Layout Factors: Line width and line space combinations
  - ❑ Minimum feature size: 0.25 µm
  - ❑ Density range: 10 % to 90 %
  - ❑ Pitch range: 0.5 µm to 200 µm
- Structures:
  - ❑ Arrays and isolated lines
  - ❑ Slotting
- Other variants of this mask have been designed and used in this work

Metrology

- Copper Thickness Measurement
    - ❑ Blanket wafers: Four Point Probe (from Prometrix)
    - ❑ Patterned wafers: MetaPULSE 200x (from Rudolph) or Impulse 300 (from Philips Analytical)
        - MetaPULSE: spot size of 20 μm and measurement accuracy of 300 Å for thick copper films
    - ❑ Patterned Wafers: Electrical measurements (can only be done after bulk copper and unwanted barrier film are completely cleared from wafer)
- Surface Profile Measurement
    - ❑ HRP (tip size of about 0.1 μm) and Veeco Profiler with AFM capabilities (tip size of less than or equal to 0.1 μm)
        - Levelling a surface profile can be very challenging
- Dielectric Thickness Measurement
    - ❑ UV-1280 (From KLA Tencor) - spot size of 5 μm at high magnification
    - ❑ F5 (From KLA Tencor) - spot size of less than or equal to 5 μm at high magnification. Measurement accuracy of 50 - 100 Å on oxide

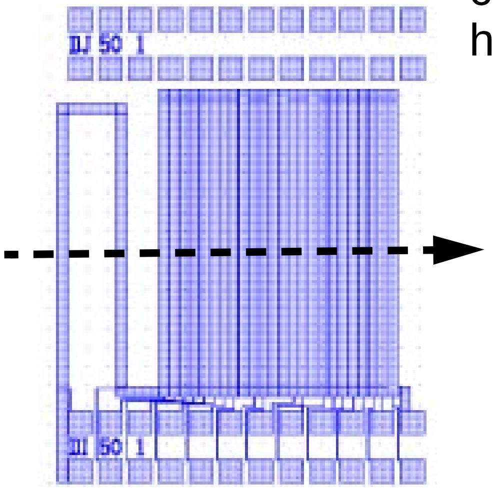
Metrology: Copper Thickness Measurement

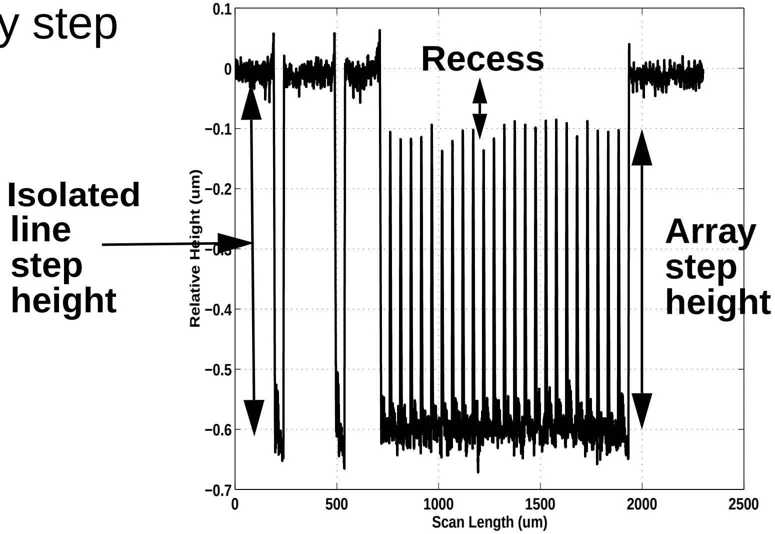




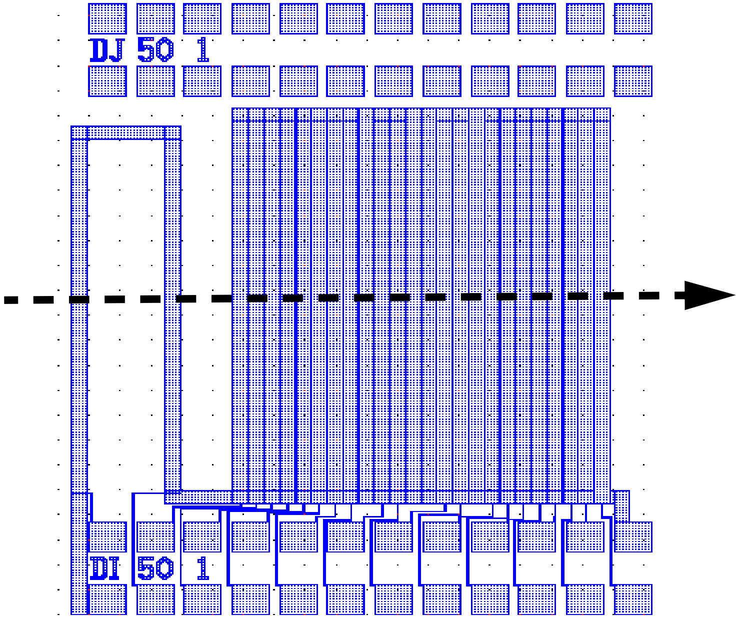
Up-array array copper thickness = Average field copper thickness - Recess

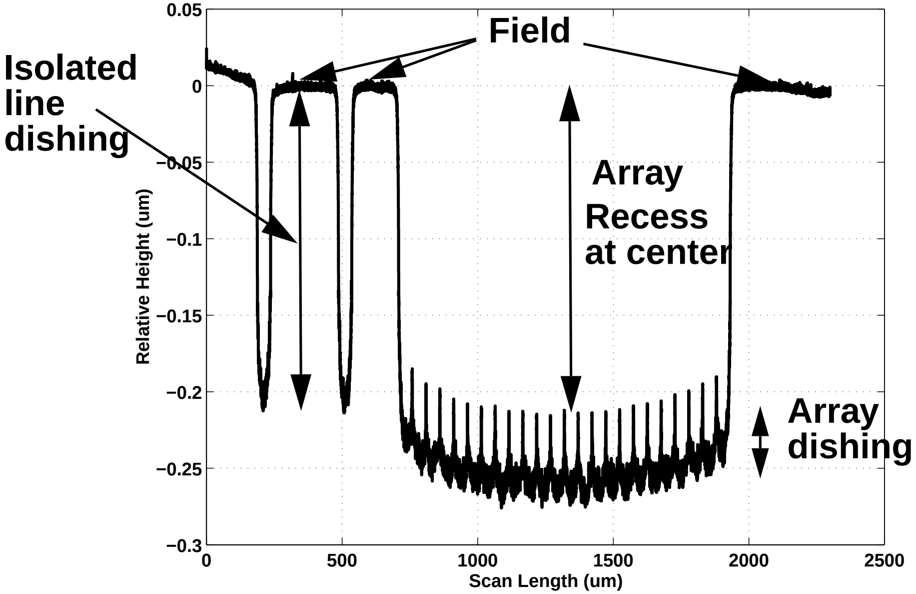
Down-area array copper thickness = Up-area array copper thickness - Array step height





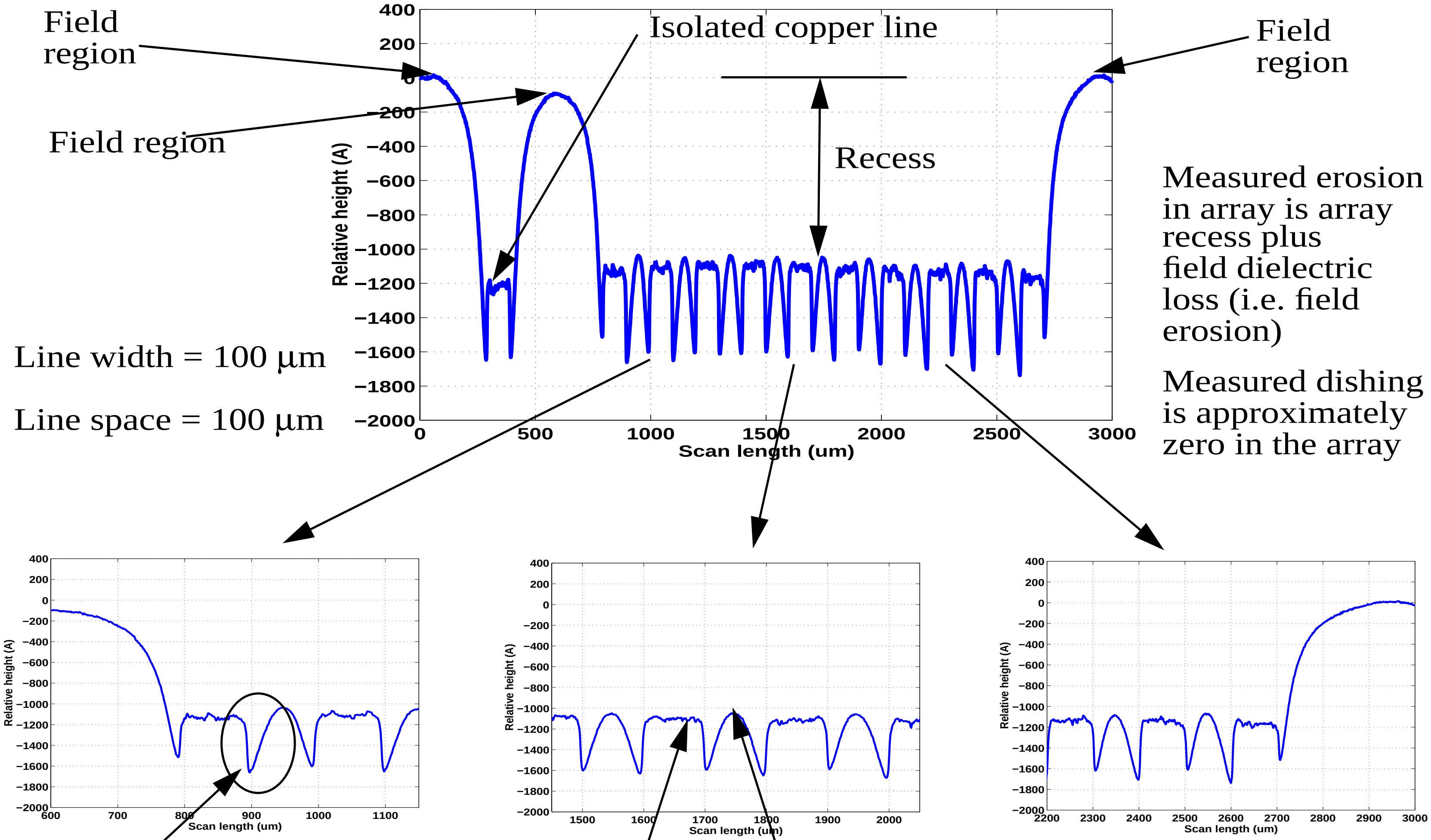
Metrology: Dishing and Erosion Measurements





Array erosion = Average field dielectric thickness loss + Recess

Limitations of Measurement Technique



Field region

Field region

Isolated copper line

Field region

Recess

Measured erosion in array is array recess plus field dielectric loss (i.e. field erosion)

Measured dishing is approximately zero in the array

Line width = 100 µm

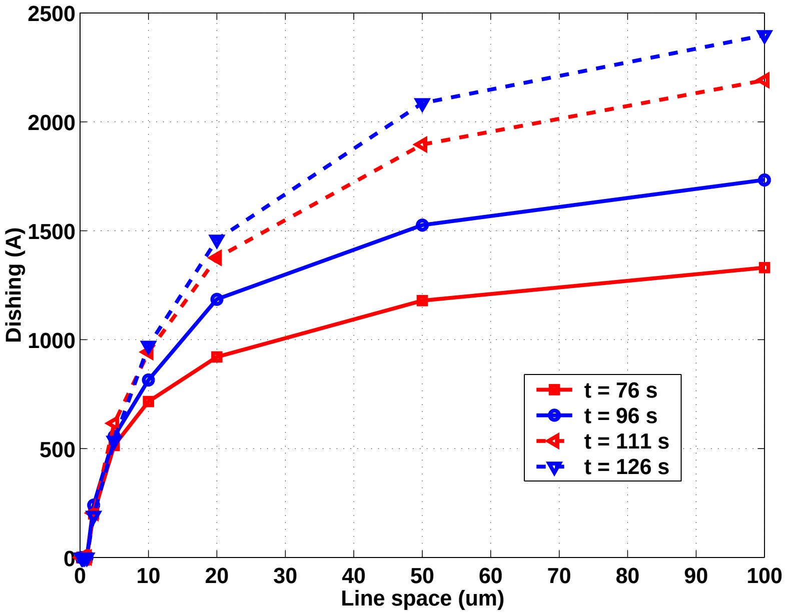
Line space = 100 µm

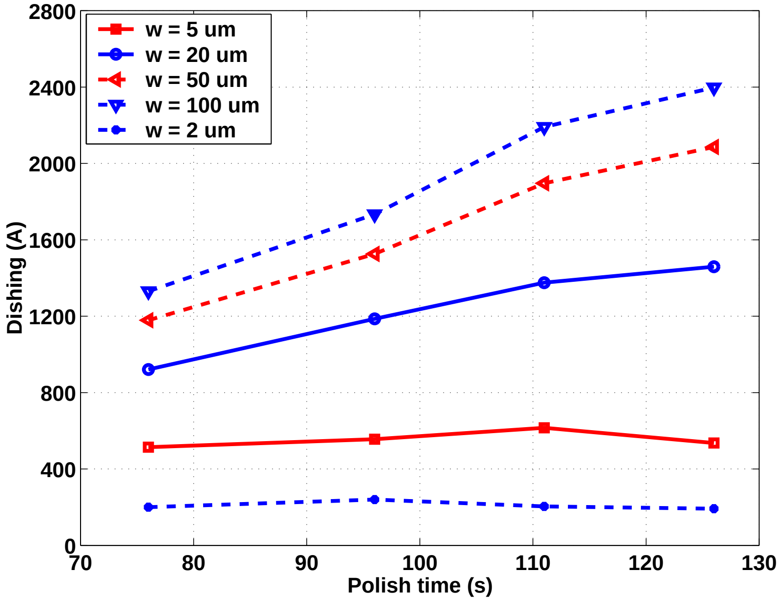
Apparent void between copper and dielectric due to excessive dielectric edge rounding

Copper (line width)

Dielectric (line space)

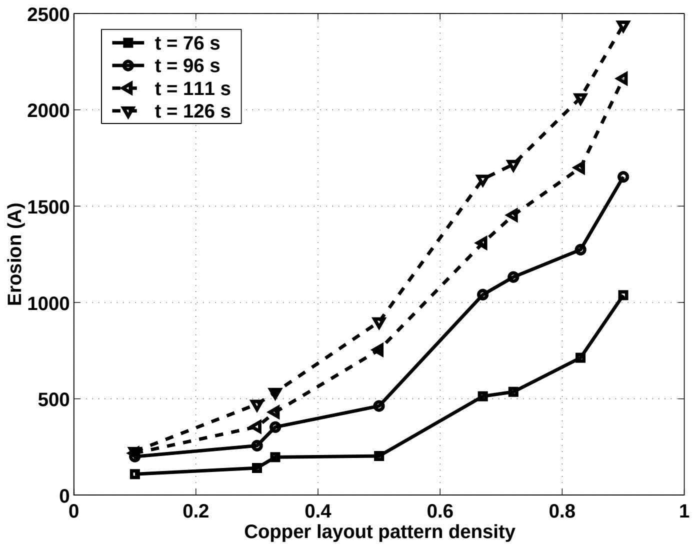
Measured Dishing Dependencies

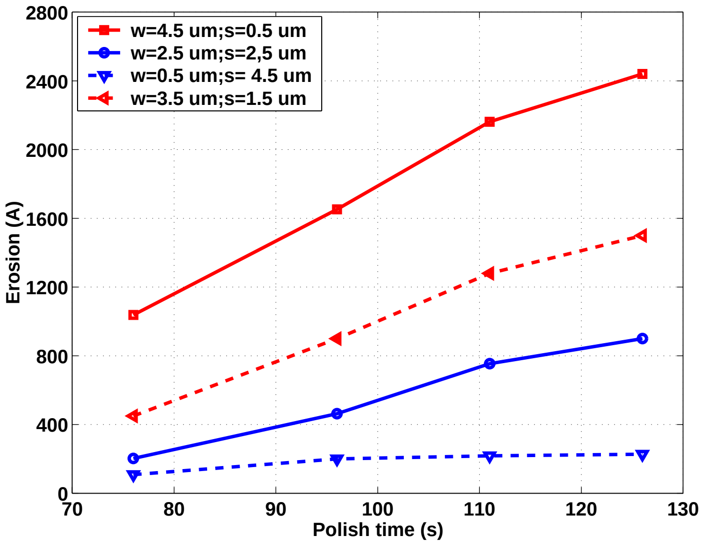


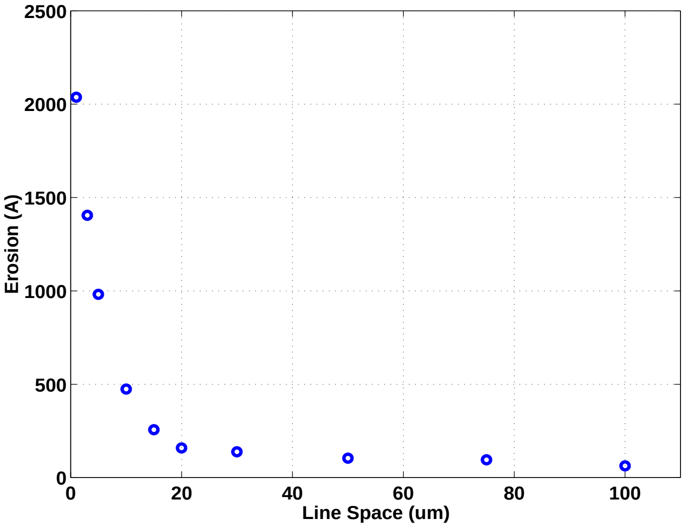


- Dishing depends on line width and line space (for conventional copper CMP processes).
- Dishing depends on polish time. It reaches steady state quickly for fine features.
- Dishing depends on process settings and consumable set.

Measured Erosion Dependencies

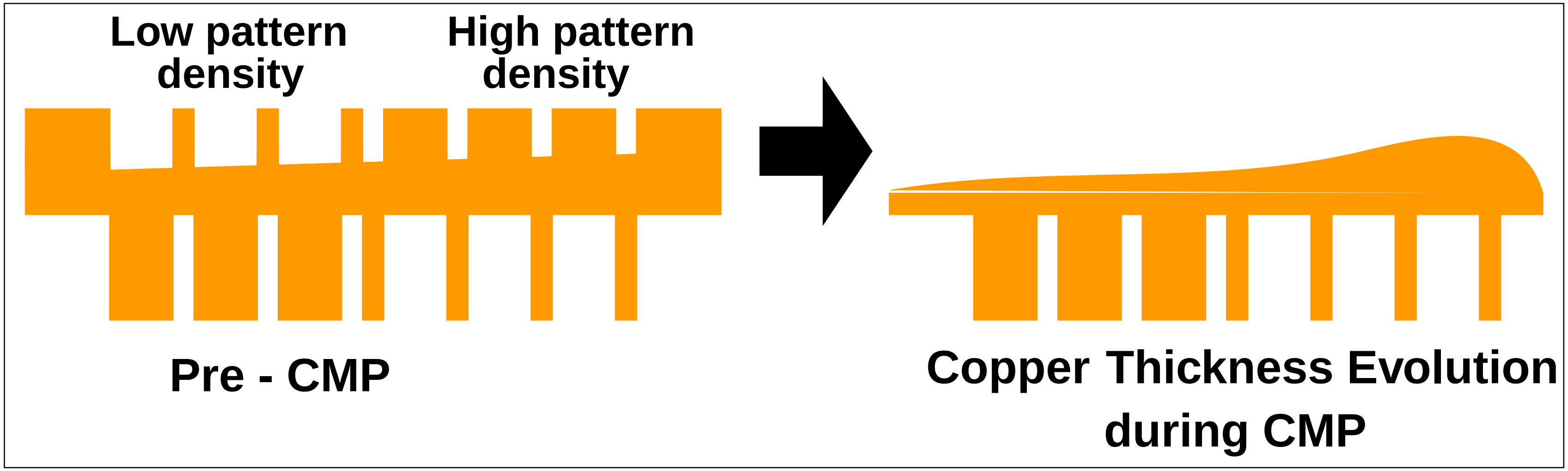






- Erosion depends on pattern density and line space.
- Erosion depends on polish time (overpolish time).
- Erosion depends on process settings and consumable set.

Density-Step-Height Model: Pattern Density Effect

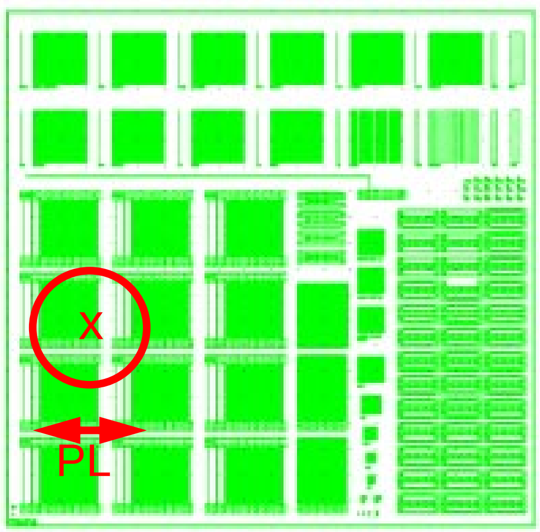


- Basic idea: up-area removal rate depends on up-area fraction (pattern density).

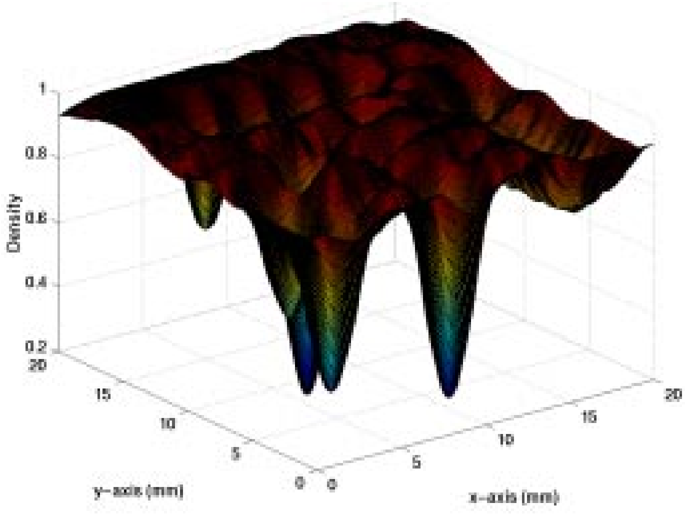
- The effective density at each point depends on nearby topography and the layout density at that point.

- The effective density can be determined by averaging local layout densities over a planarization length (L).

Pattern Density Effect (cont).



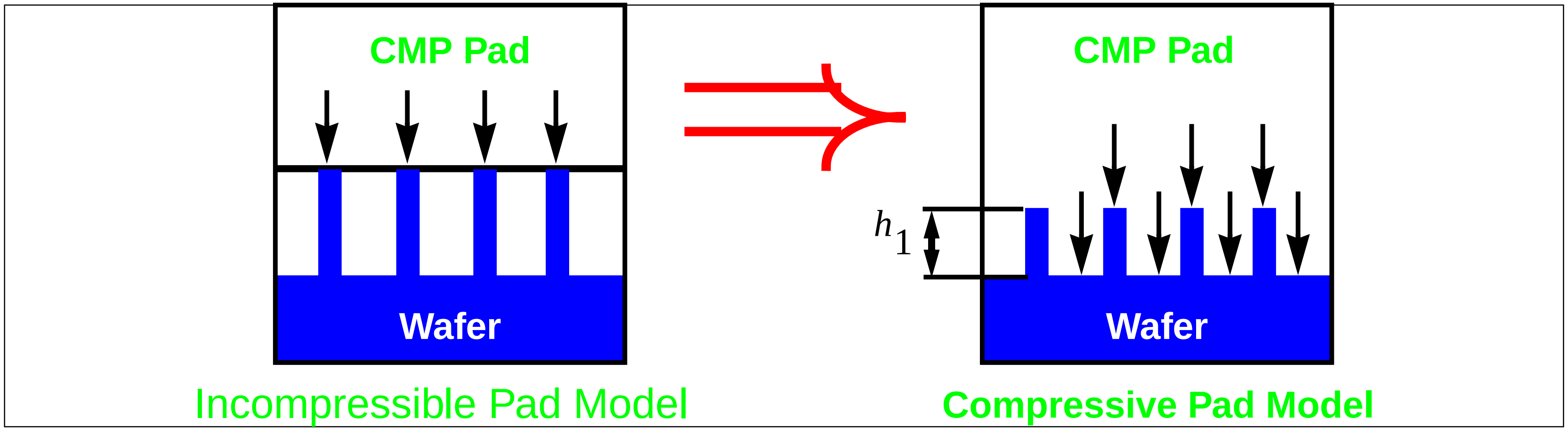
Mask 931- version 1.2



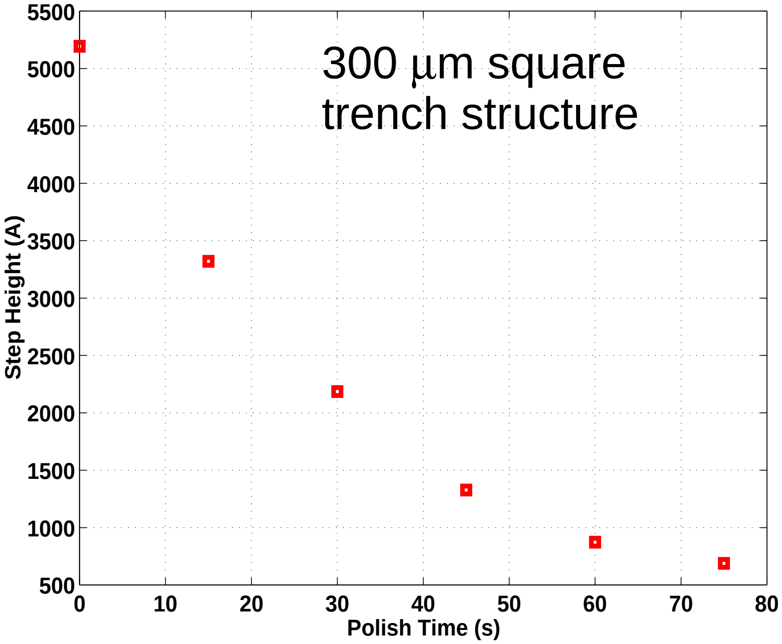
Electroplated effective pattern density assuming a planarization length of 2.76 mm

- Use circular weighted window (based on deformation of an elastic material) to calculate average or effective density for each point on die.
- The polish rate at each point is inversely proportional to the effective density at that point.

Step Height Effect



- **Incompressible Pad Model**: up-area removal rate determined by density. No down-area removal (original MIT dielectric density Model)
- **Compressible Pad Model**: up-area and down-area removal rates are proportional to step height (Burke, Tseng, Grillaert, MIT CMP Team)
- Transition from incompressible to compressible pad model occurs at a critical height (Grillaert et al., MIT CMP Team)



Density-Step-Height-Model: Main Idea

- Removal rate is a function of pressure, relative speed, and consumable set.
  - ❑ Find the functional dependence of removal rate on pressure for given speed, and consumable set. **(OR)**
  - ❑ More generally, find the functional dependence of removal rate on pressure and speed, for given consumable set.
- Effective polish pressure is a function of step height, pattern density and the applied pressure
  - ❑ According to Hooke's law, the effective polish pressure is linearly dependent on step height
- Combine the removal rate versus pressure relationship with the pressure versus step height (and density) relationship to get a removal rate versus step height (and density) relationship.

Density-Step-Height: Bulk Cu Removal Stage

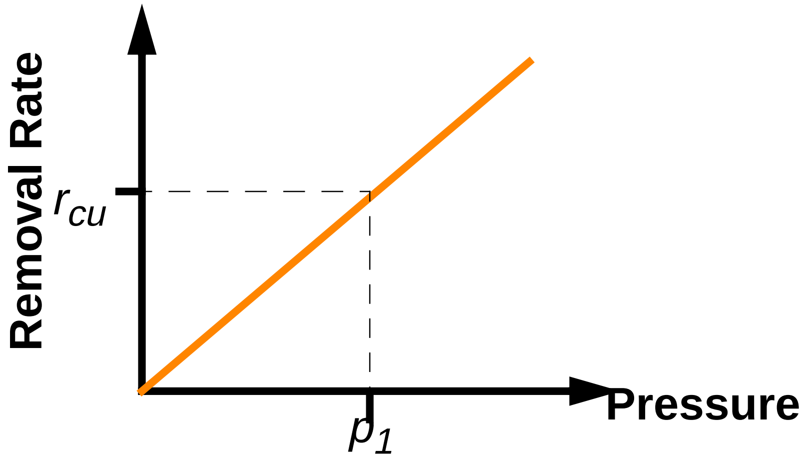


Fig. 1: Removal Rate versus Pressure

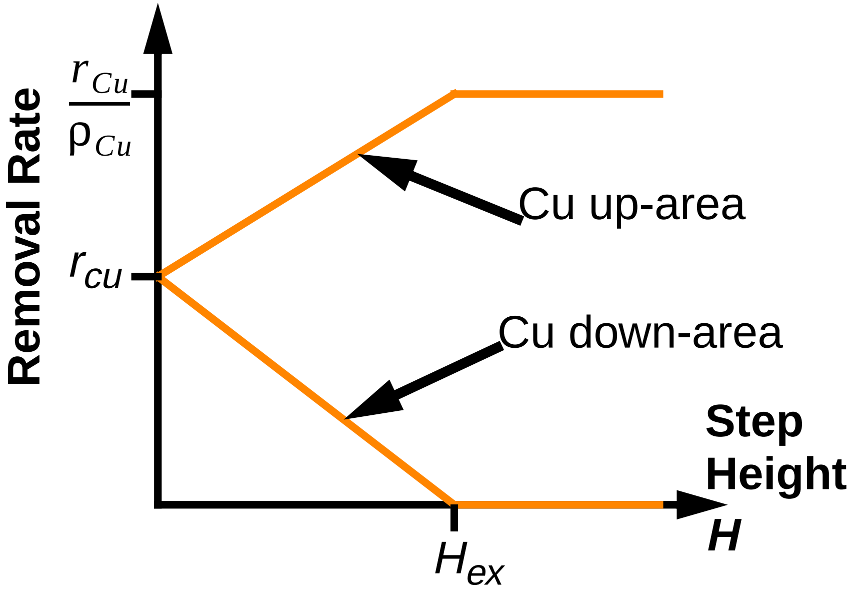


Fig. 3: Removal Rate vs Step Height

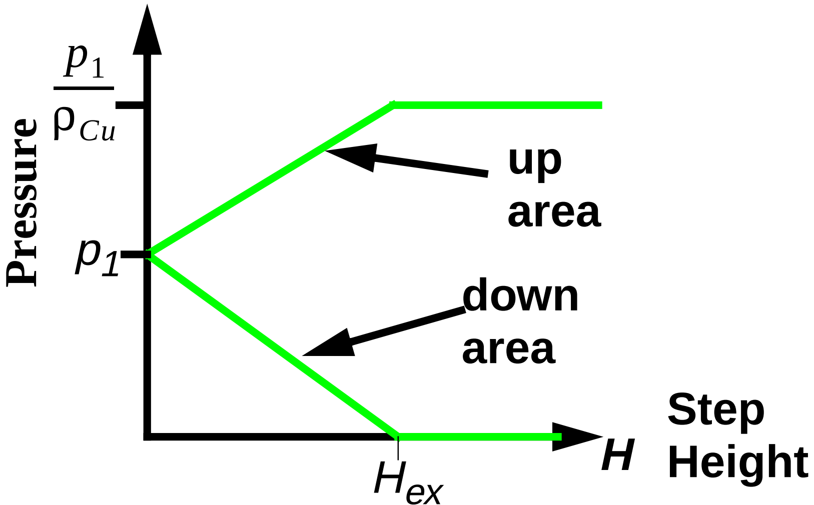
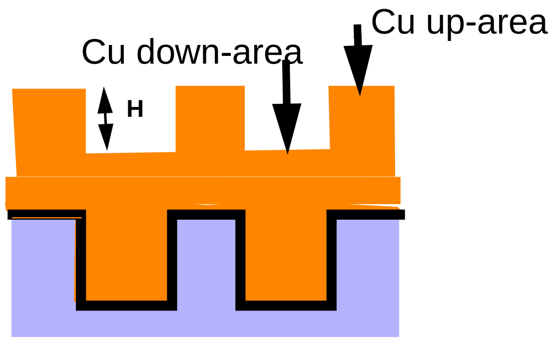


Fig. 2: Pressure versus Step Height



Density-Step-Height: Overpolish Stage

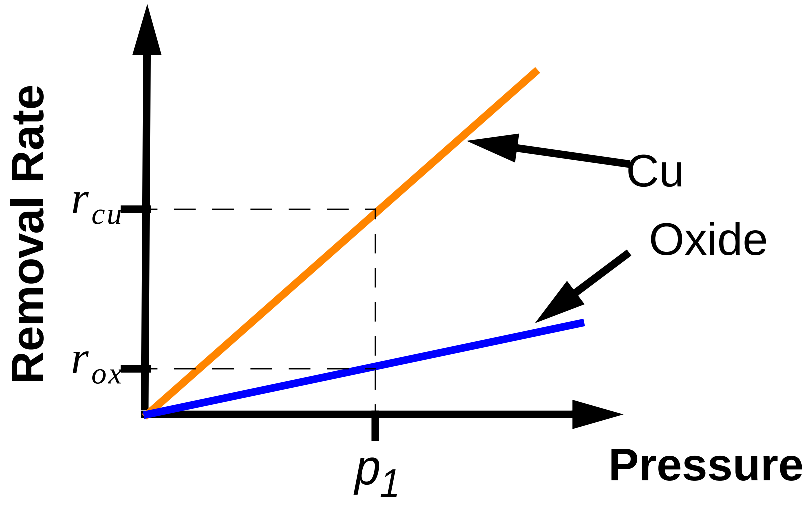


Fig. 1: Removal Rate versus Pressure

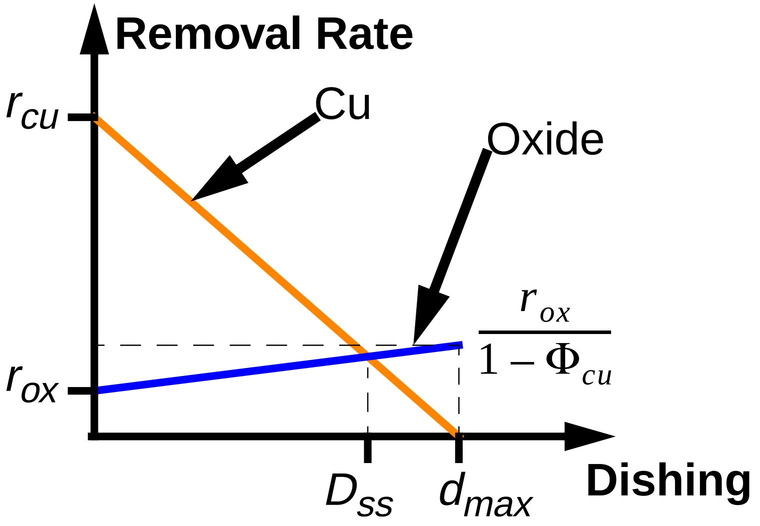


Fig. 3: Removal Rate versus Dishing

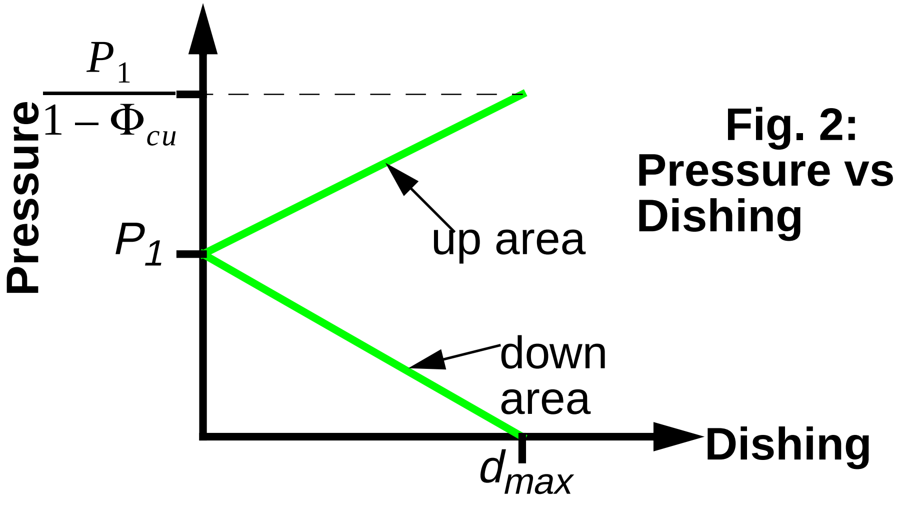
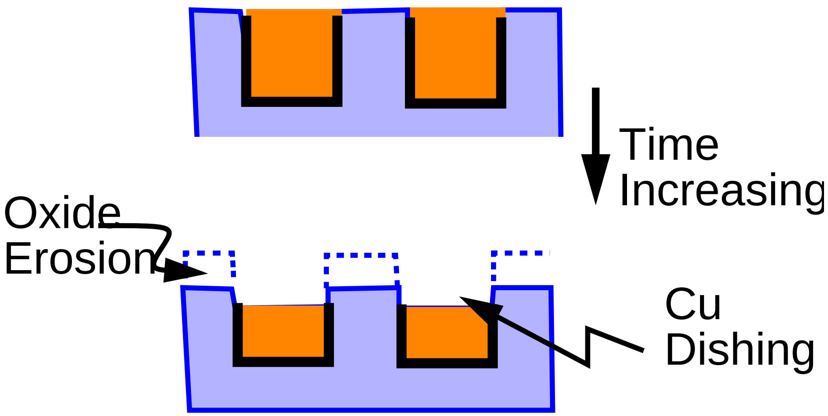


Fig. 2: Pressure vs Dishing

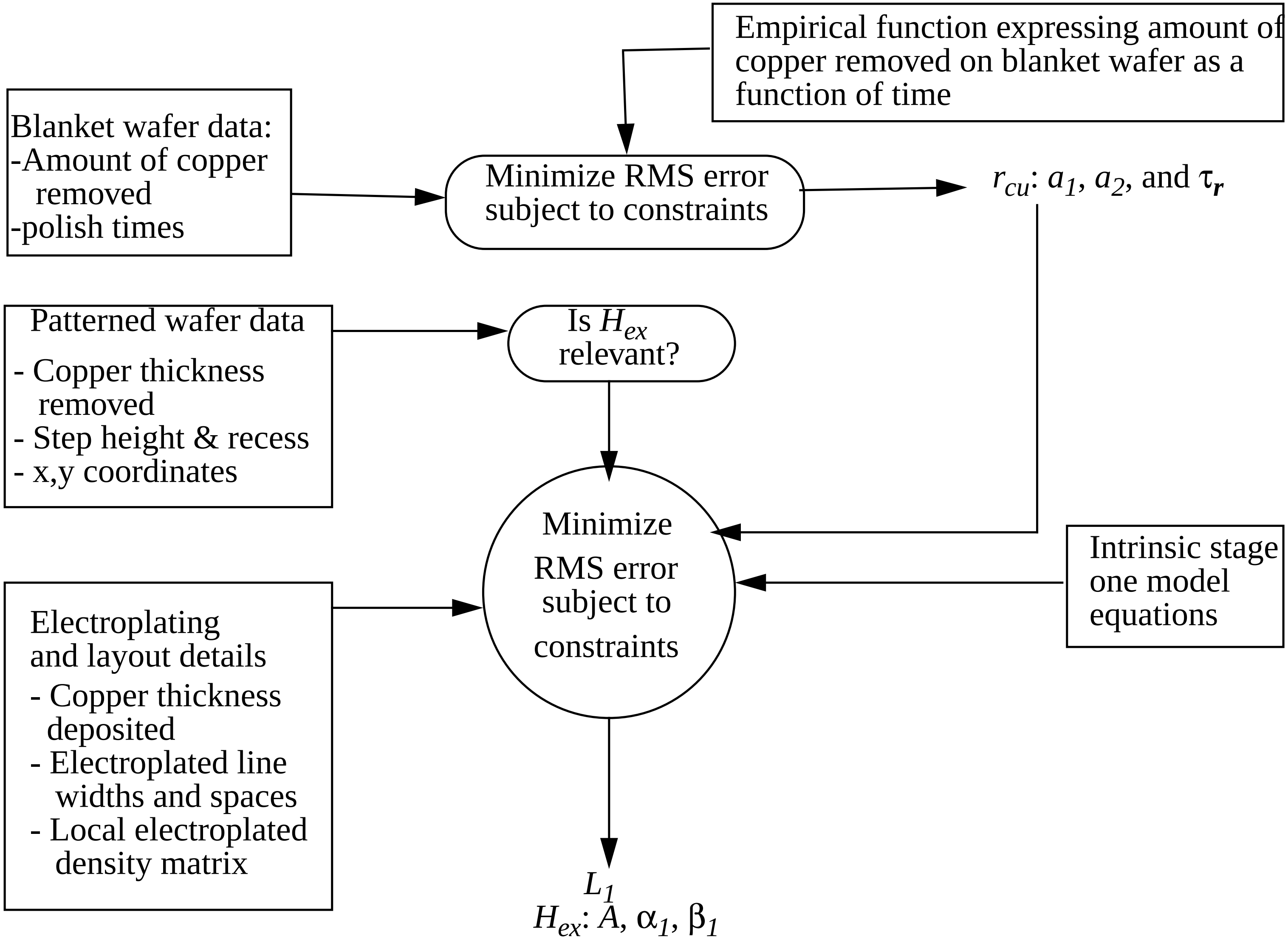


Density-Step-Height Model Parameters

Intrinsic Stage One		Intrinsic Stage Two		Intrinsic Stage Three	
r_{cu}	Effective blanket copper removal rate	r_{cu}	Effective blanket copper removal rate	r_{cu}	Effective blanket copper removal rate
L_1	Planarization length	r_b	Effective blanket barrier removal rate	r_{ox}	Effective blanket dielectric removal rate
H_{ex}	Critical Step Height	L_3	Planarization length	L_3	Planarization length
		d_{max}	Maximum dishing	d_{max}	Maximum dishing
		ψ	Edge rounding factor	ψ	Edge rounding factor

- H_{ex}: An analytical function of line width and line space (or pattern density).
- d_{max}: An analytical function of line width and line space (or pattern density)
- ψ: An analytical function of line space
- r_{cu}: Observed to be time dependent

Model Parameter Extraction Methodology: Stage 1



Empirical function expressing amount of copper removed on blanket wafer as a function of time

Blanket wafer data:
-Amount of copper removed
-polish times

Minimize RMS error subject to constraints

r_{cu}: a_1, a_2, and τ_r

Patterned wafer data
- Copper thickness removed
- Step height & recess
- x,y coordinates

Is H_{ex} relevant?

Minimize RMS error subject to constraints

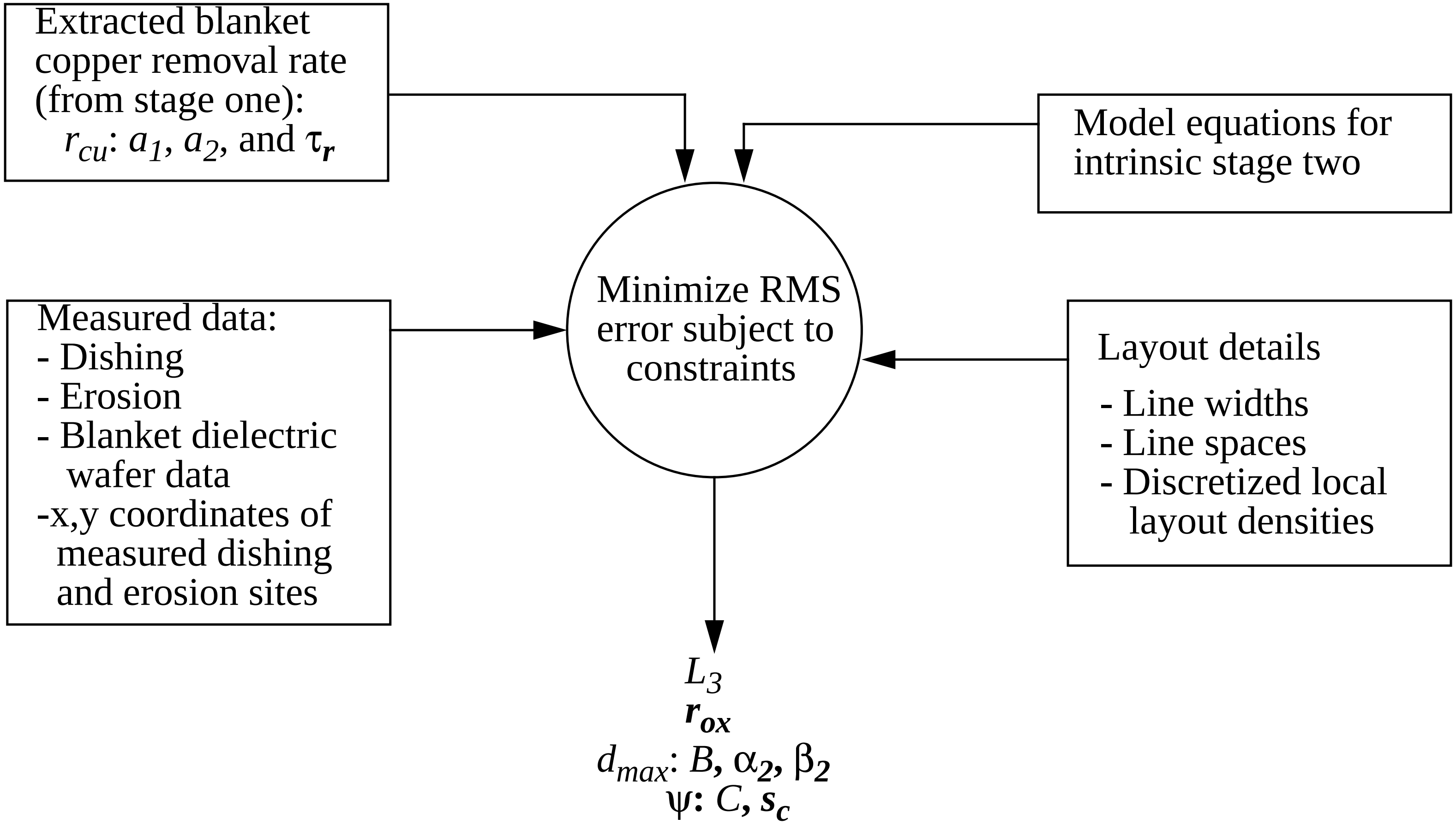
Intrinsic stage one model equations

Electroplating and layout details
- Copper thickness deposited
- Electroplated line widths and spaces
- Local electroplated density matrix

L_1

H_{ex}: A, α_1, β_1

Model Parameter Extraction Methodology: Stage 3



Extracted blanket copper removal rate (from stage one): r_{cu}: a_1, a_2, and $\tau_{\boldsymbol{r}}$

Model equations for intrinsic stage two

Minimize RMS error subject to constraints

Measured data:
- Dishing
- Erosion
- Blanket dielectric wafer data
- x,y coordinates of measured dishing and erosion sites

Layout details
- Line widths
- Line spaces
- Discretized local layout densities

L_3

$\boldsymbol{r_{ox}}$

d_{max}: B, α_2, β_2

ψ: C, s_c

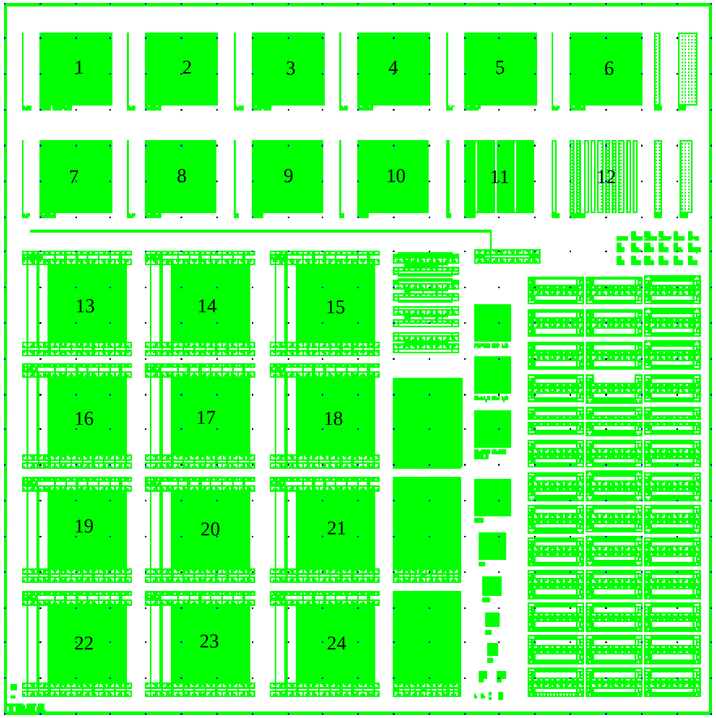
Calibration Experiment: Three Step Cu CMP Process

Three step process experiment on Mirra

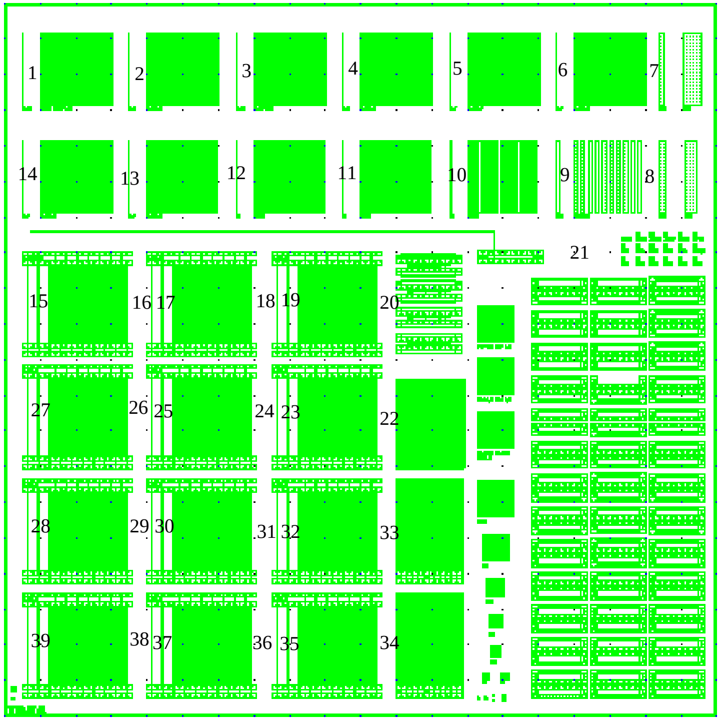
Step #	Platen #	Pad	Slurry	Down force (psi)	Speed (rpm)	Selectivity Cu:TaN:Oxide
1	1	Stacked	EPC-5001	5	63	249:4:1
2	2	Stacked	EPC-5001	2	43	232:3:1
3	3	Stacked	10K-1	3	100	2.3:1:5

- Test Mask: MIT mask version 1.2
- Time split experiments in each step
  - ❑ 5 patterned copper wafers in step 1
  - ❑ 7 blanket copper wafers in step 1
  - ❑ 5 patterned copper wafers in step two (one polish time duplicated)
  - ❑ 3 blanket copper, 3 blanket oxide, and 3 blanket TaN wafers in step 2
  - ❑ 4 patterned copper wafers in step 3
  - ❑ 3 blanket copper, 3 blanket TaN, 3 blanket oxide wafers in step 3

Array and Field Sites used in Extraction



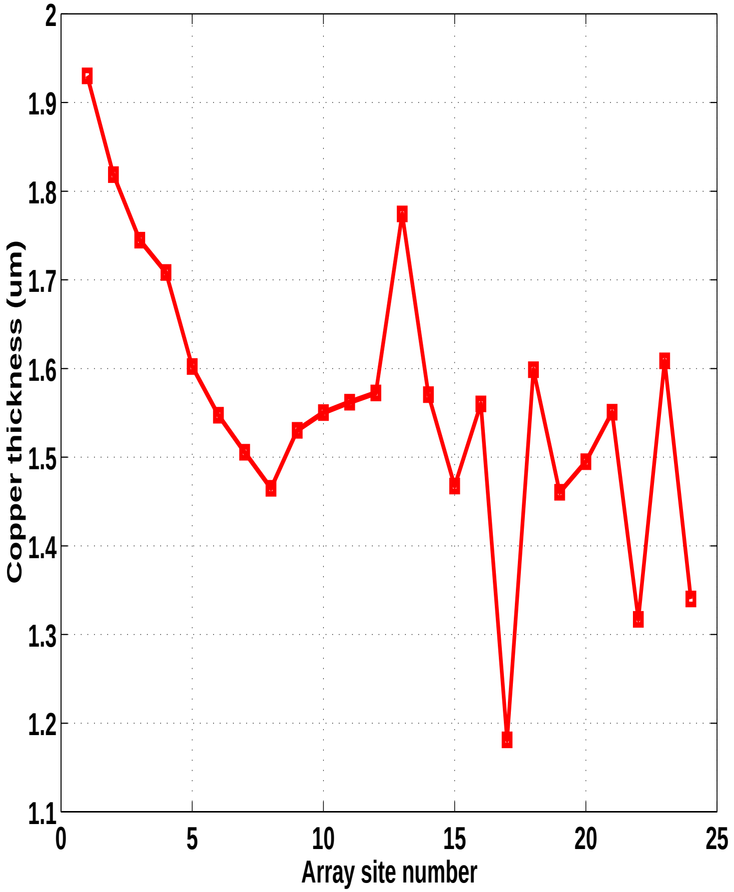
Array site numbers

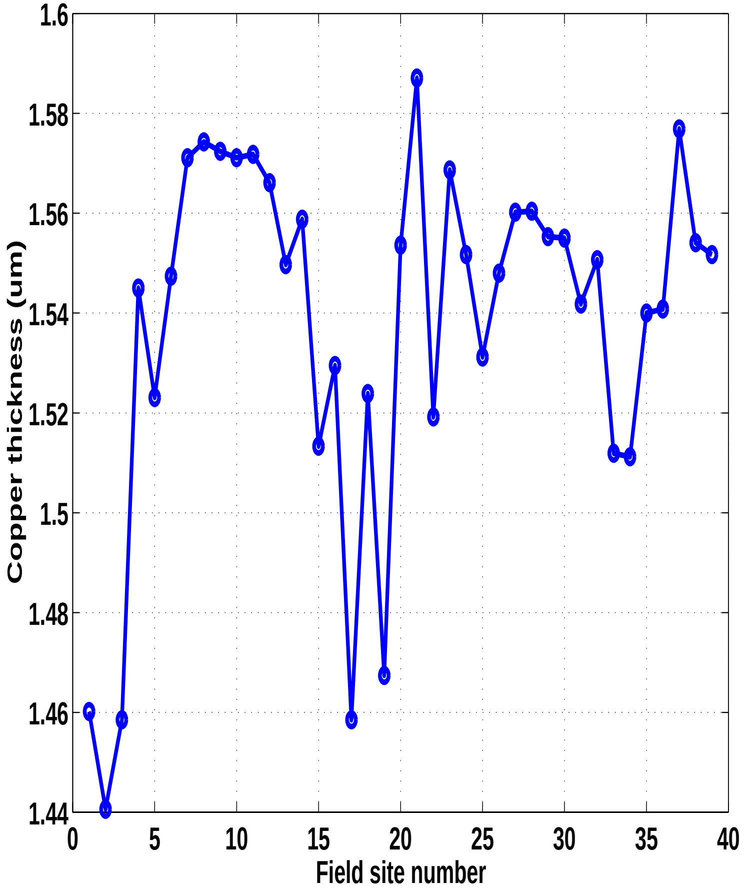


Field site numbers

- 24 array sites: all density and pitch structures
- 39 field sites: Used only in the extraction of step one model parameters

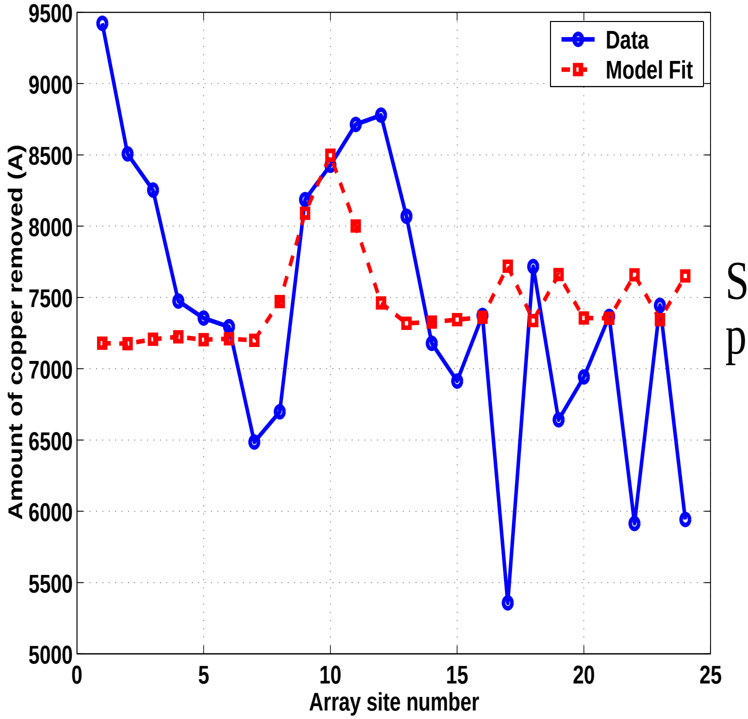
Initial Copper Thickness Deposited (measured)



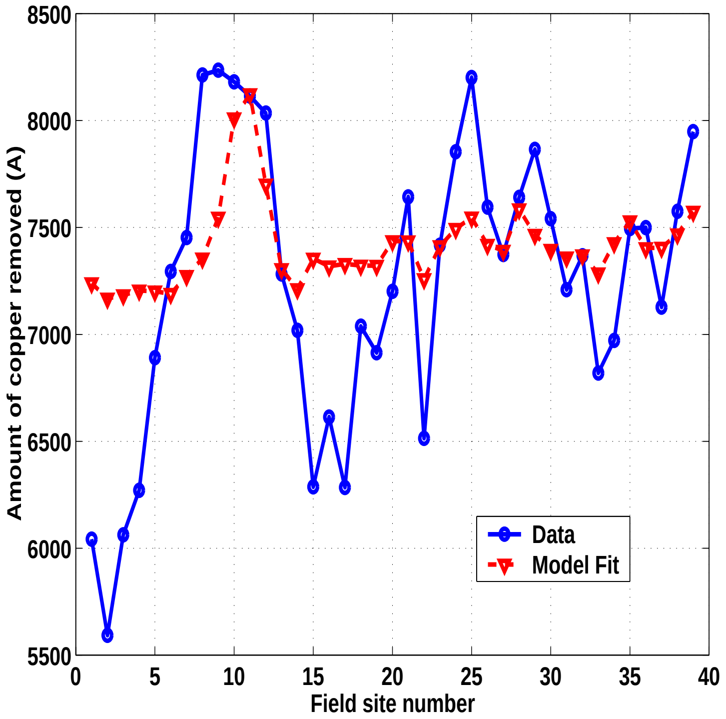


- Significant long range thickness variation (global heights) across the die

Model Fits vs. Data: Stage 1



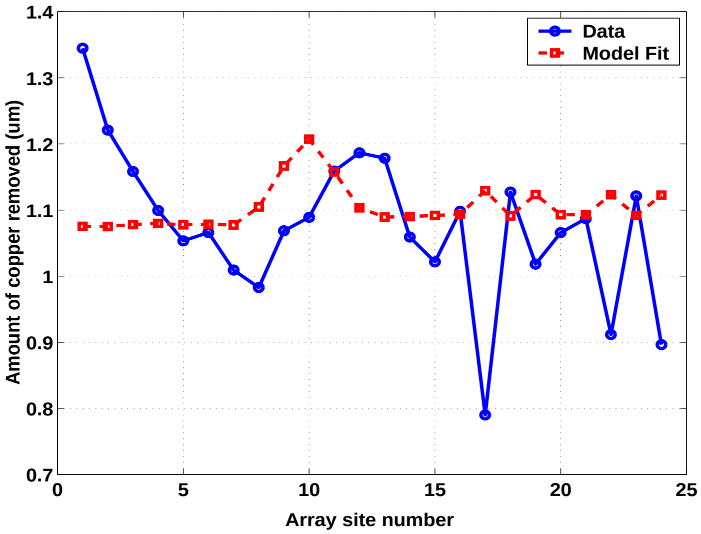
Step one polish time = 43 s



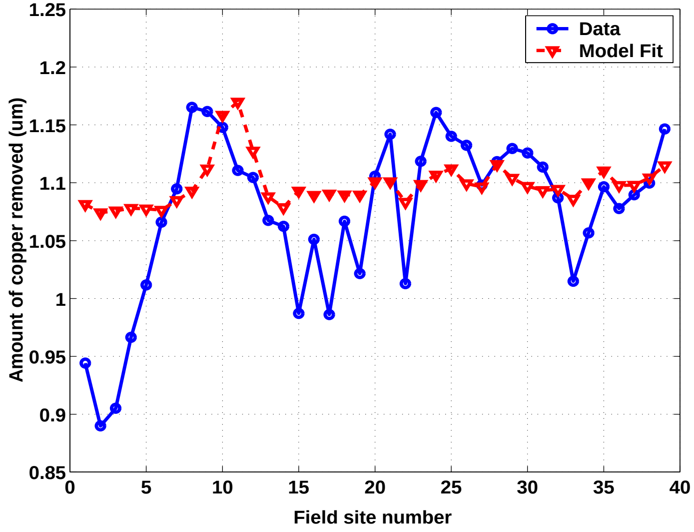
r_{cu1} (Å/s)					
a_1 (Å/s)	a_2 (Å)	τ_r (s)	L_{11} (µm)	H_{ex11} (Å)	RMS Error (Å)
249.5	3987	16.4	4893	negligible	817

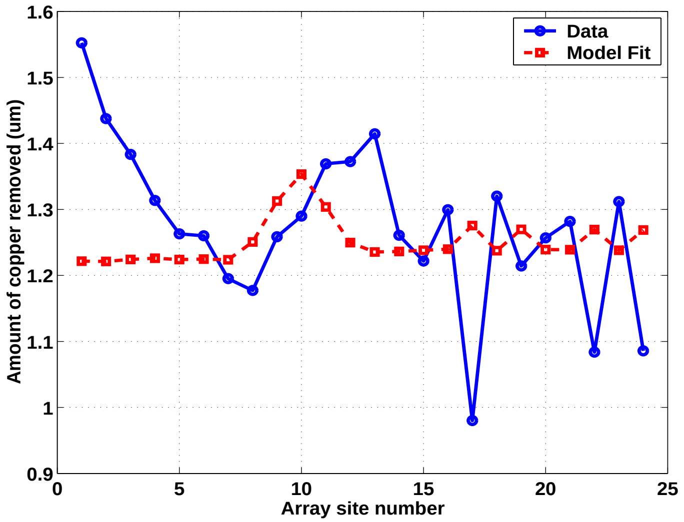
- Model does not fit the data well
  - ❑ Density-step-height model neglects long range thickness variation (global heights) introduced by electroplating

Model Fits vs. Data: Stage 1 (cont.)

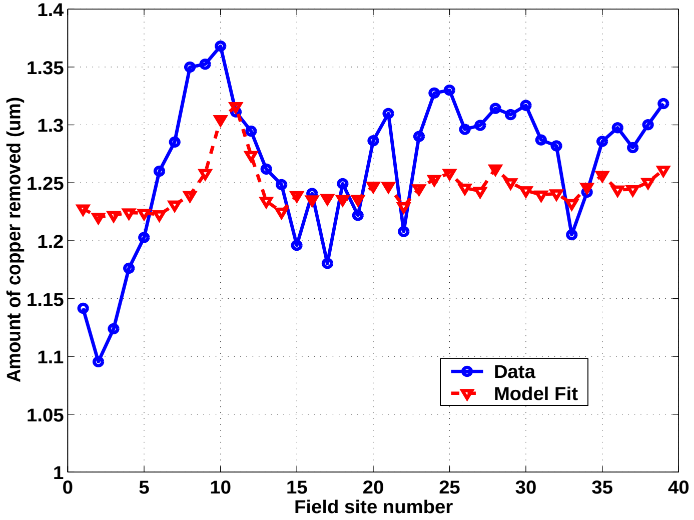


Step one polish time = 58 s

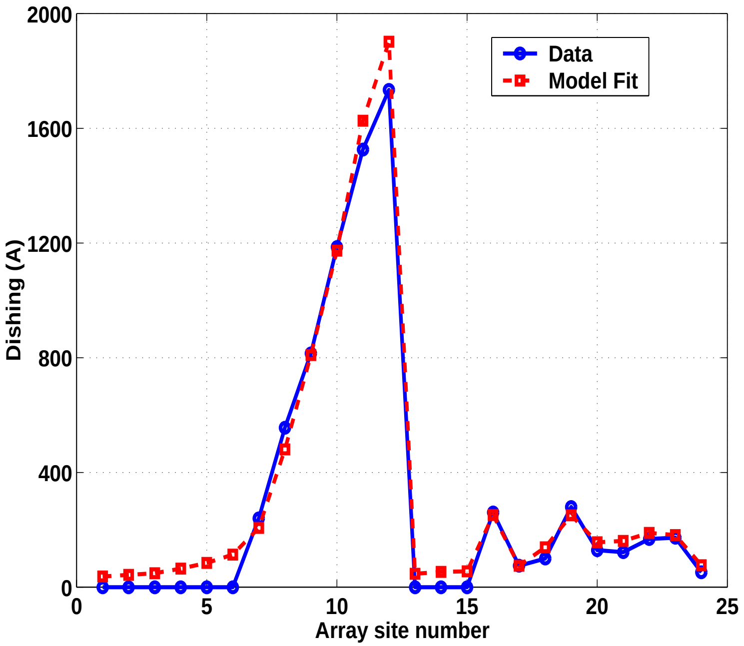




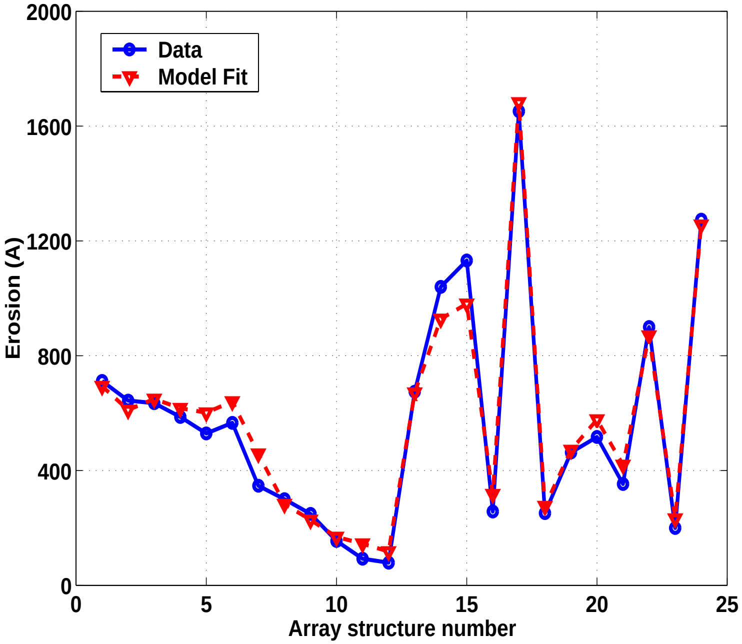
Step one polish time = 64 s



Model Fit vs. Experimental Data: Step 2 (edge rounding included in equations)



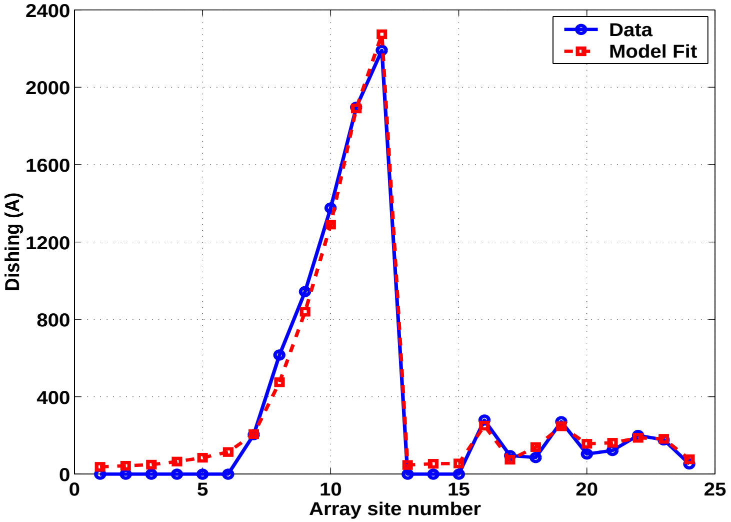
Step two polish time = 94 s



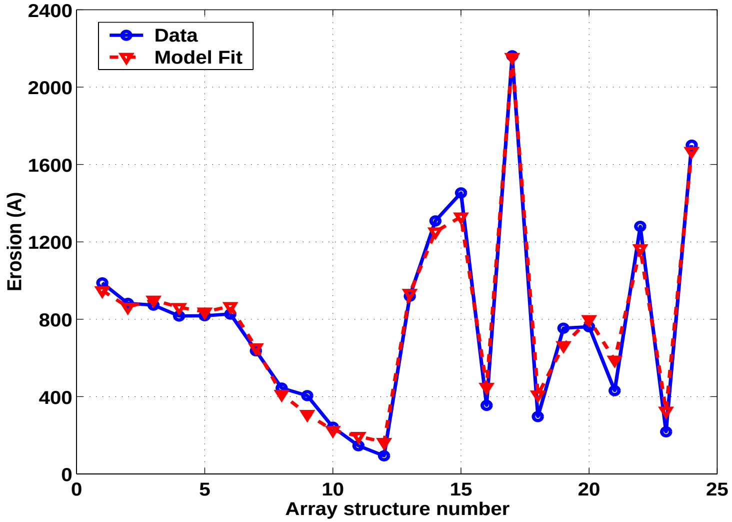
r_{cu2} (Å/s)	r_{ox2} (Å/s)	r_{b2} (Å/s)	L_{23} (µm)	d_{max2} (Å)			ψ_2		RMS Error (Å)
				B (Å)	α_2	β_2	C	s_c	
44	7.95	25.5	1596	159.3	0.467	0.468	N/A	N/A	120
44	2.36	7.58	2456	173.6	0.427	0.331	4.03	4.19	73

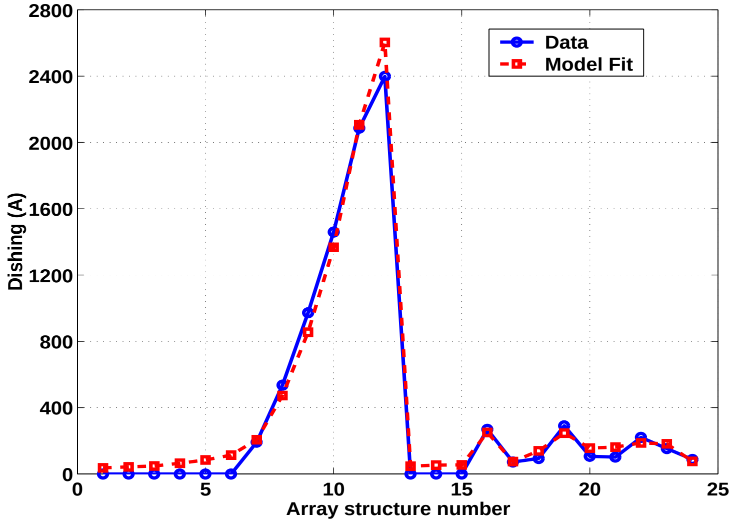
- Model fits the data very well
  - No global heights present in this step

Model Fit vs. Data: Step 2 (cont.)

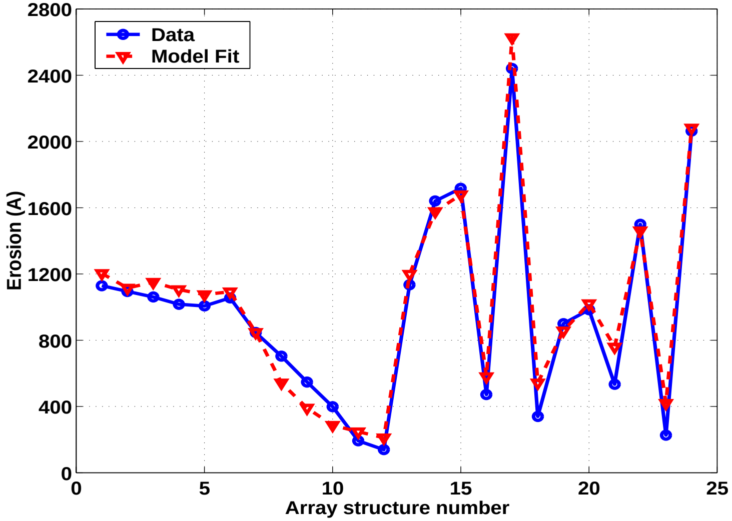


Step two polish time = 110 s

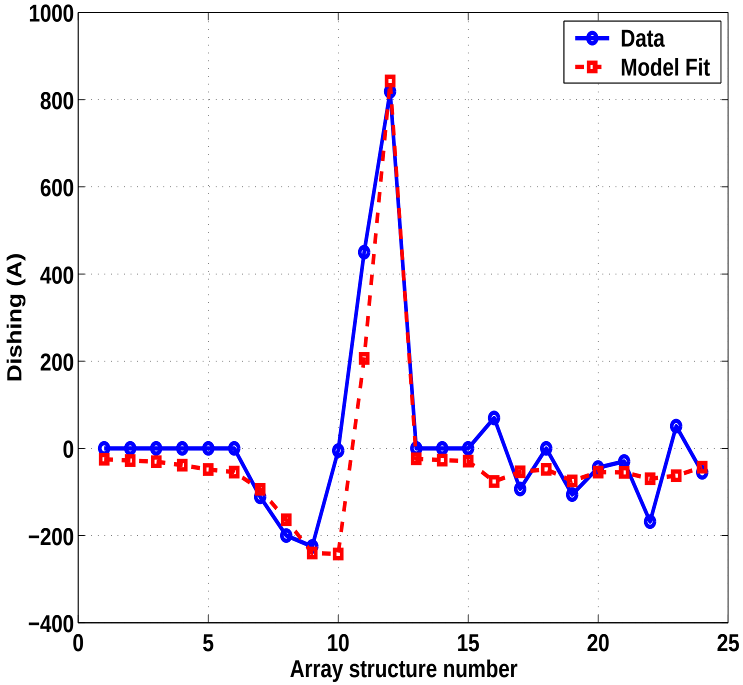




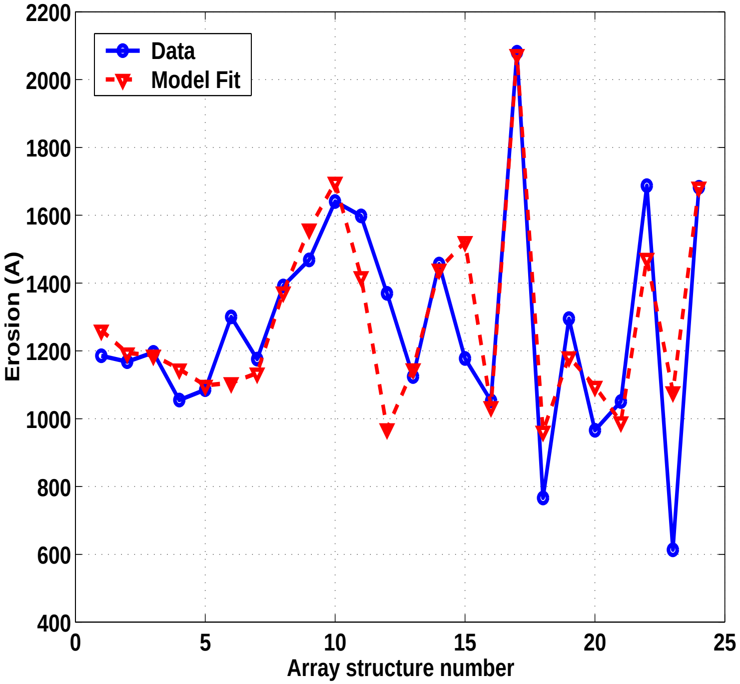
Step two polish time = 124 s



Model Fits vs. Data: Step Three (with edge rounding)



Polish time in step three = 20 s

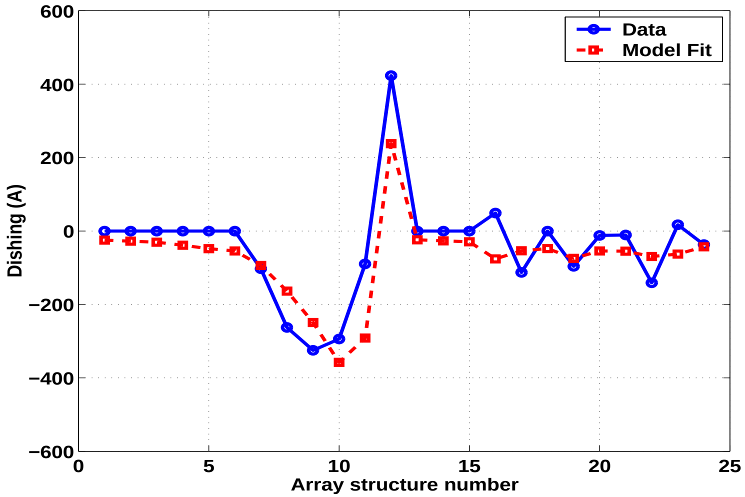


r_{cu3} (Å/s)	r_{ox3} (Å/s)	$*r_{b3}$ (Å/s)	L_{33} (µm)	d_{p3} (Å)			ψ		RMS Error (Å)
				A_3 (Å)	α_3	β_3	C_3	s_{c3}	
13.7	45.2	9.0	3707	54.5	0.896	0.014	N/A	N/A	137.0
9.0	20.0	4.0	4500	31.0	0.625	0.014	3.41	57.3	126

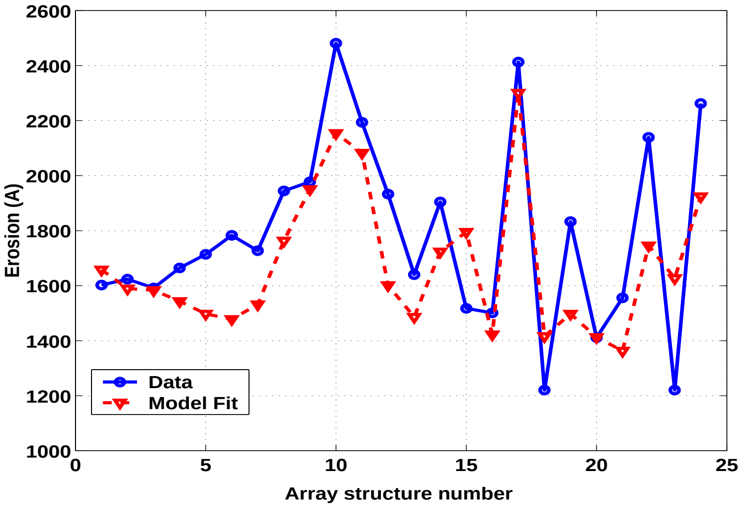
- Model fits data very well to within measurement error
  - No global heights present in this step

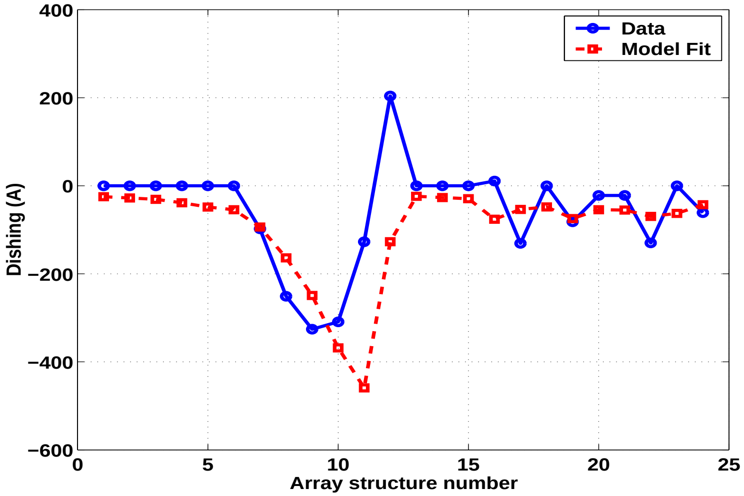
- Without edge rounding, the extracted blanket dielectric rate is too high

Model Fits vs. Data: Step Three (cont.)

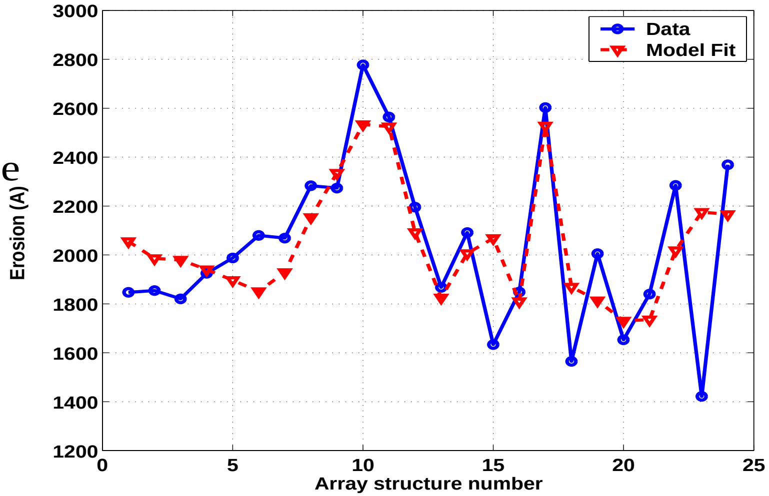


Polish time in step three = 35 s

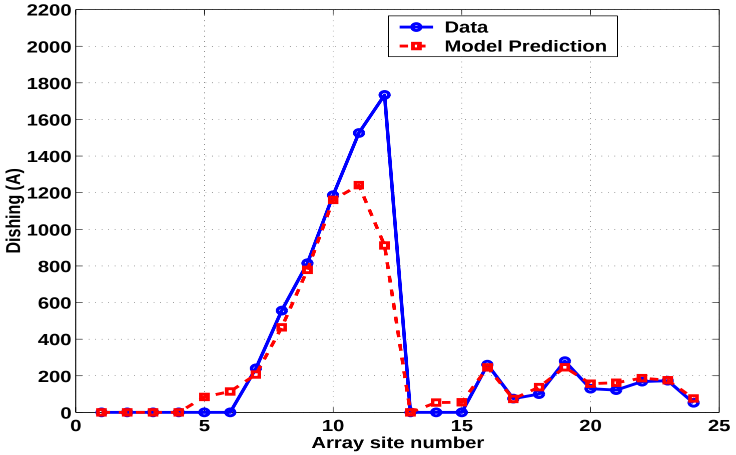




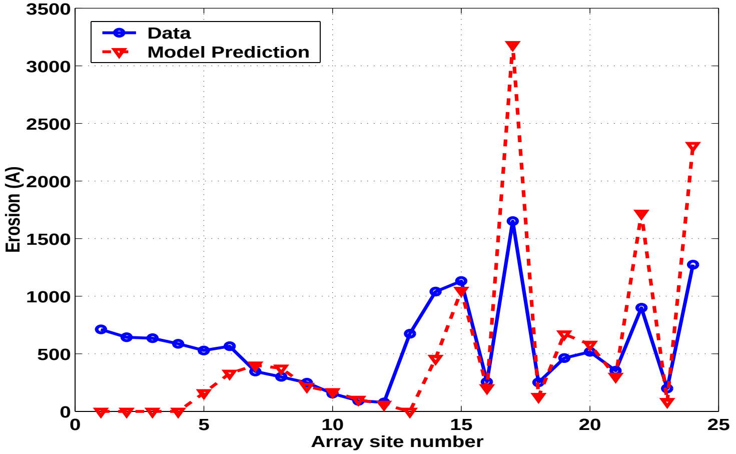
Polish time in step three = 50 s

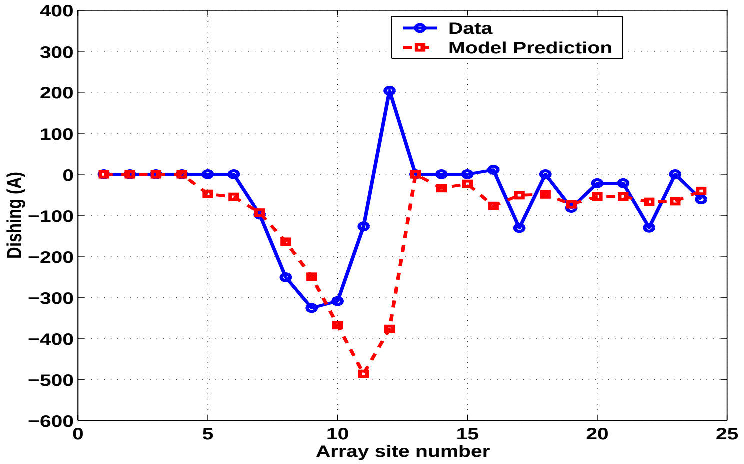


Verification of Extraction Procedure

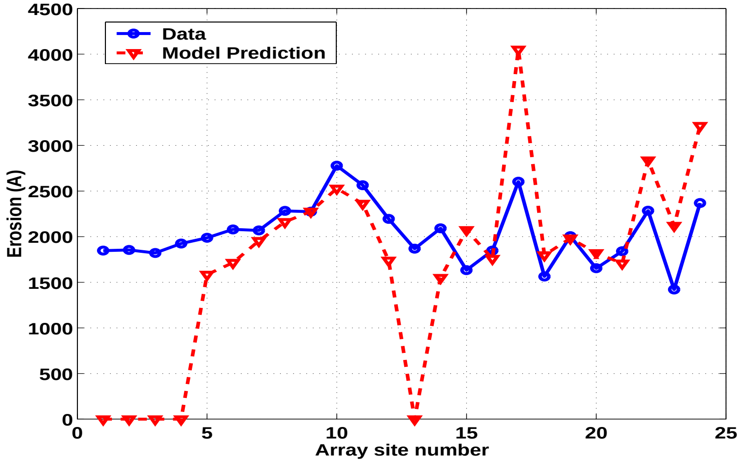


Nominal steps one and two polish



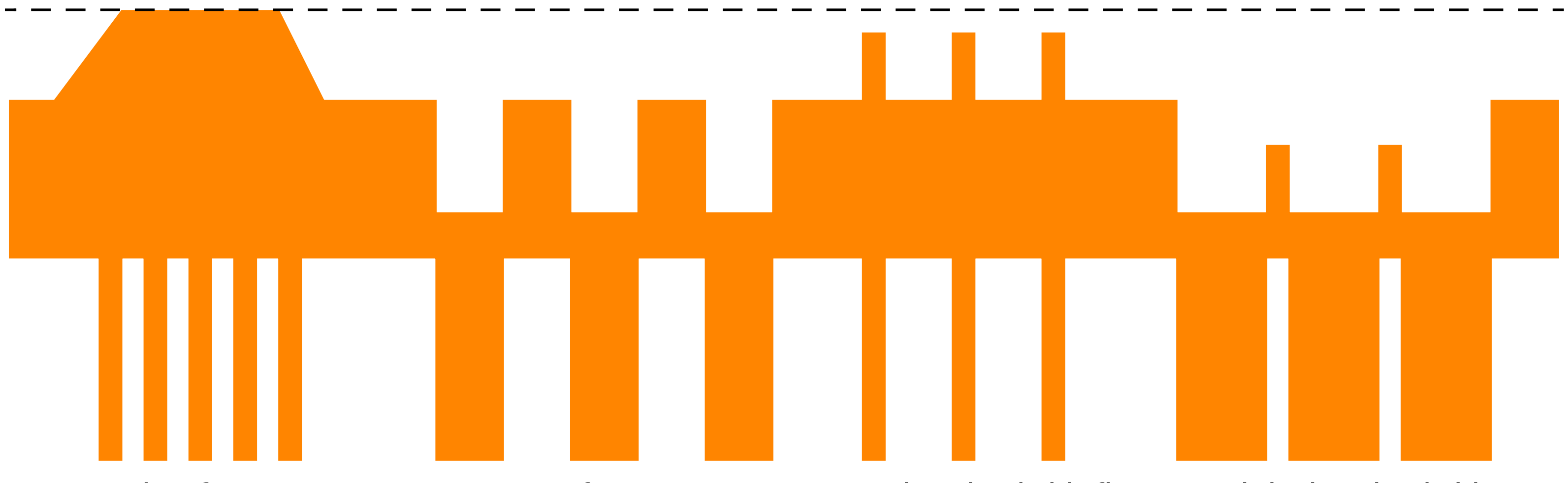


Nominal steps one and two polish plus 50 s step three polish

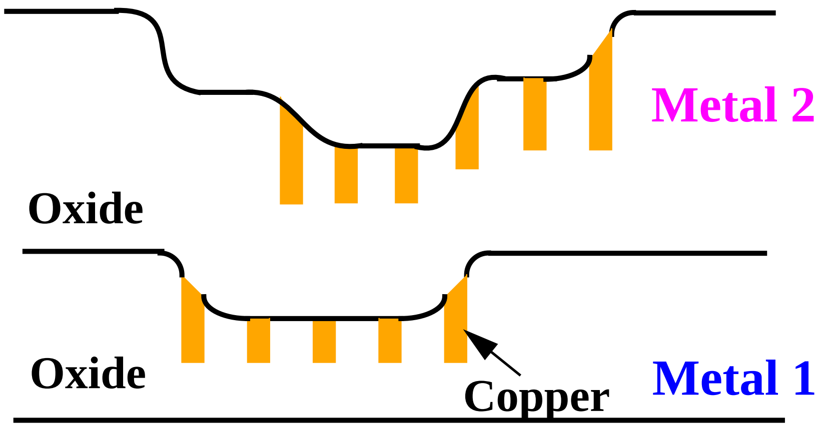


- Extraction errors in step one lead to inaccurate overpolish time simulation, and inaccurate erosion simulation

Density-Step-Height Model: Limitations



Bottom-up Fill Electroplating Technique



Multi Level

- Plating introduces initial global heights
- Excessive overpolish might cause global heights
- Dishing and erosion on metal level one can lead to global heights on higher metal levels

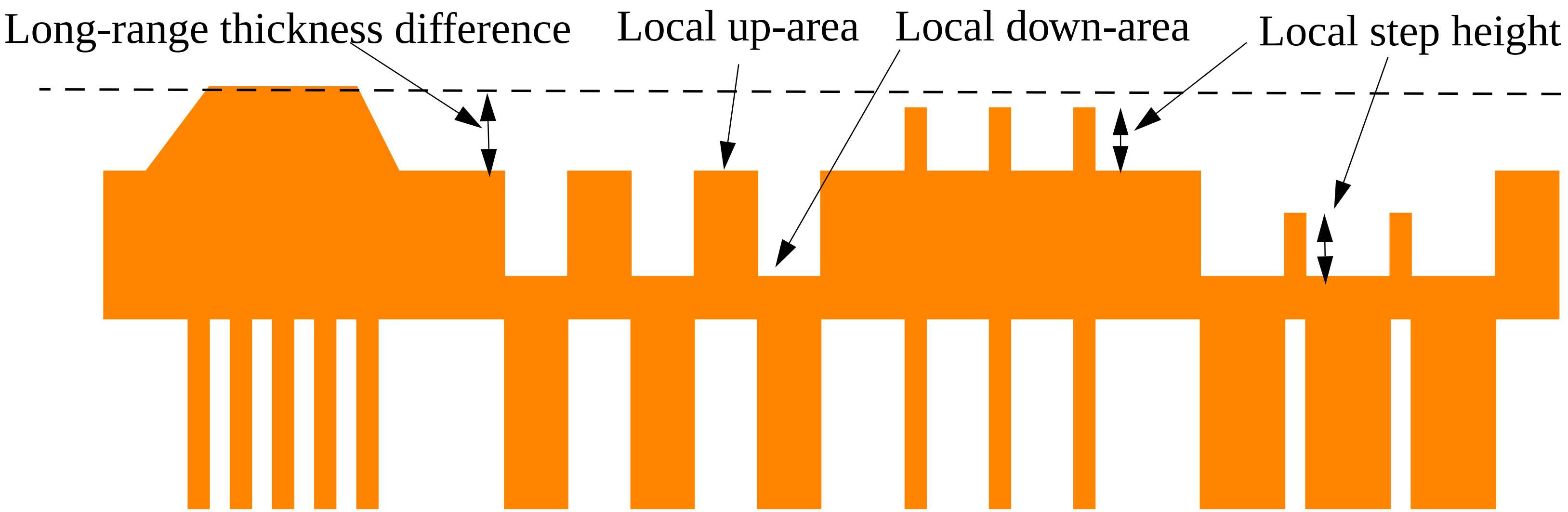
Issue: Global Heights (Hills and Valleys)

- ECD causes large initial global heights.
- As we polish, the global heights change, and bring about pressure redistribution.
- Excessive overpolish could lead to large global heights.
- Dishing and erosion on metal level one, cause global heights on metal level two.
- The issue of global heights, raises two questions:
  - Is there contact on up-areas?
  - If there is, what is the degree of contact?
- Global heights need to be taken into account for accurate dishing and erosion prediction.

Outline

- ■ Introduction to Copper CMP
- ✔ **Copper CMP Model Development**
  - ❑ Integrated Copper CMP Characterization and Modeling Methodology
  - ❑ Intrinsic Stages in Copper CMP
  - ❑ CMP Test Mask Design
  - ❑ Metrology
  - ❑ Dishing and Erosion Dependencies
  - ❑ Density-Step-Height Model
  - ✔ **Integrated Contact Mechanics and Density-Step-Height Model**
- ■ Chip-Scale Simulation
- ■ Conclusion and Future Work

Integrated Contact Mechanics and Density-Step-Height Model



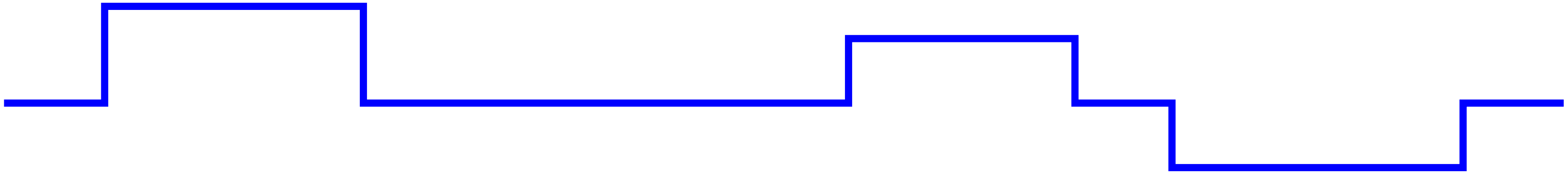
Long-range thickness difference

Local up-area

Local down-area

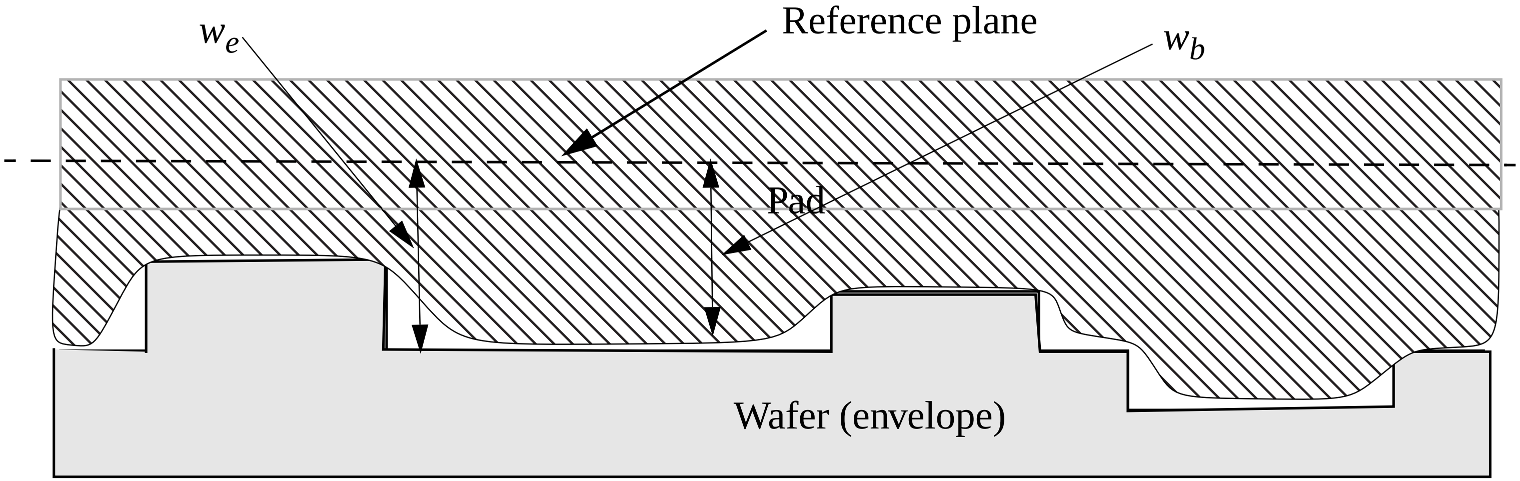
Local step height

Bottom-up fill electroplated profile for several arrays of lines



Envelop function for the electroplated profile shown in electroplated profile above

Integrated Model (cont.)



$$w_b(x,y) = k_c \iint_A \left(\frac{p_b(x,y)}{\sqrt{(x-\xi)^2 + (y-\eta)^2}} \right) d\xi d\eta$$

$$P_e = \begin{cases} P_1 - p_b & w_e = w_b \\ 0 & w_e > w_b \end{cases}$$

p_b: Perturbation pad pressure

w_b: Perturbation pad displacement

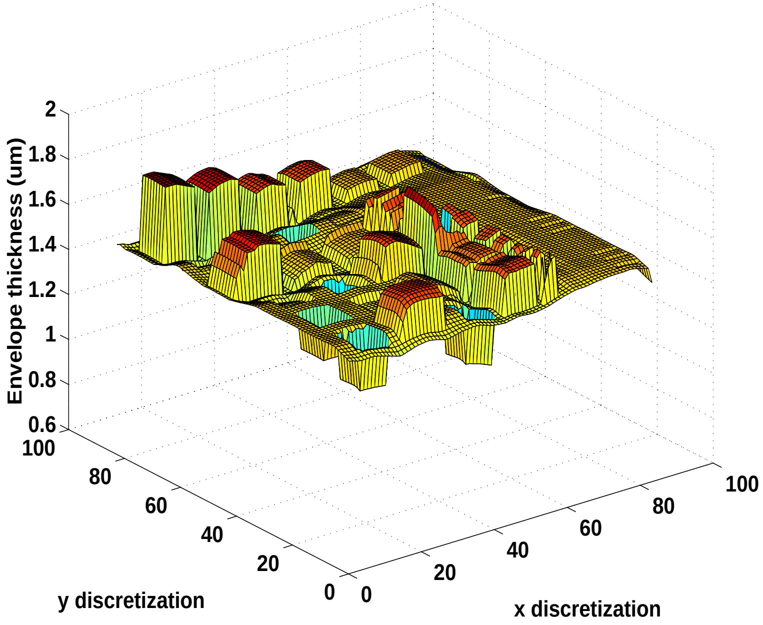
w_e: Pertubation wafer displacement

P_1: Applied pressure

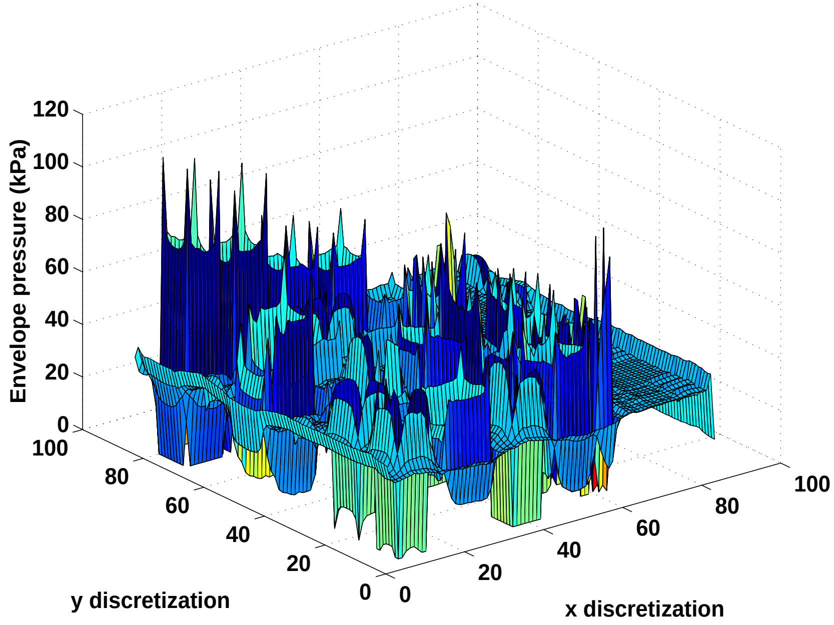
P_e: Envelope pressure (wafer pressure)

k_c: Contact factor (units of 1/kPa)

Initial Envelope and Envelope Pressure



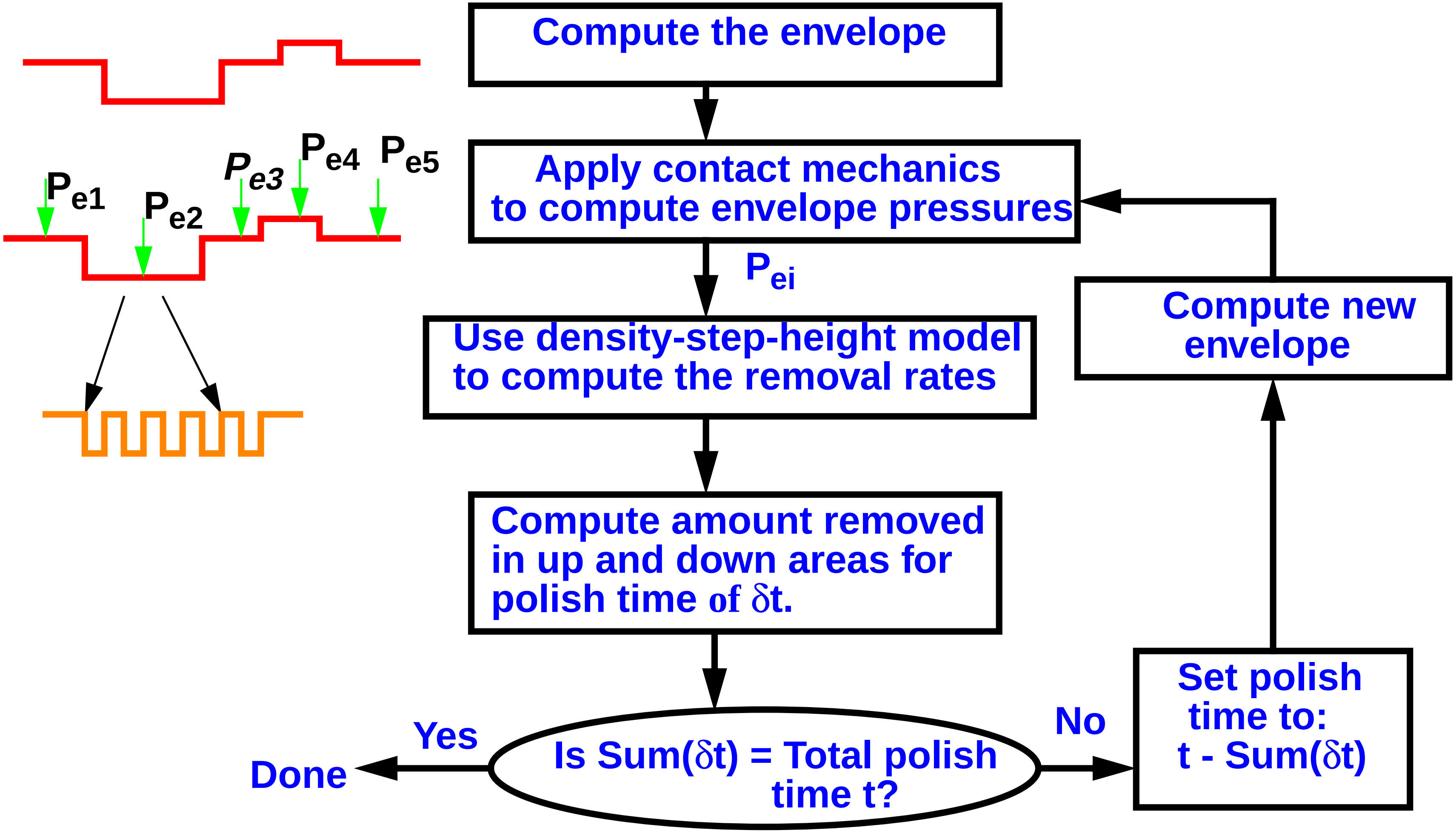
Initial Envelope



Initial Envelope Pressure

- The long range thickness variation or global height is captured by the envelope function
- The initial envelope pressure is not necessarily the applied pressure as assumed by the density-step-height model

Integrated Model (cont).



Compute the envelope

Apply contact mechanics to compute envelope pressures

Use density-step-height model to compute the removal rates

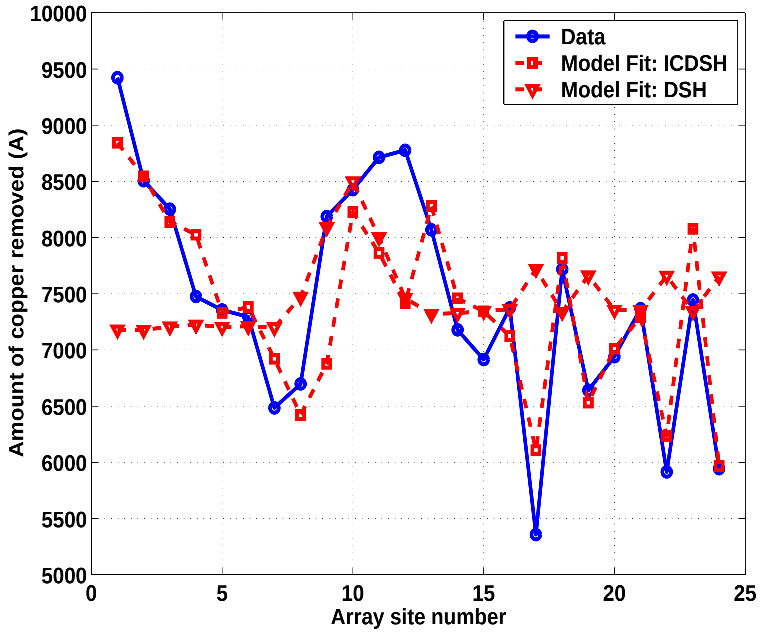
Compute amount removed in up and down areas for polish time of δt.

Is Sum(δt) = Total polish time t?

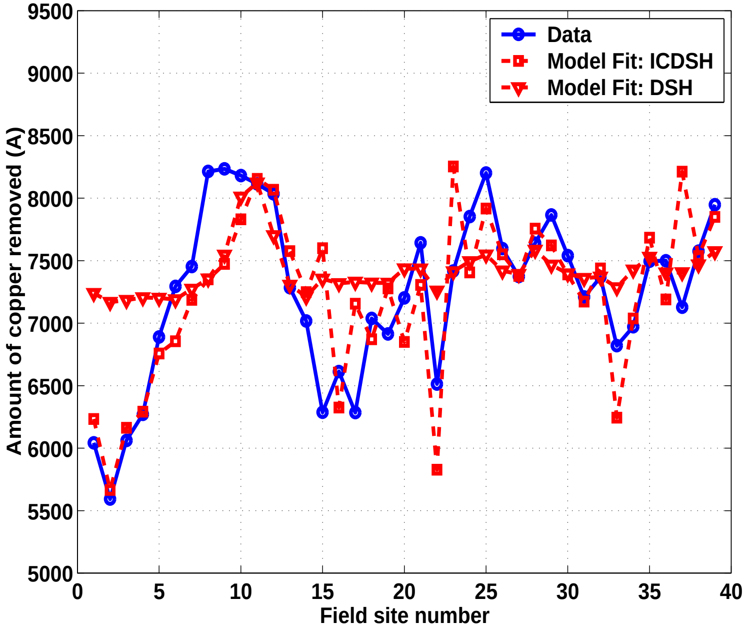
Set polish time to: t - Sum(δt)

Compute new envelope

Integrated Model Fits vs. Data: Step 1 Process



Polish time in step one = 43 s



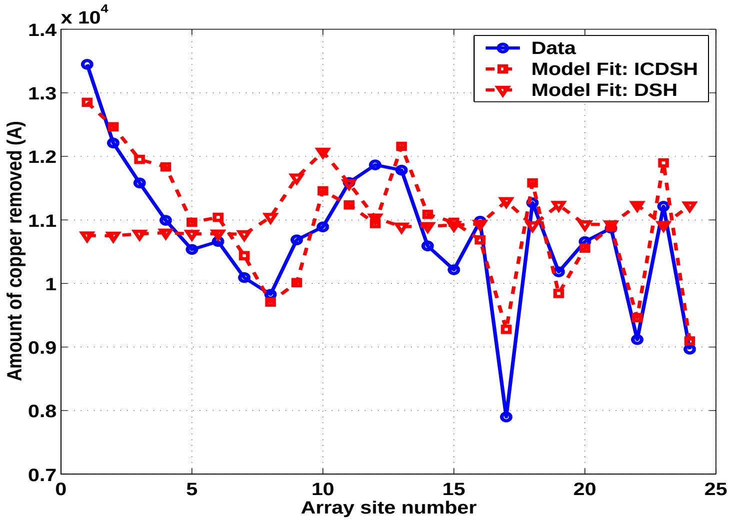
r_{cu1} (Å/s)			L_{11} (µm)	k_{c1} (1/kPa)	H_{ex11} (Å)	RMS Error (Å)
a_1 (Å/s)	a_2 (Å)	τ_r (s)				
249.5	3986	16.4	2758	9.95	negligible	569
249.5	3986	16.4	4893	N/A	negligible	817

- ICDSH fits data better than DSH

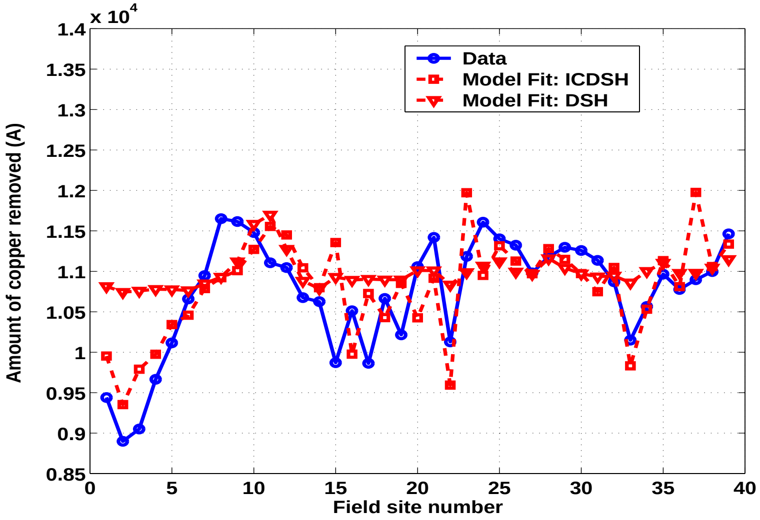
- ICDSH: Integrated contact mechanics and density-step-height model

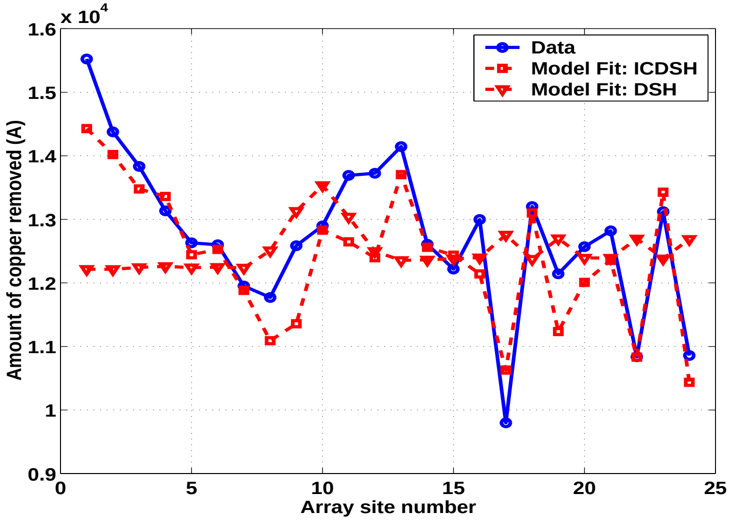
- DSH: Density-step-height model

Integrated Model Fits vs. Data: Step 1 Process (cont.)

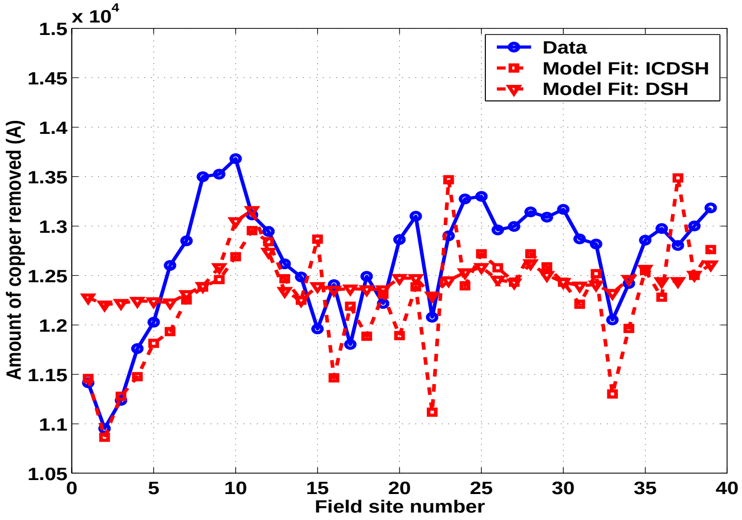


Polish time in step one = 58 s

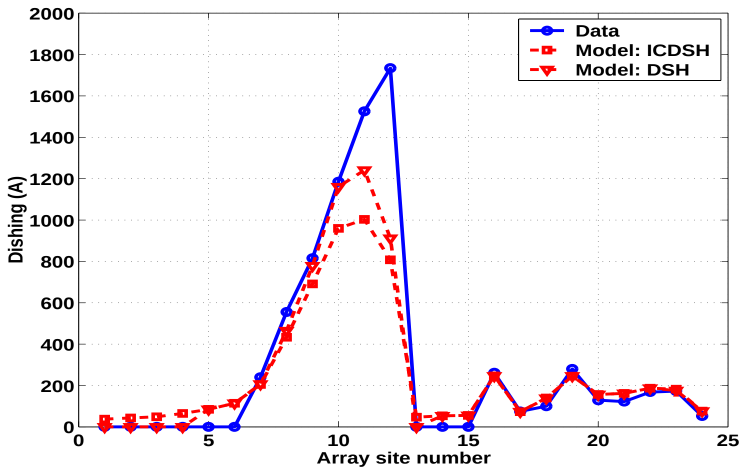




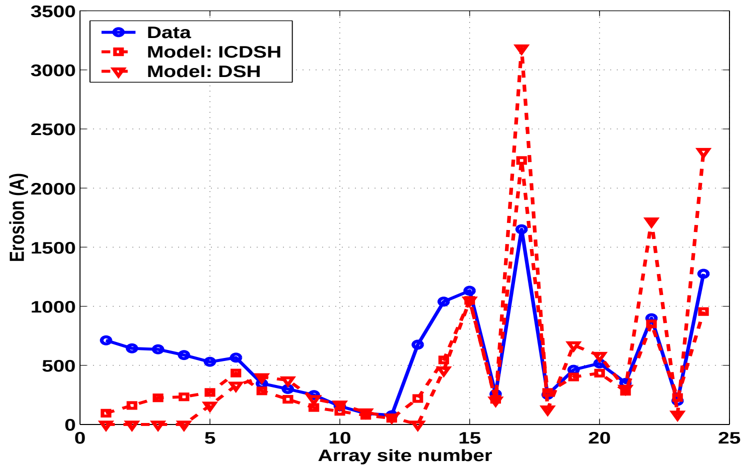
Polish time in step one = 64 s

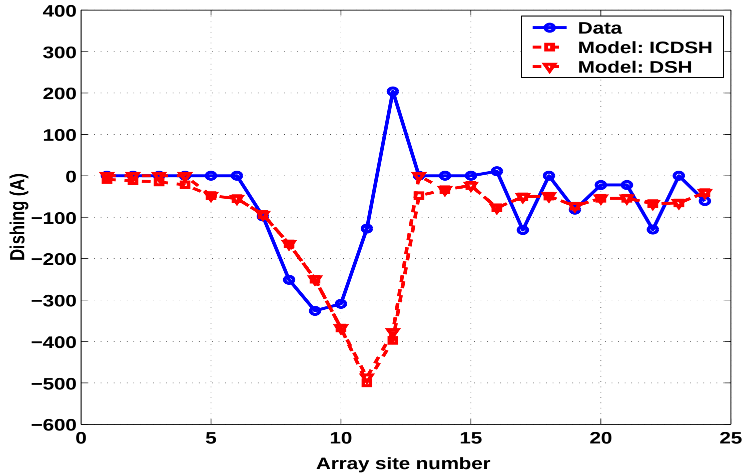


Integrated Model: Verification of Extraction

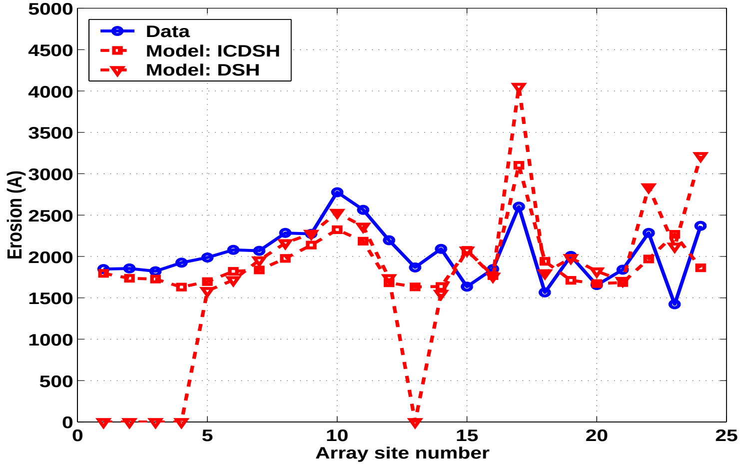


Nominal steps one and two polish





Nominal steps one and two polish plus 50 s step three polish



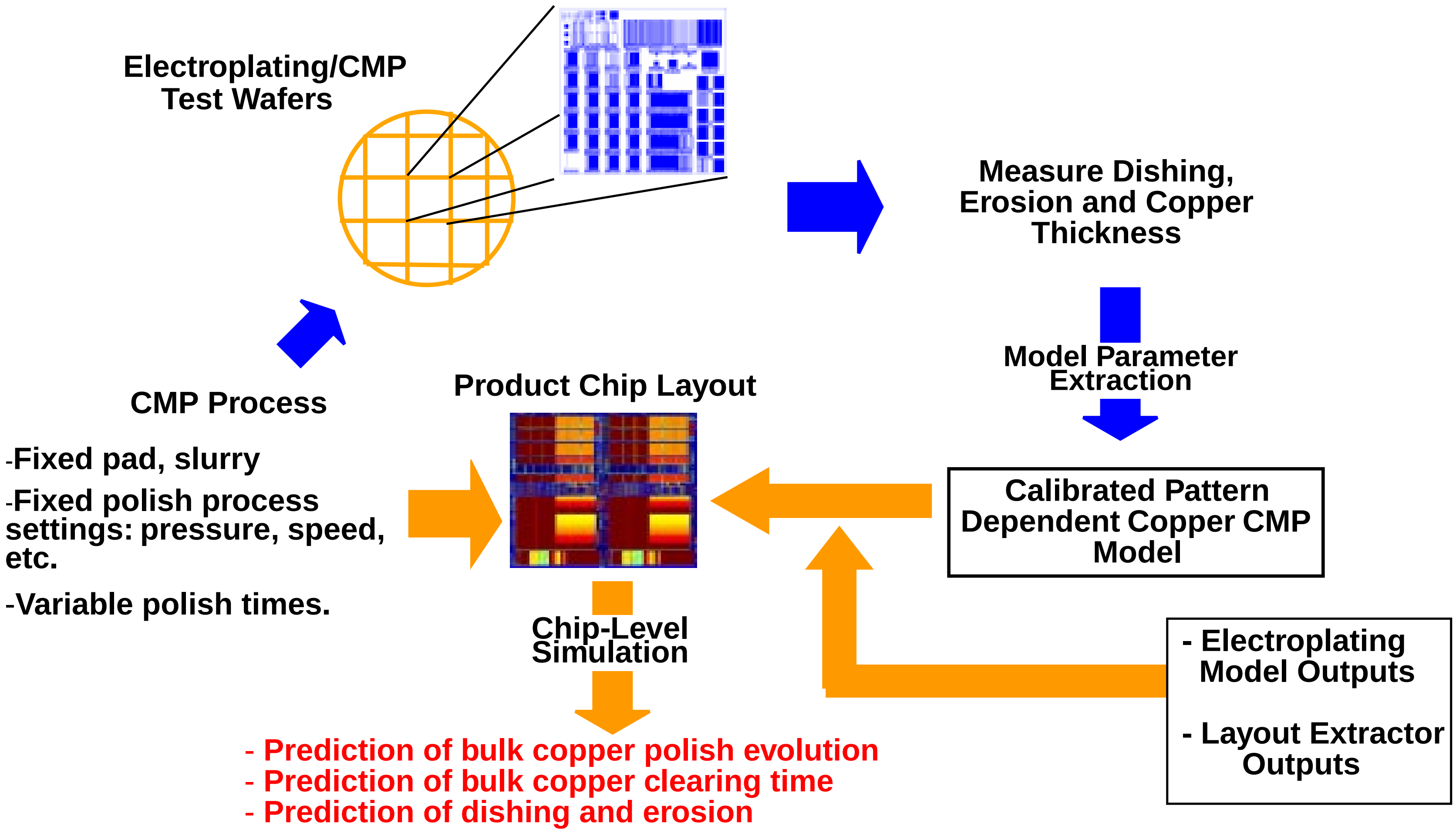
- Simulated overpolish times for ICDSH closer to actual overpolish times
    - ISDSH simulated erosion closer to data than DSH simulated erosion

Outline

- ■ Introduction to Copper CMP
- ■ Copper CMP Model Development
- ✔ **Chip-Scale Simulation**
- ■ Conclusion and Future Work

Integrated Electroplating and CMP Chip-Scale Simulations

Copper CMP Modeling Methodology



Electroplating/CMP Test Wafers

Measure Dishing, Erosion and Copper Thickness

Model Parameter Extraction

Calibrated Pattern Dependent Copper CMP Model

- Electroplating Model Outputs

- Layout Extractor Outputs

Product Chip Layout

CMP Process

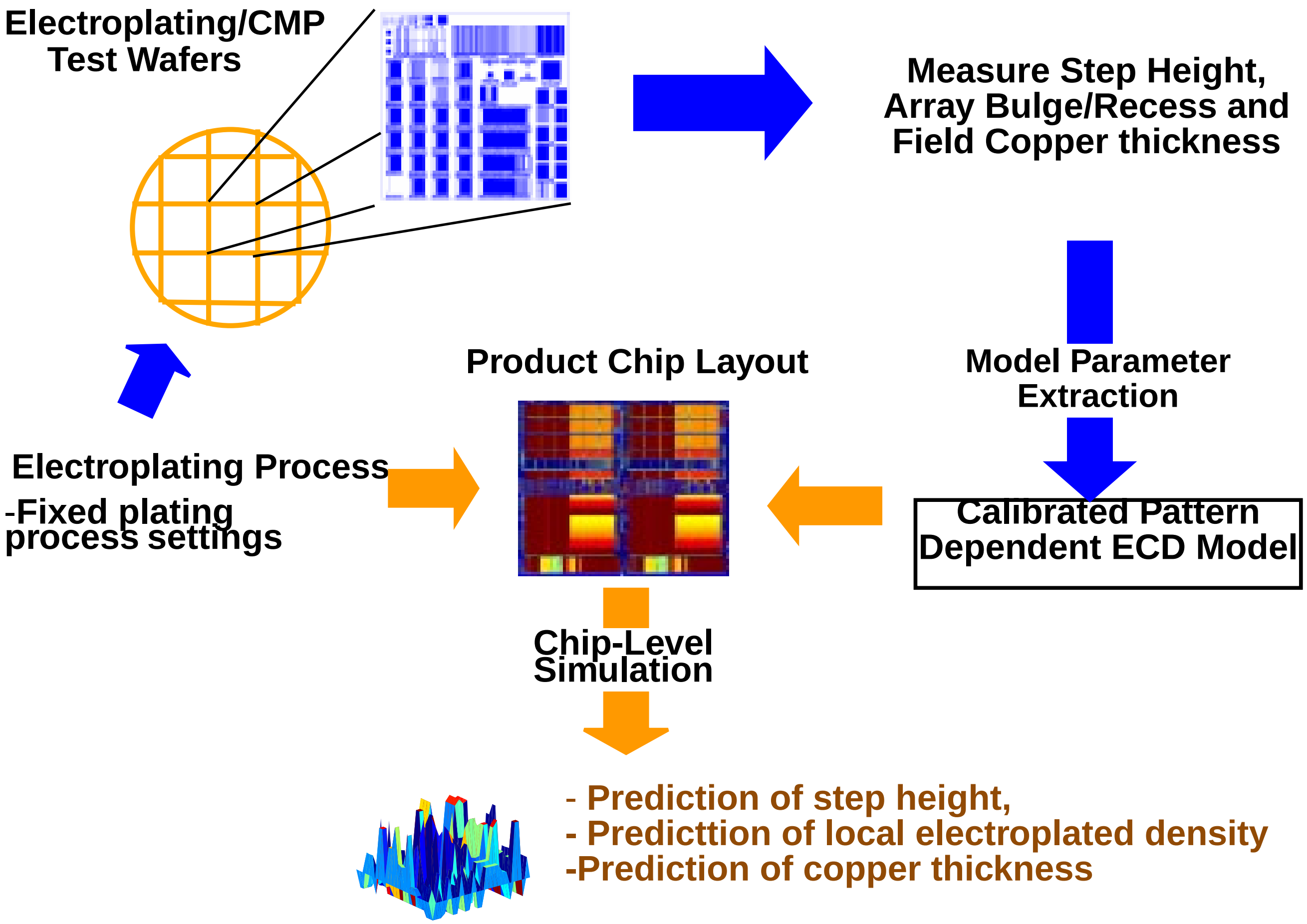
- **Fixed pad, slurry**
- **Fixed polish process settings: pressure, speed, etc.**
- **Variable polish times.**

Chip-Level Simulation

- **Prediction of bulk copper polish evolution**
- **Prediction of bulk copper clearing time**
- **Prediction of dishing and erosion**

Integrated Electroplating and CMP Chip-Scale Simulations (cont.)

Electroplating Modeling Methodology



Electroplating/CMP
Test Wafers

Measure Step Height,
Array Bulge/Recess and
Field Copper thickness

Model Parameter
Extraction

Calibrated Pattern
Dependent ECD Model

Product Chip Layout

Electroplating Process

-Fixed plating
process settings

Chip-Level
Simulation

- Prediction of step height,
- Predicttion of local electroplated density
-Prediction of copper thickness

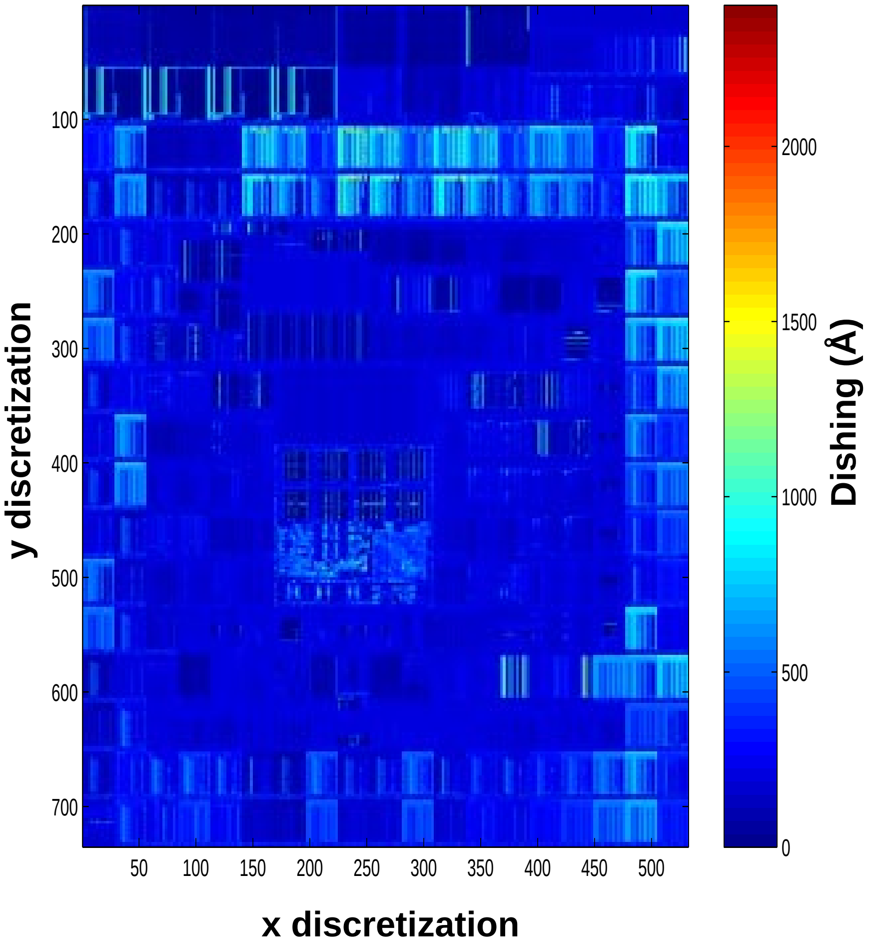
Accuracy of Simulator

- Three step copper CMP process performed on layout not used in copper CMP model and copper electroplating model calibration.
- Use simulator to predict the dishing and erosion across the entire die, for the new layout
- Compare predicted results to measured results, at specific points on the die.

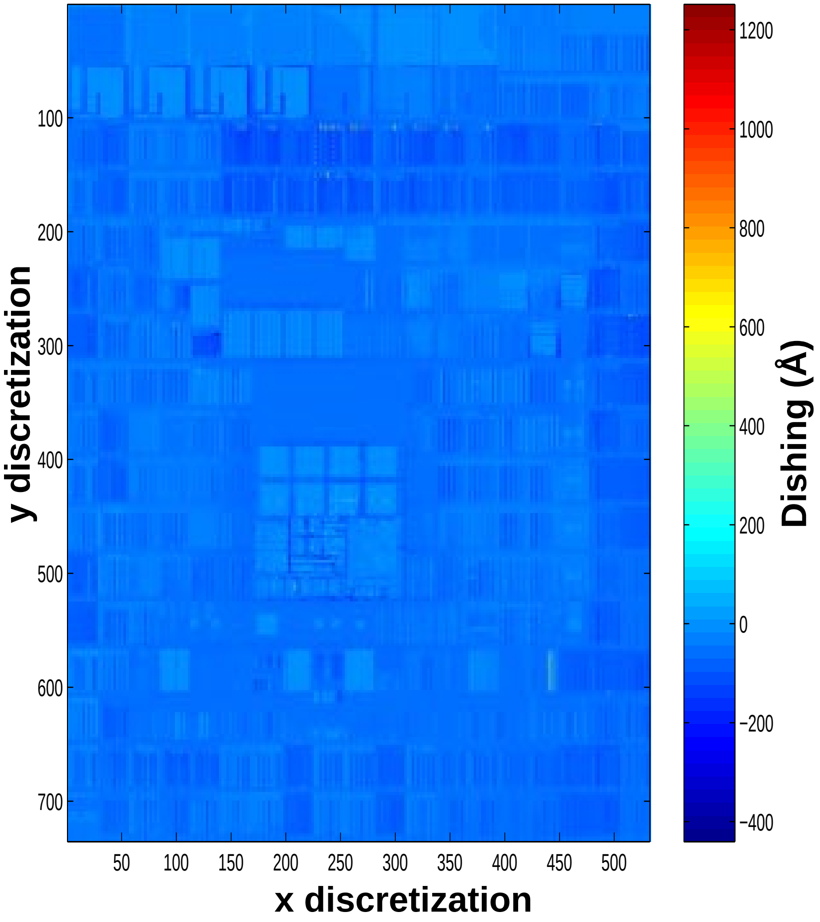
Step #	Platen #	Pad	Slurry	Down force (psi)	Speed (rpm)
1	1	Stacked	EPC-5001	5	63
2	2	Stacked	EPC-5001	2	43
3	3	Stacked	10K-1	3	100

Wafer #	Step one	Step two	Step three
Z-1	63	102	55
Z-2	63	117	0

Die Level Predicted Results: Dishing

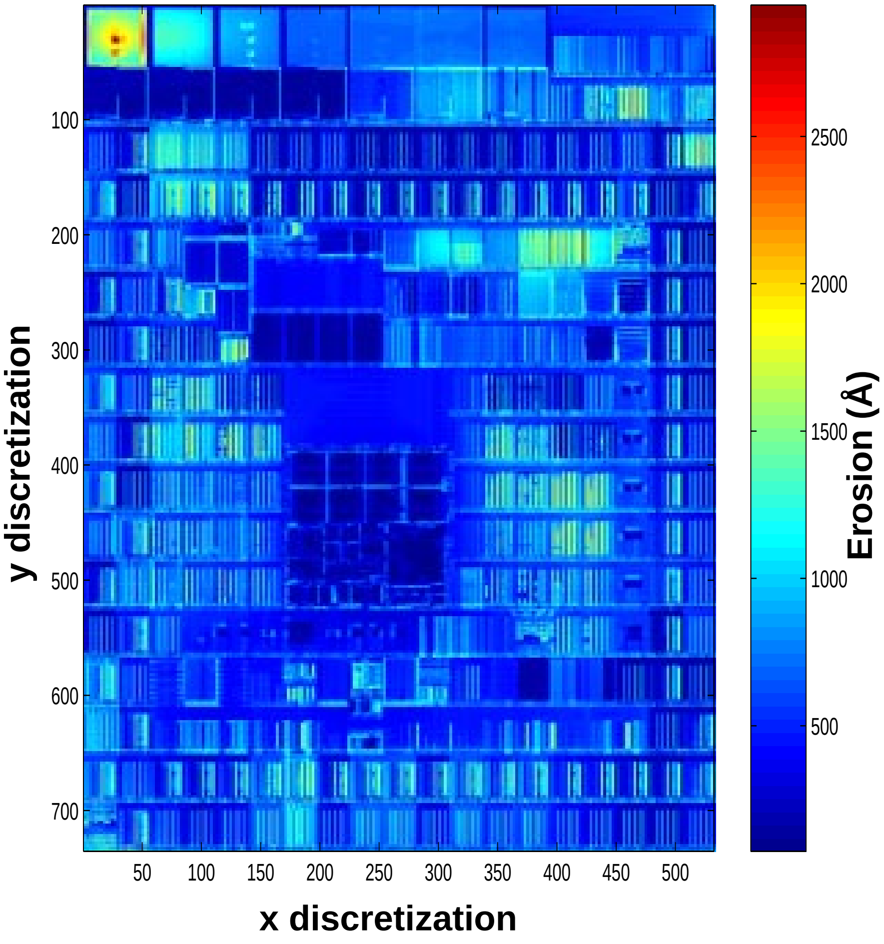


Dishing after step two for wafer Z-1

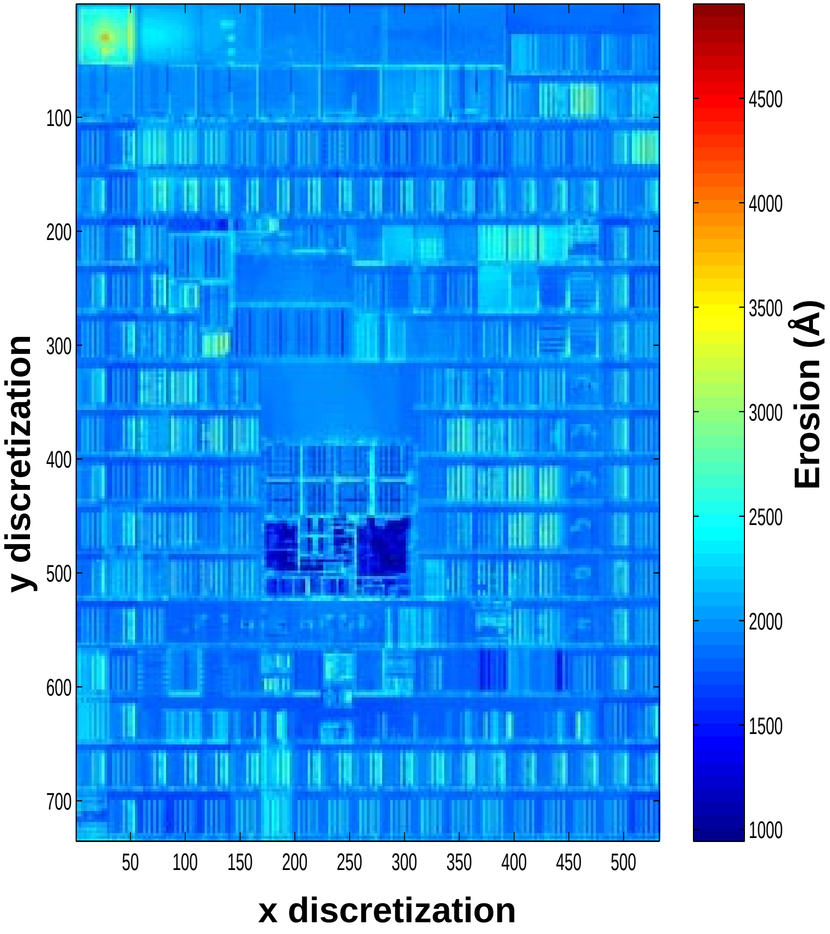


Dishing after step three for wafer Z-1

Die-Level Predicted Results: Erosion

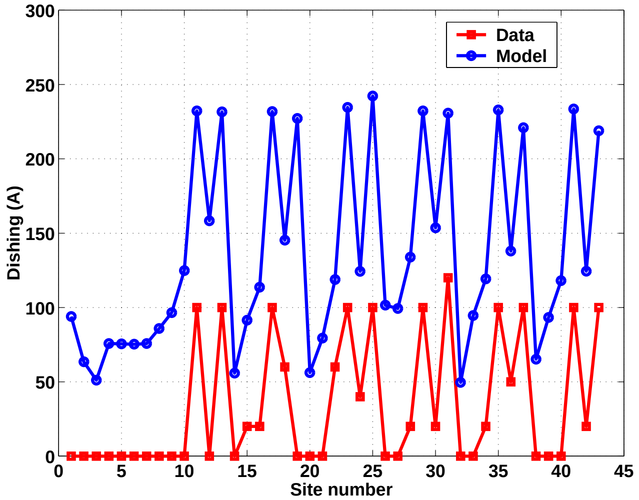


Erosion after step two for wafer Z-1

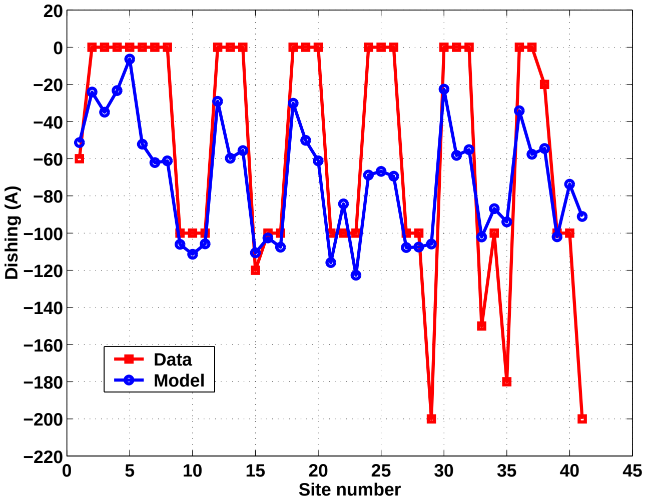


Erosion after step three for wafer Z-1

Predicted Results vs. Measured Data

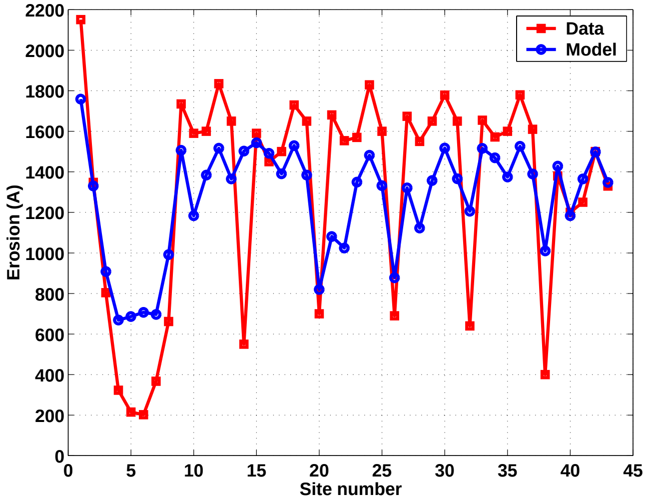


Dishing

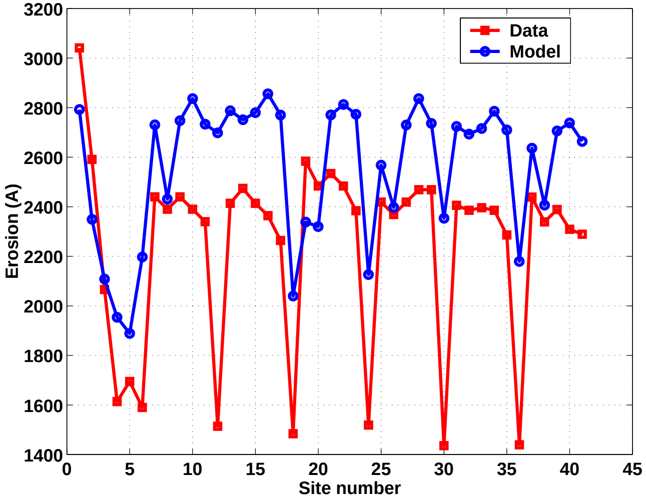


After step two for wafer Z-1

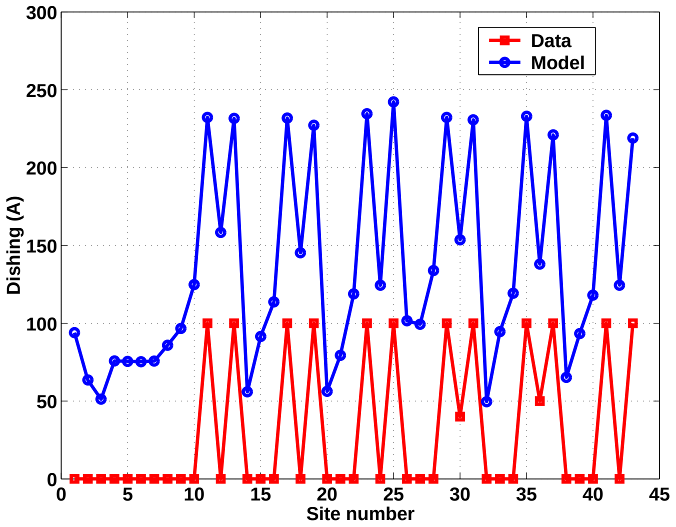
After step three for wafer Z-1



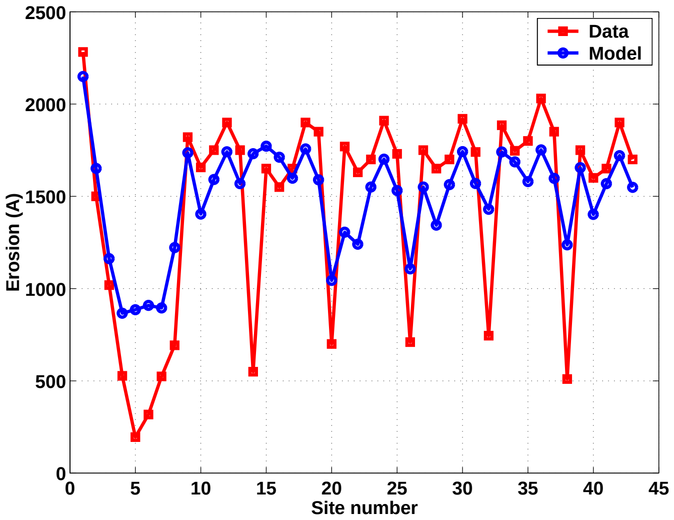
Erosion



Predicted Results vs. Measured Data (cont).



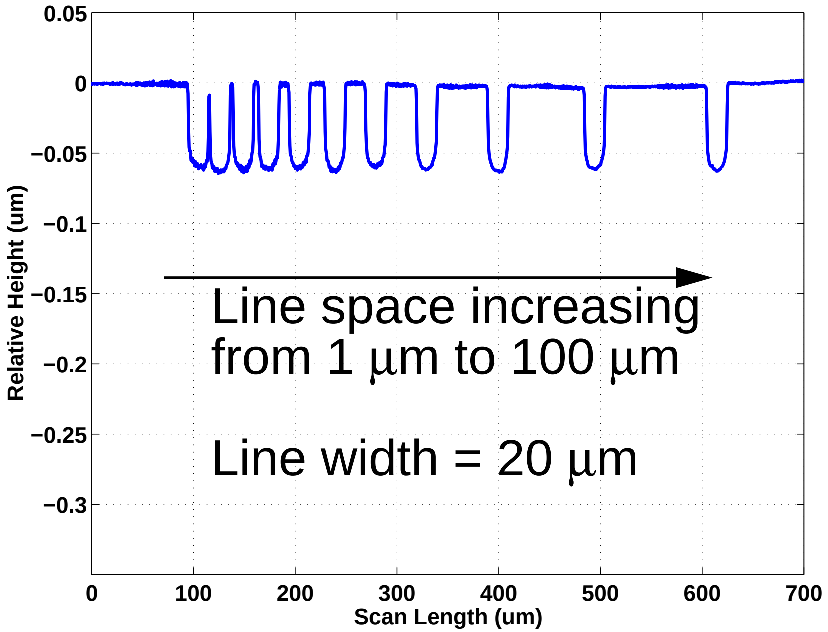
Dishing after step two for wafer Z-2



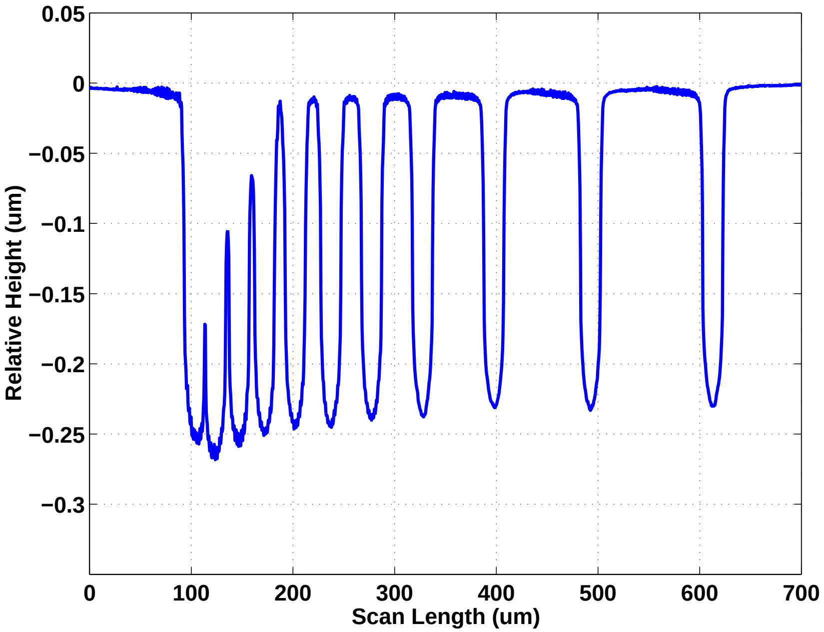
Erosion after step two for wafer Z-2

- Predicted results follow trend in measured data reasonably well, and are reasonably close to the measured data
- Simulator shows great promise for:
  - Predicting dishing and erosion on random layouts
  - Assessing the effectiveness of dummyfills in minimizing within-die non-uniformity
  - Detect clearing problems in multi-level metallization schemes

Defining Dishing in an array with Varying Line Space



Polish time = 98 s (Just cleared bulk and barrier)



Polish time = 114 s (overpolish)

- What is dishing when the line space in an array varies?
- Does it make sense to talk about dishing in such a case, or should we now talk about the copper thickness loss in the trench?

Conclusion and Future Work

- A chip-scale pattern dependent copper CMP model has been developed
- A comprehensive model calibration methodology has been developed
- A simulator (based on model equations) has been developed. It can be used to:
  - Predict dishing and erosion across an entire chip
  - Assess the effectiveness of dummification in minimizing within-die non-uniformity
  - Detect any bulk copper clearing problems in multi-level metallization schemes
  - Aid in developing smart interconnect design rules
- Future work needed includes:
  - Incorporate wafer level variation into the model
  - Incorporate process variation (day to day, lot to lot, etc.) into the model
  - Study relationships between model parameters and process parameters (down force, table speed, pad stiffness, slurry type, slurry flow rate, etc.)

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