# Chip-Scale Modeling of Copper Plating Pattern Dependencies

**Tae Park and Duane Boning**

Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology

NSF/SRC Engineering Research

Center for Environmentally Benign Semiconductor Manufacturing

TeleSeminar

February 20, 2003

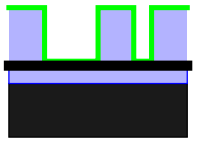


# Motivation: Pattern Dependent Problems in Copper Interconnects

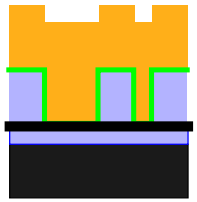
## Damascene Process

1. Oxide Deposition

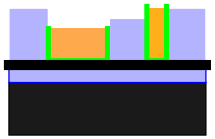
2. Oxide Pattern/Etch



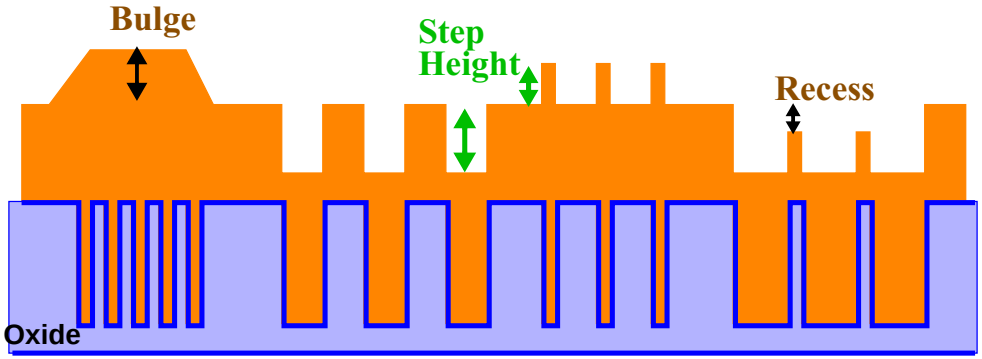
3. Barrier Layer Dep.



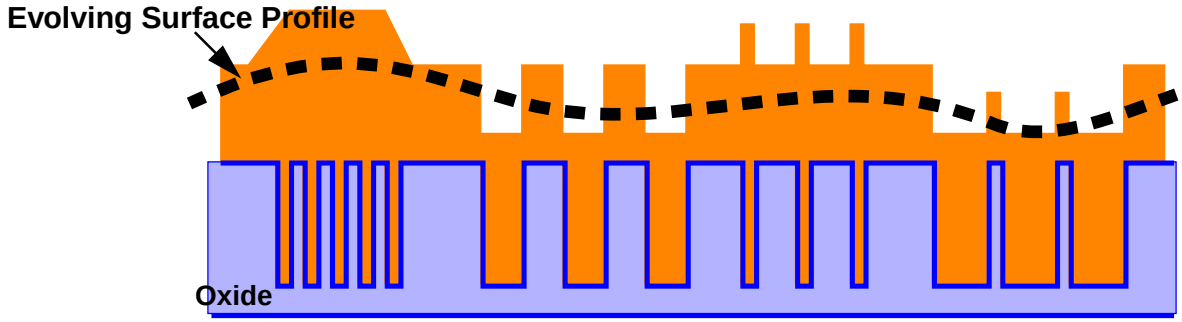
4. Electroplating

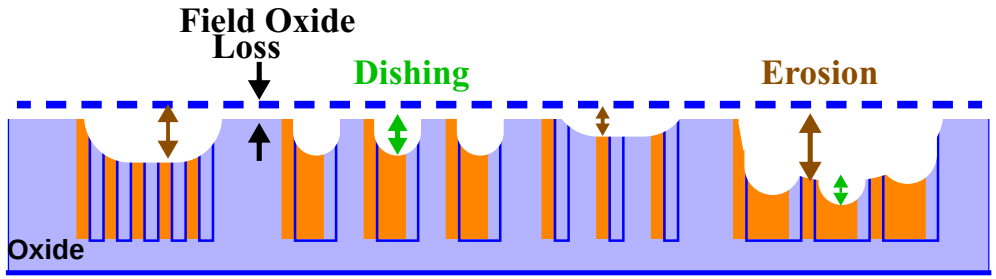


5. CMP




Electroplating Problems



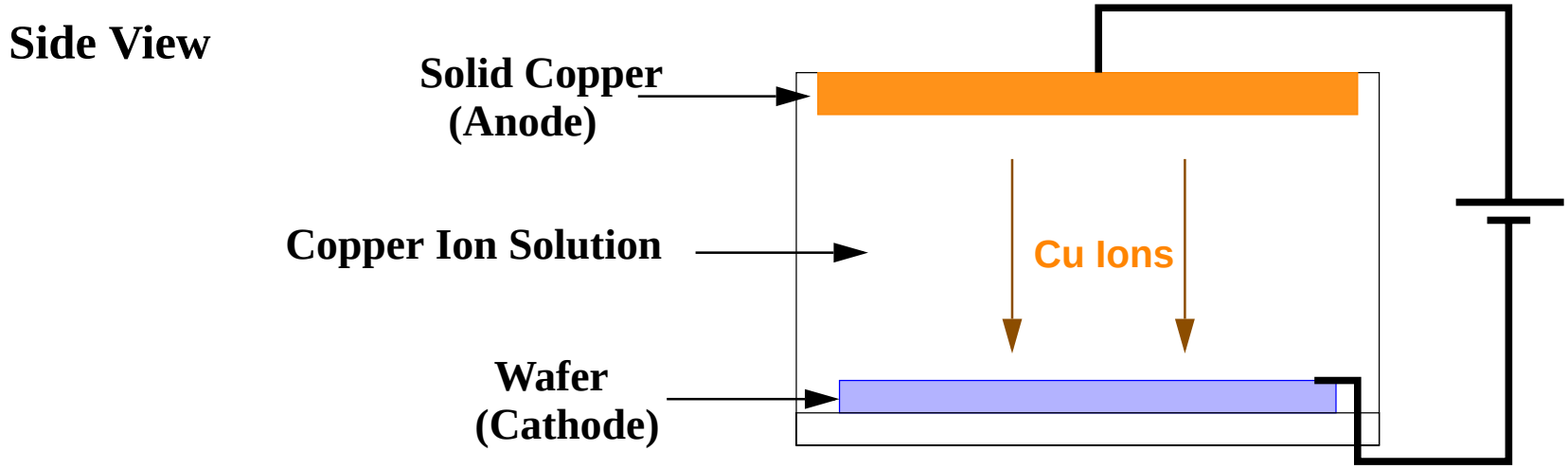

Chemical Mechanical Polishing (CMP) Problems

# Outline

- Introduction
  - Basics of Electroplating
- Characterization and Modeling Methodology
  - Test Mask Design and Measurement
  - Data Trends
  - Model Development
  - Chip-Scale Simulation Approach
  - Chip-Scale Simulation and Prediction Result
- Conclusion



# What is Copper Electroplating?

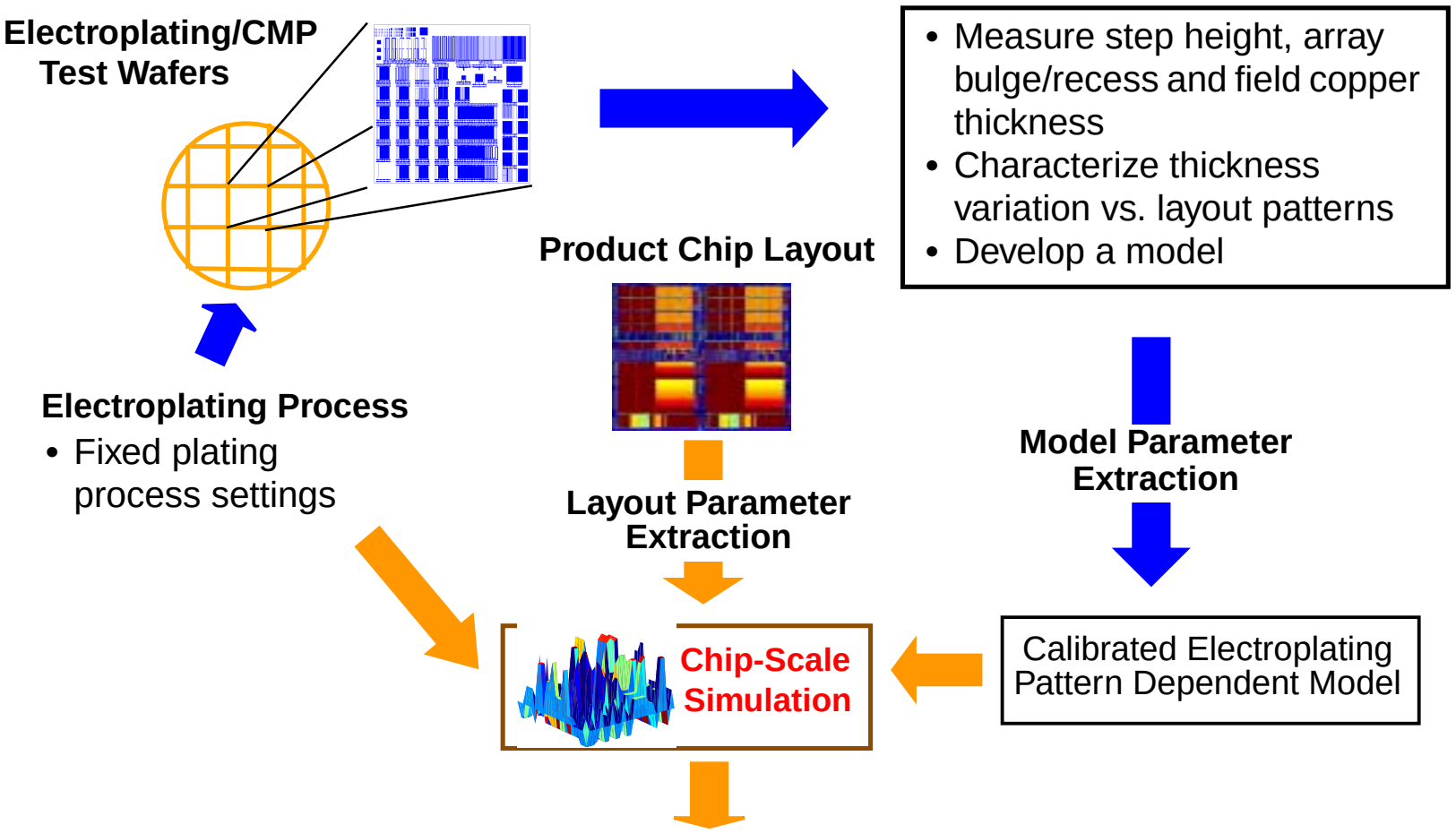



- Copper Ion Solution
  - Cu ions react with electrons and form copper at wafer surface
- Material deposited by a combination of
  - Faraday's law of electrolysis: amount of Cu deposition ~ current density
  - Added chemistry: suppresses or accelerates deposition rates on top and bottom of trenches => for bottom-up fill or superfill

✔ **Problem: non-uniform deposition due to layout patterns**

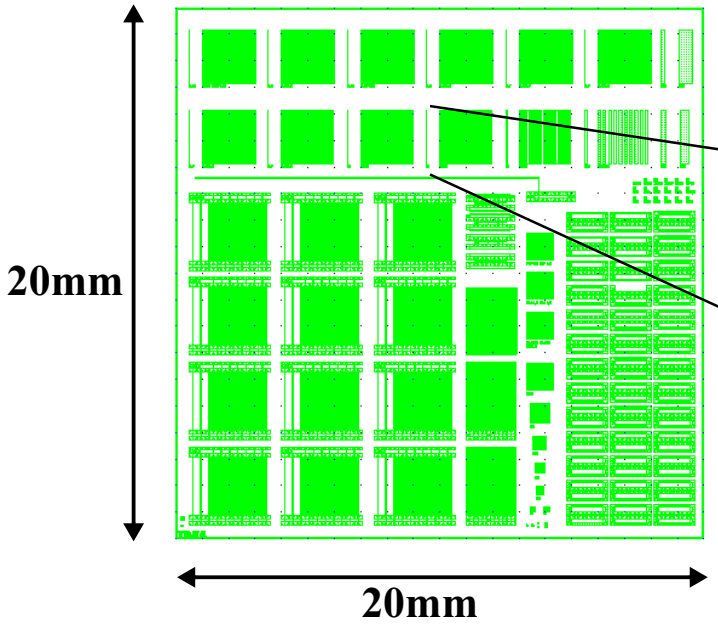
# Methodology for Electroplating Topography Characterization and Modeling

■ Goal: Chip-scale prediction of plated copper topography

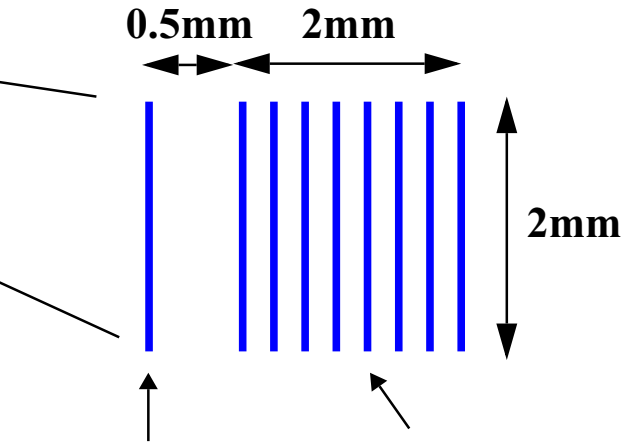


# Test Structure and Mask Design

- Purpose: capture and identify key pattern factors
- Basic test pattern: line and array structure
- Layout factors:
  - Pattern density from 10% to 90%
  - Pitch from 0.5μm to 200μm for fixed pattern density of 50%



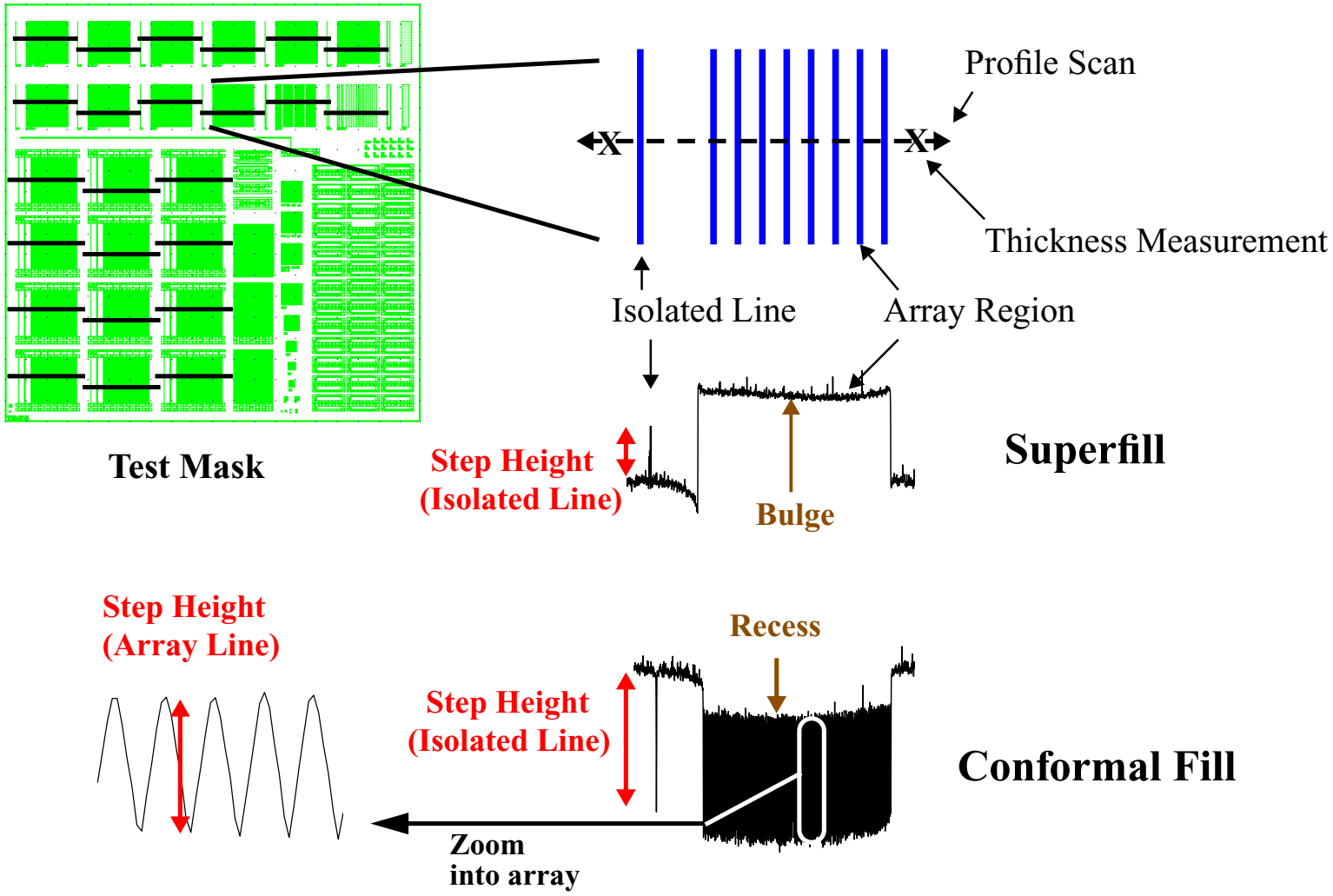

Copper Test Mask (V1.2)



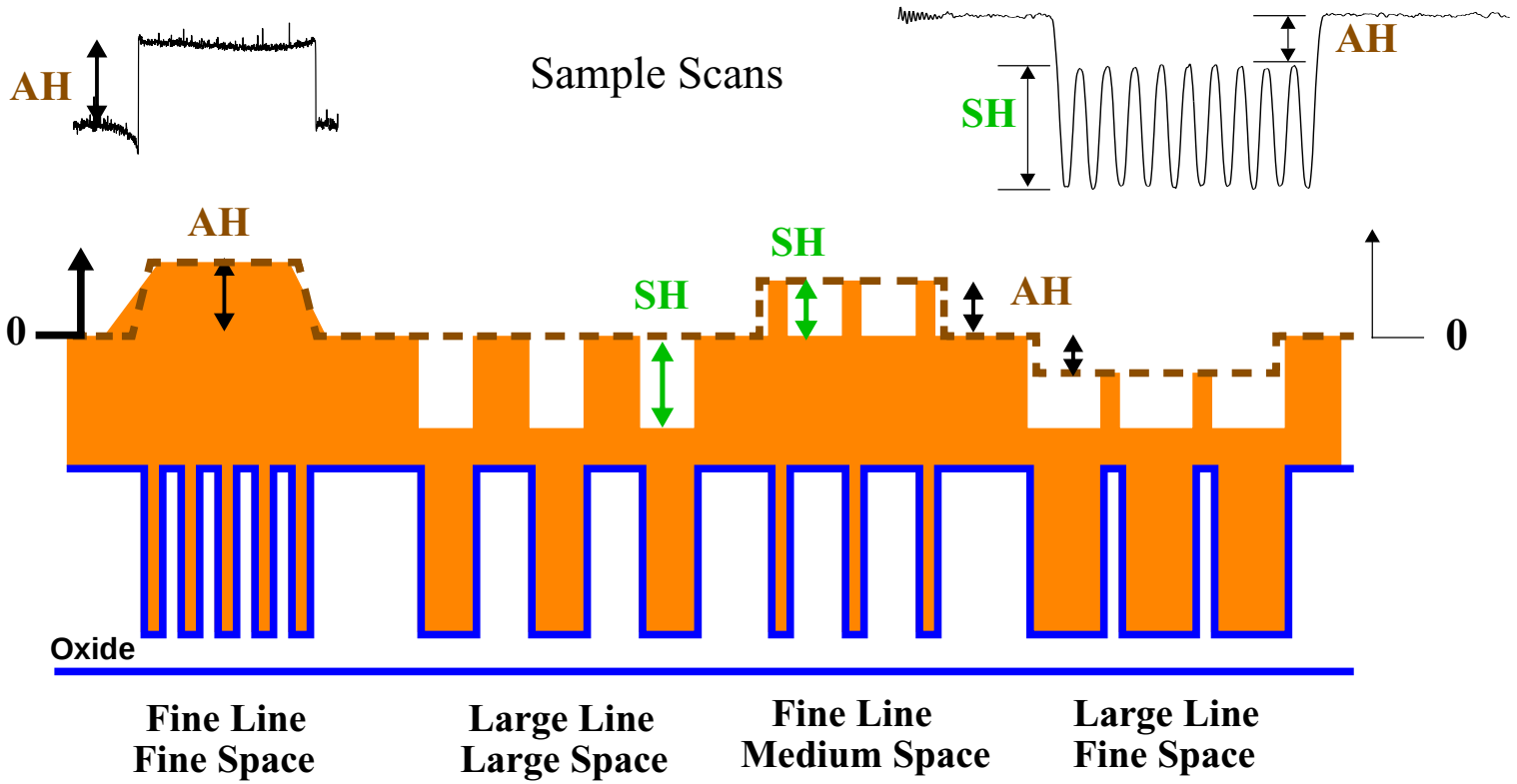

Basic Test Structure

# Measurement Plan and Sample Profile Scan

- Profile scans taken across each line/array structure

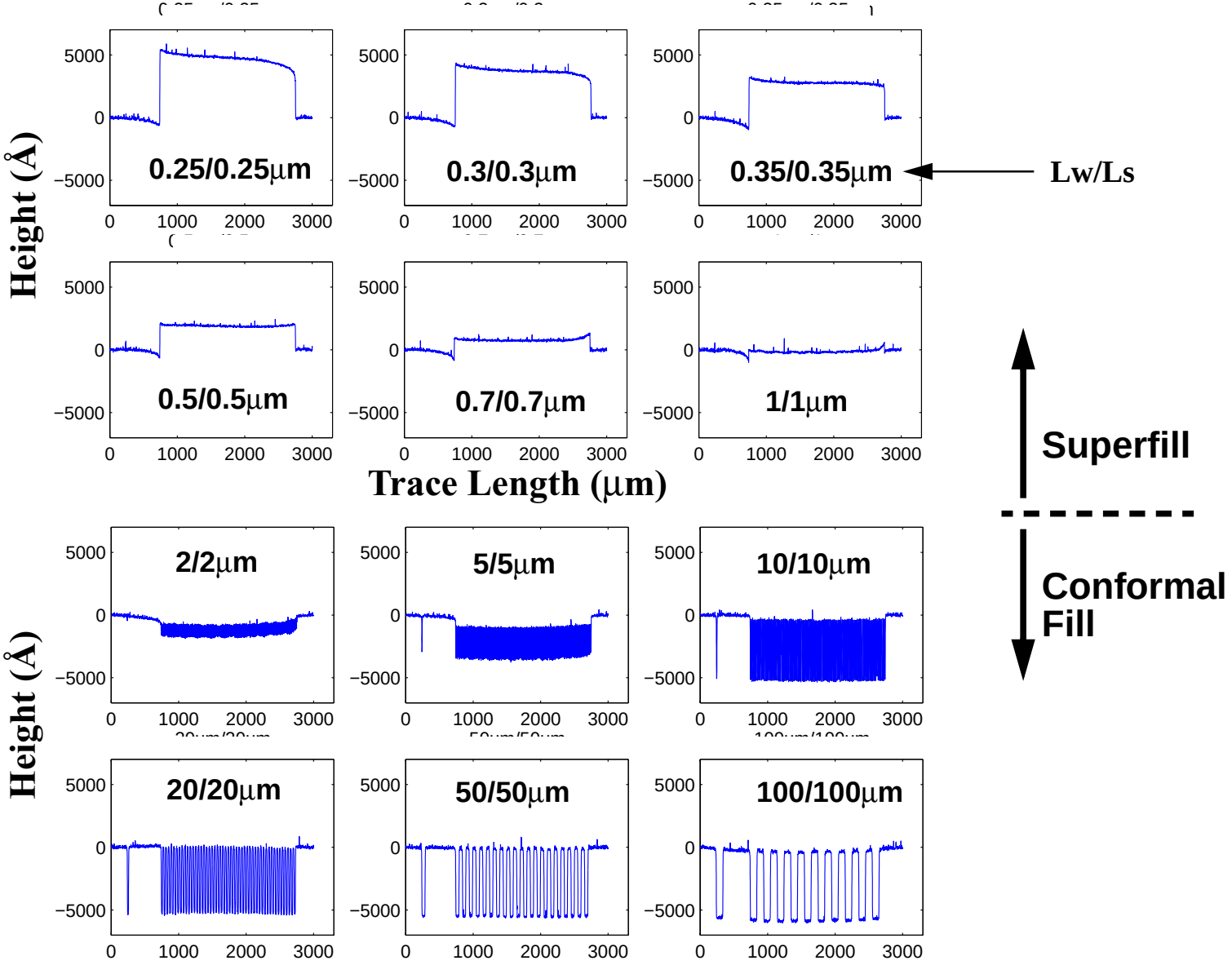


# Definitions of Electroplated Profiles

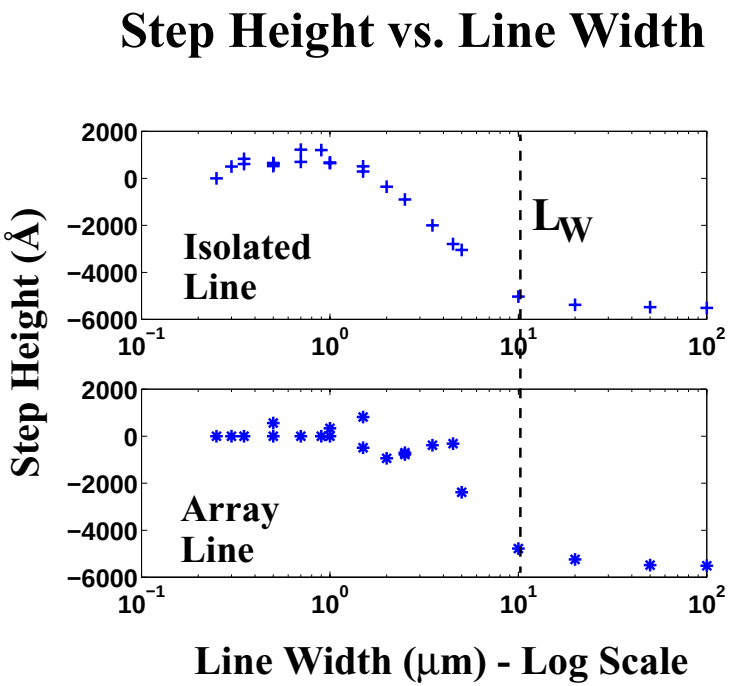


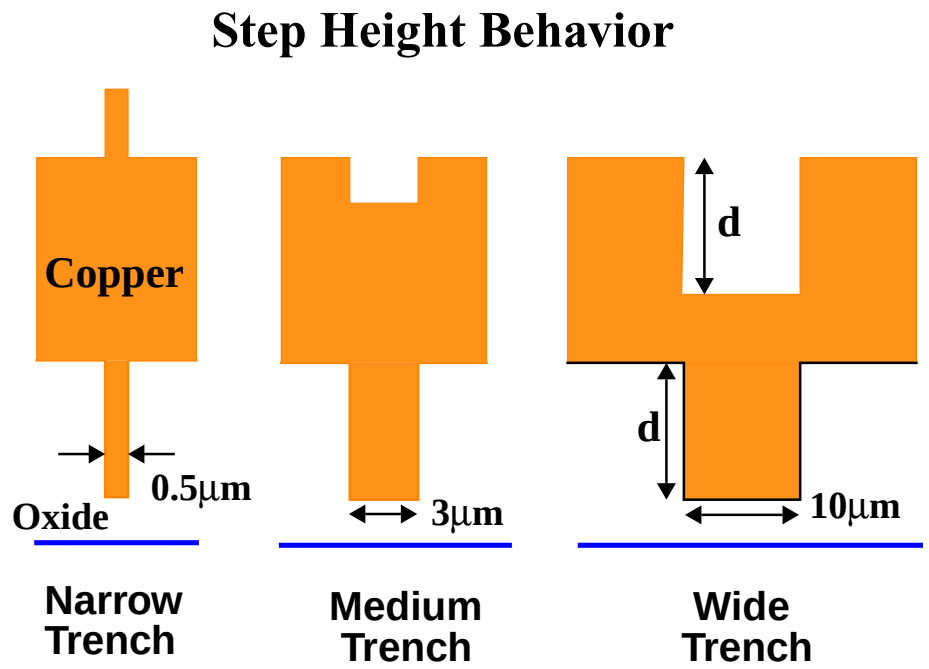

- Two topography variations defined
  - Step Height (SH): height associated with each copper line
  - Array Height (AH): height difference between the top of the raised features in an array and the flat copper field region over wide oxide

# Electroplated Profile Trends: Pitch Structures



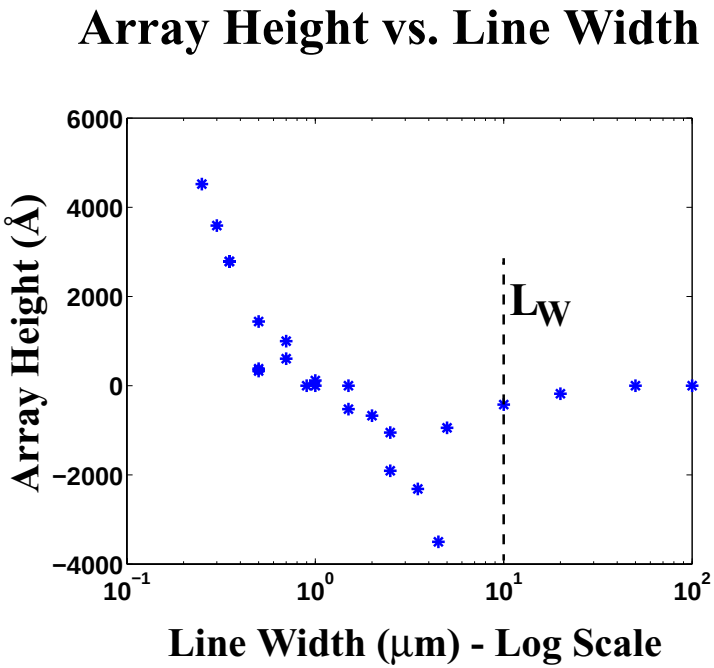
# Step Height Data Analysis

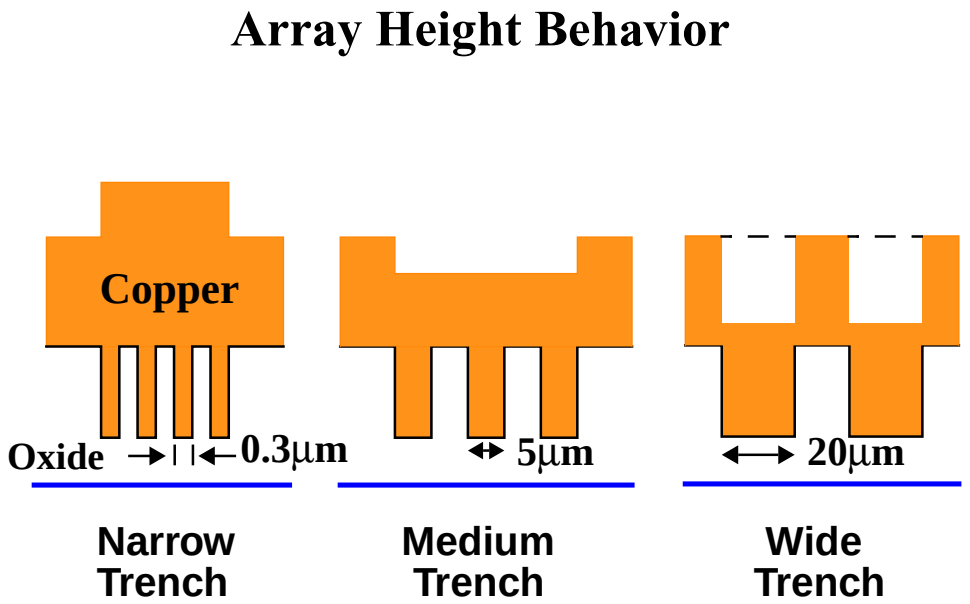



- Trends
  - SH depends on line width: near zero or positive (superfill) for small features and becomes more conformal as line width increases
- Saturation Length: fill becomes fully conformal and SH = Trench Depth
  - Line width $L_W$ = 10μm

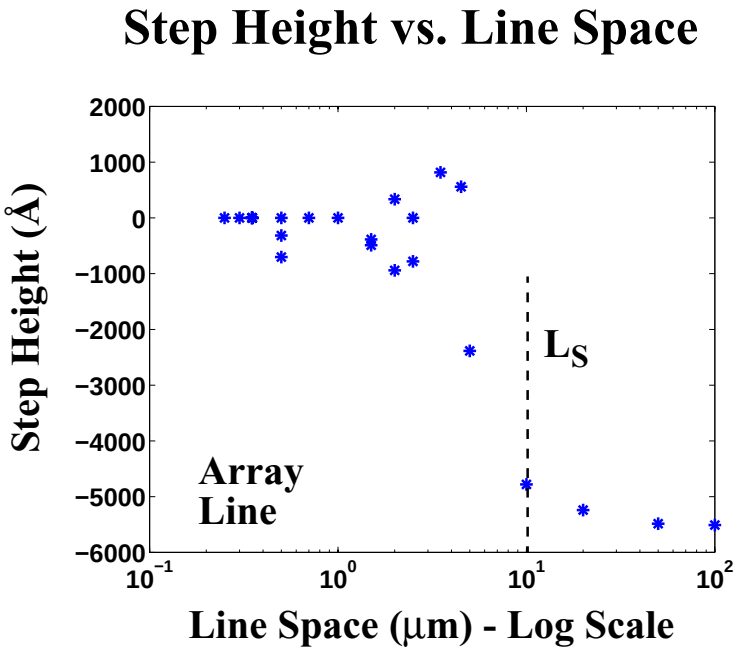
# Array Height Data Analysis

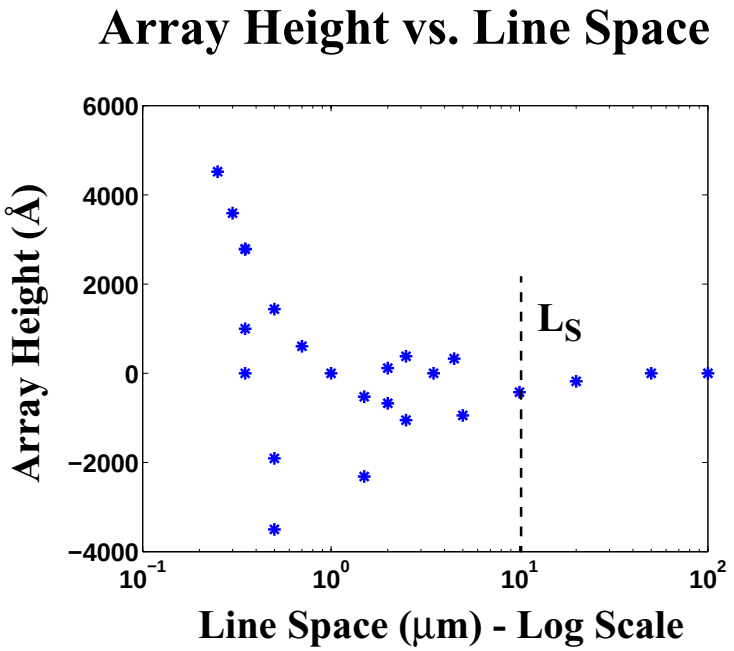



- Trends
  - Positive (superfill) for small features, and becomes negative (conformal), and saturates to field level as line width increases
- Saturation length: fill becomes fully conformal and AH = 0Å
  - Line width $L_W$ = 10μm

# SH and AH vs. Line Space

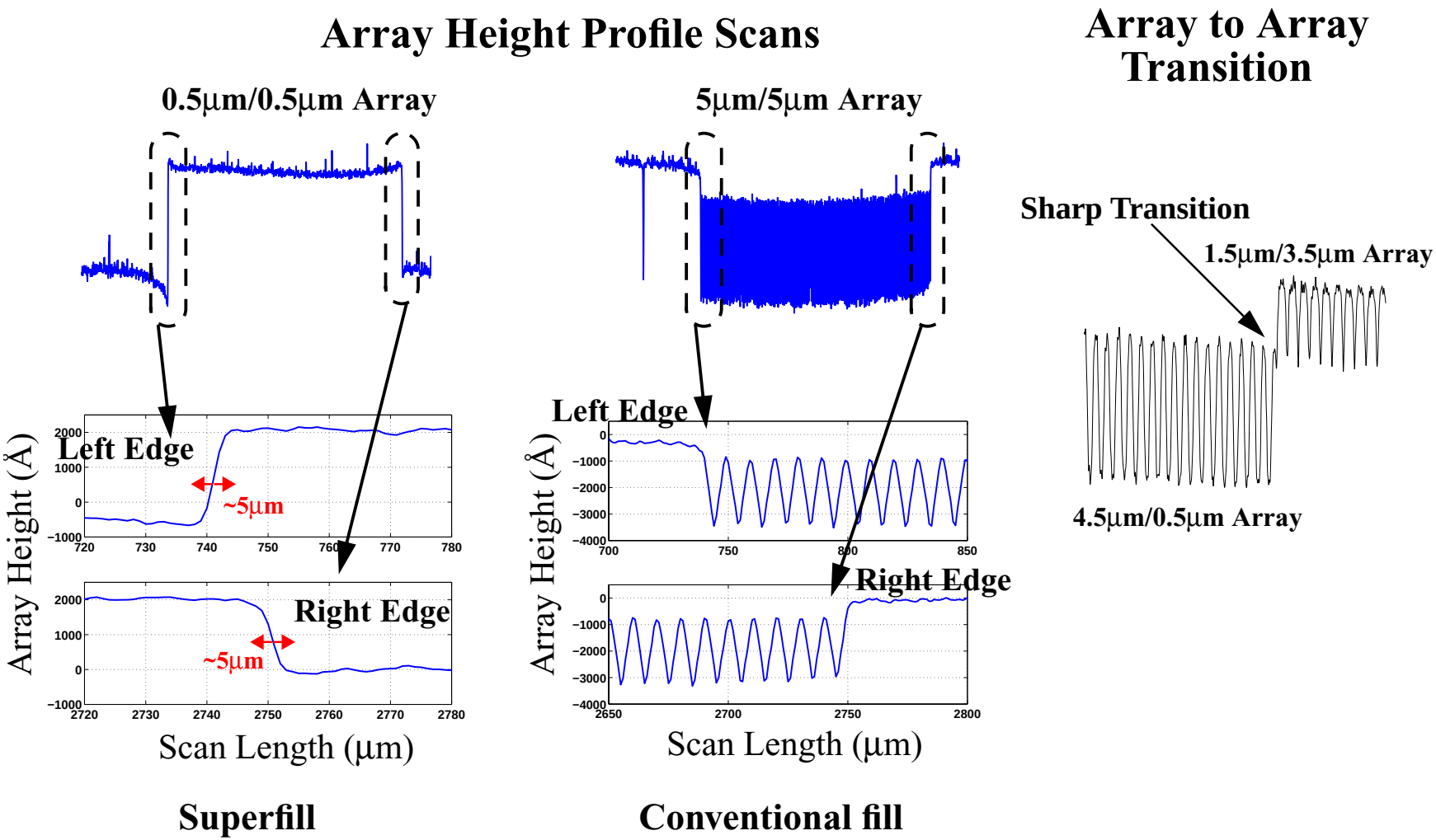



- Trends
  - Line space dependency for SH and AH is similar to line width dependency
- Saturation length: similar value is observed for line space
  - Line space $L_S$ = 10μm

# Transition Length Scale in Electroplating

- Plating depends on local feature (feature scale) and nearest neighbors within 2-5μm range



# Modeling Approach

- Trends are observed in electroplated topography dependent on the underlying layout parameters of line width and space
- Possible Implementation: Physical Feature-Scale Model
  - Often based on numerical analysis
  - Computationally prohibitive
  - Not suitable for chip-scale prediction: a wide range and combinations of line widths and spaces found in a “random” layout
- Our Approach: Response Surface Model:

  **Height ~ f(underlying layout parameters)**
  - Effective in chip-scale prediction (our eventual goal!)
  - Suitable for “random” layout

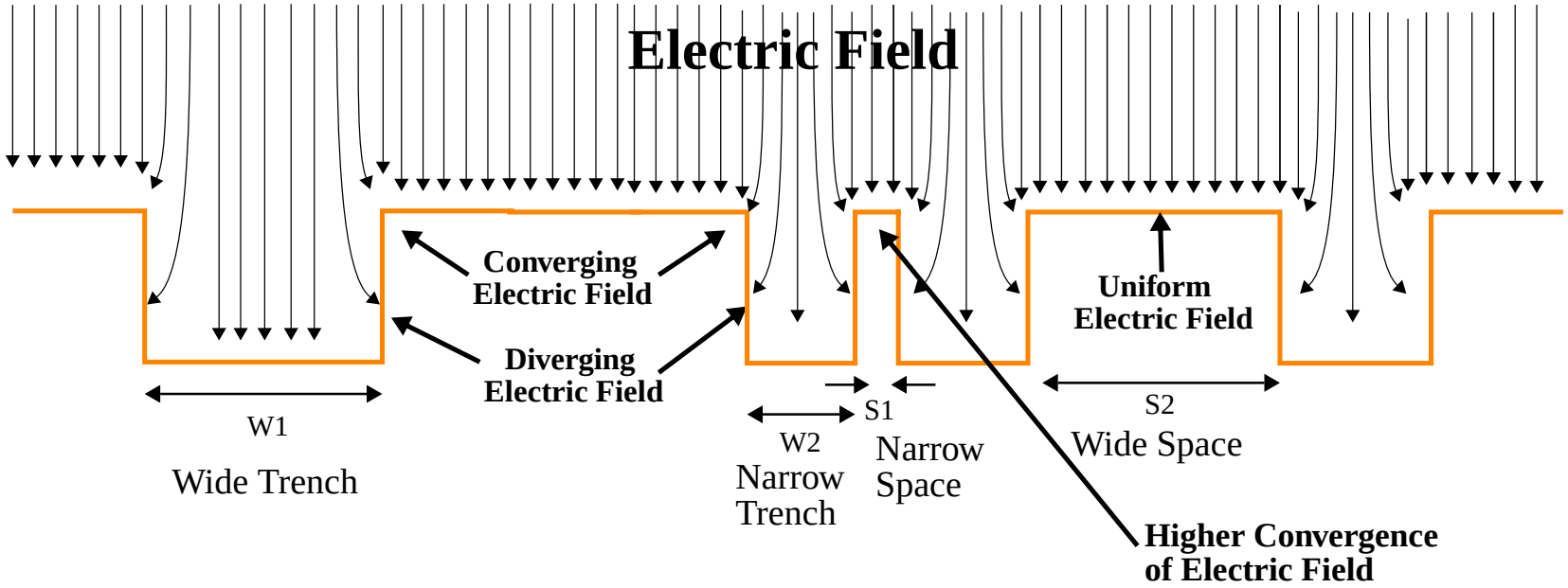
✔ **How do we choose the model variables?**
  - Physically motivated model variables are desired
  - Examine: basic principles and superfill effect



# Basic Electroplating Principles

- Governing Principle: Faraday's law of electrolysis
  - Amount of copper deposition ~ current density *J*

$$J = \sigma E = -\sigma \nabla \phi$$

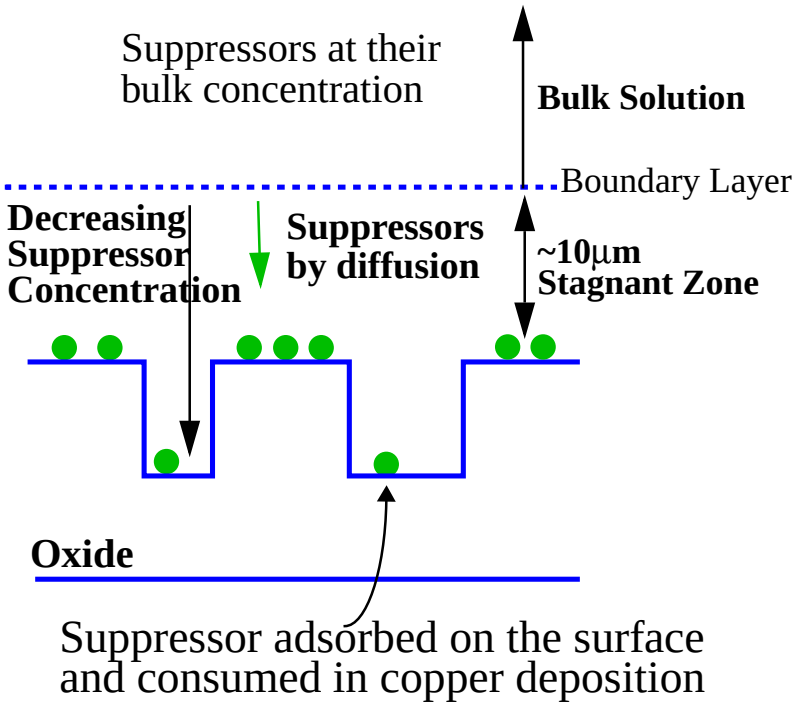



- Both line width and line space influence copper deposition rate
- Problem: voids are formed inside a trench due to early closing of trench top corners ☞ Superfill plating introduced

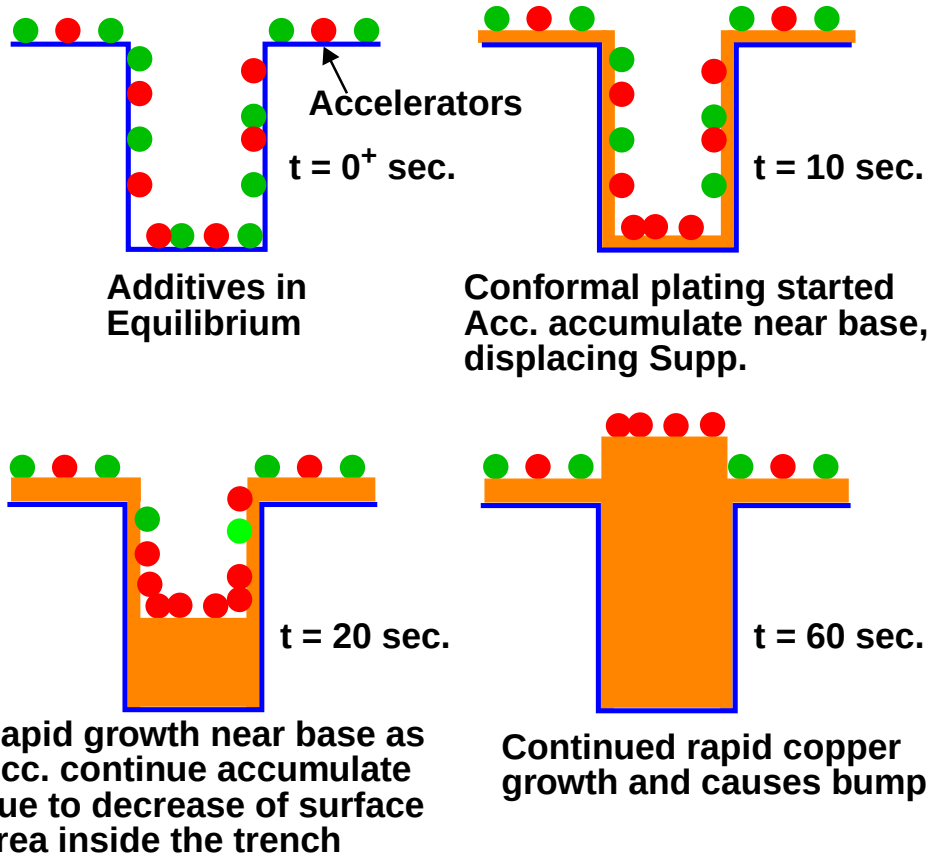
# Superfill Effect

- Various proposed mechanisms fall into two general categories

## Diffusion-Adsorption




## Additive-Accumulation




- Aspect ratio (depth/width) influences plating rate

# Semi-Empirical Model for Topography Variation

- Physically Motivated Model Variables:
  - Width, Space, 1/Width, and Width*Space
- Semi-Empirical Model Development
  - Capture both conformal regime and superfill regime in one model frame
  - $1/W^2$ and $W^2$ terms explored as well
- Model Form
  - Array Height:

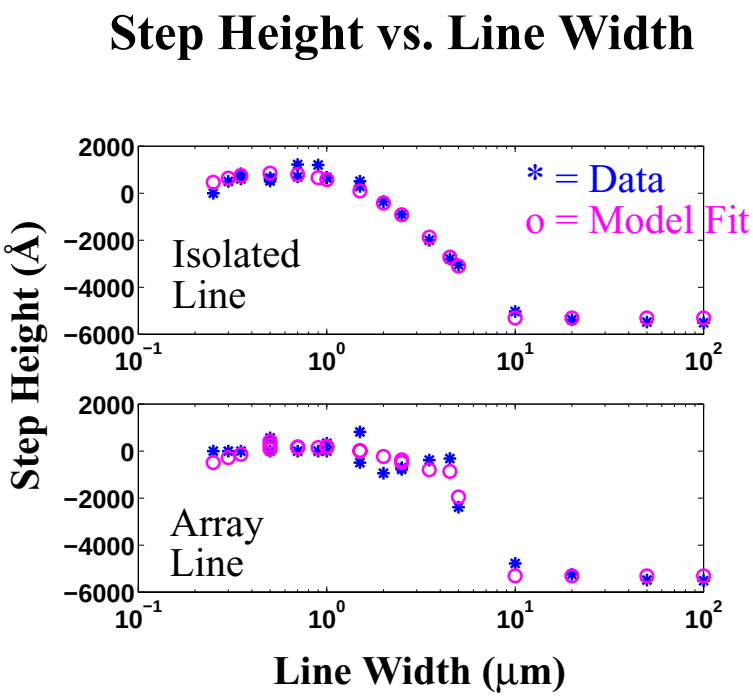
$$AH = a_E W + b_E W^{-1} + c_E W^{-2} + d_E S + e_E W \times S + Const_E$$

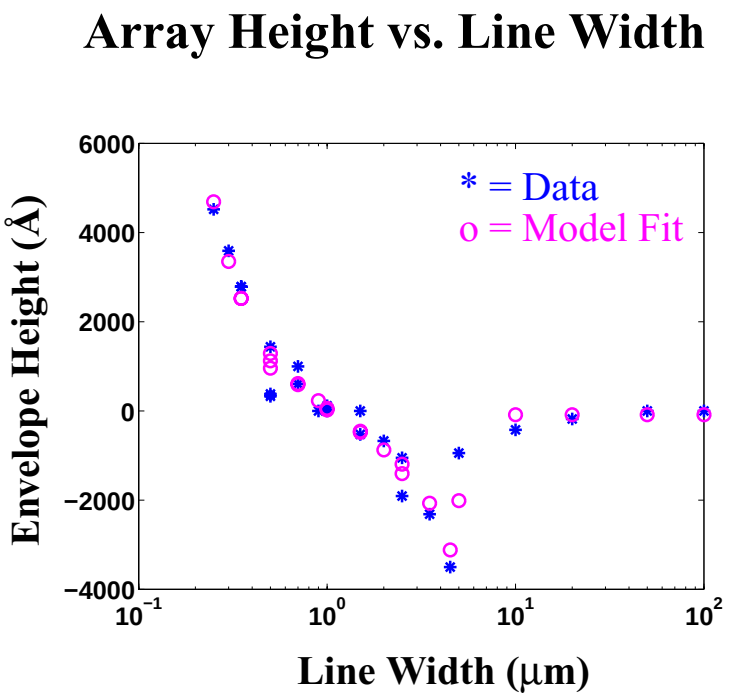
  - Step Height:

$$SH = a_S W + b_S W^{-1} + c_S W^{2} + d_S S + e_S W \times S + Const_S$$



# Model Fit: Step Height and Array Height



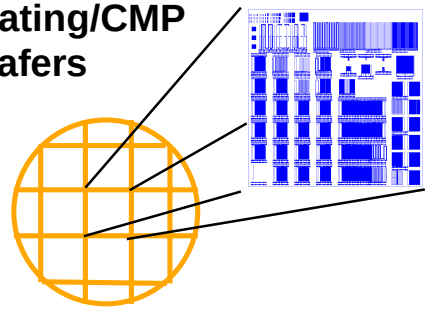




- The models capture both trends well
  - Step Height RMS error = 327 Å
  - Array Height RMS error = 424 Å
- Model coefficients are calibrated and used for chip-scale simulations

# Outline

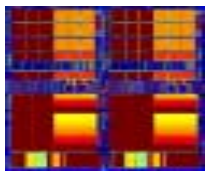
## ■ Procedure for Chip-Scale Prediction

**Electroplating/CMP Test Wafers**



- Measure step height, array bulge/recess and field copper thickness
- Characterize thickness variation vs. layout patterns
- Develop a model

**Product Chip Layout**

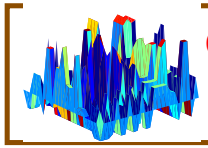


**Electroplating Process**

- Fixed plating process settings

**Layout Parameter Extraction**

**Model Parameter Extraction**

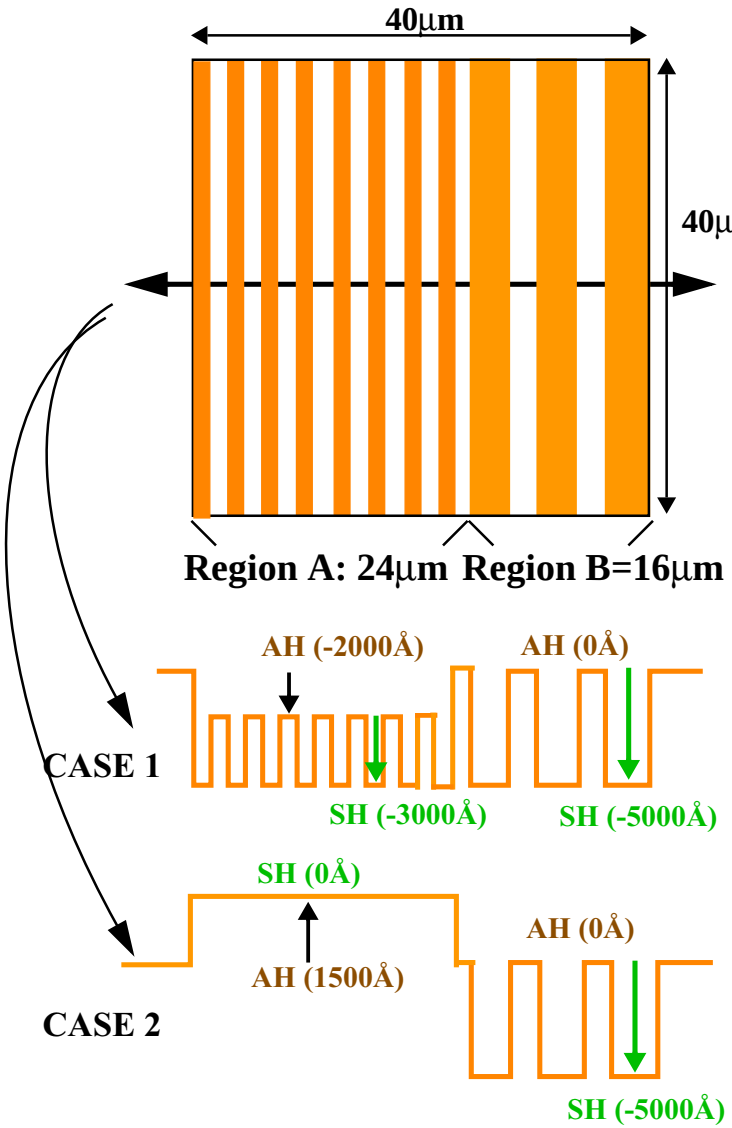


**Chip-Scale Simulation**

Calibrated Electroplating Pattern Dependent Model

**Prediction of step height and array height across an entire chip**

# Chip-Scale Simulation: Basic Approach




**Electroplated Surface Profiles**

## ■ Approach:

- ❑ Compute a generalized "average" (area-weighted) array height and step height for a grid cell
- ❑ Grid cells are equally divided small regions on a die

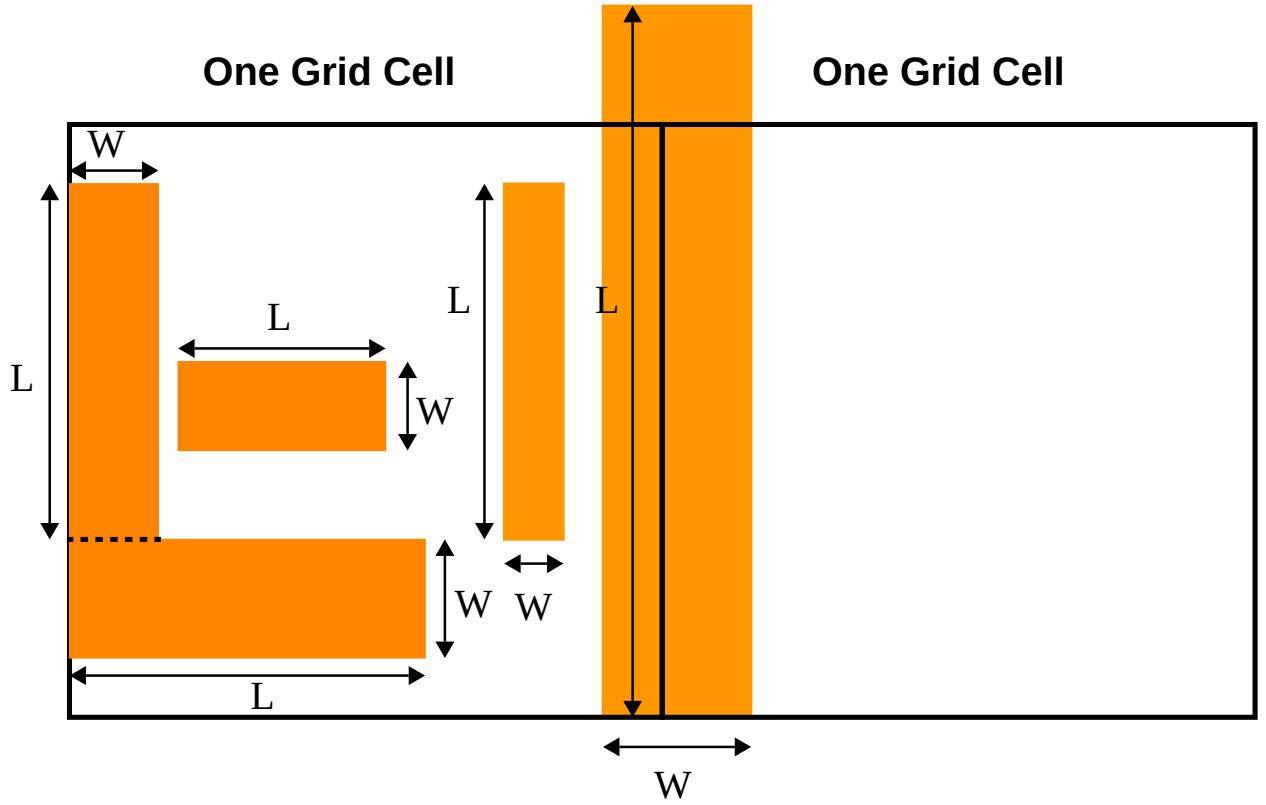
## ■ Example: CASE 1:

- $AH_{Avg}$ = (-2000Å x 24μm + 0Å x 16μm)/40μm = -1200Å
- $SH_{Avg}$ = (-3000Å x 24μm + -5000Å x 16μm)/40μm = -3800Å

## ■ Example: CASE 2:

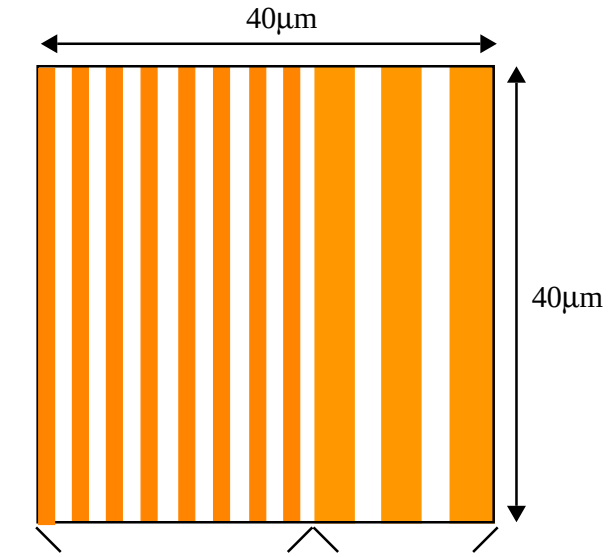
- $AH_{Avg}$ = (1500Å x 24μm + 0Å x 16μm)/40μm = 900Å
- $SH_{Avg}$ = (0Å x 24μm + -5000Å x 16μm)/40μm = -2000Å

# Layout Extraction: Line Width and Length for Random Layout




- Line Width: shorter dimension; Line Length: longer dimension
- Polygons: cut into rectangles and apply the same definition

# Example Grid Cell and Layout Extraction Result




**Example Layout Extraction**

| Layout Parameter Extracted | Values |
|---|---|
| Min. W | 1.5μm |
| Avg. W | 2.182μm |
| Max. W | 4μm |
| Avg. Length, $\overline{L}$ | 40μm |
| Layout Copper Pattern Density, $\rho_c$ | 60% |
| Bin 1: Min_CD < W < 0.35μm | 0 Count |
| Bin 2: 0.35μm < W <= 0.5μm | 0 Count |
| Bin 3: 0.5μm < W <= 1μm | 0 Count |
| Bin 4: 1μm < W <= 2μm | 8 Counts |
| Bin 5: 2μm < W <= 5μm | 3 Counts |
| Bin 6: 5μm < W <= 10μm | 0 Count |
| Bin 7: 10μm < W | 0 Count |
| Total Count (of lines in all bins) | 11 |
| X, Y Location of the Grid Cell | $X_o$, $Y_o$ |

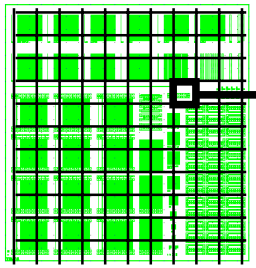
- Use a binning approach to the distribution of line widths
  - Gives a count of the number of lines having a line width in each bin of the line width distribution



# Layout Extraction and Simulation Procedure

## Layout Extraction

**Mask Layout**



Mask discretized into 40 x 40μm cells

**One Grid Cell**

Layout extractor is used to compute layout parameters in each cell

**Layout Parameters Extracted for Each Cell:**

- Average, min., and max. line width
- Average line length
- Copper pattern density
- Line width distributions

**Layout Parameters**

## Chip-Scale Simulation

**Area-Weighted Average of Each Bin**

1. Assign representative line width for each bin
2. Derive line space for each bin from copper pattern density and line width bins
3. Compute area occupied by lines in each bin
4. Simulate step and array heights for each bin
5. Determine step and array heights by area-weighted averages



# 1. Representative Line Width for Each Bin

- Assign a representative width for each bin: mean of the low and high cutoff values of each bin

| Width, $W_i$, for $i^{th}$ Bin | Min. Line Width for Each Bin | Max. Line Width for Each Bin | Assigned Line Width |
|---|---|---|---|
| W1 | Min_CD = 0.25μm | 0.35μm | (Min_CD + 0.35)/2 = 0.3μm |
| W2 | 0.35μm | 0.5μm | 0.425μm |
| W3 | 0.5μm | 1μm | 0.75μm |
| W4 | 1μm | 2μm | 1.5μm |
| W5 | 2μm | 5μm | 3.5μm |
| W6 | 5μm | 10μm | 7.5μm |
| W7 | 10μm | | $L_W$ = 10μm |

# 2. Average Line Space for Each Bin *i*

$$\rho_c = \frac{W}{W + S}$$

- Estimate line space $S$ in terms of the available copper pattern density, $\rho_c$, and width, $W$

$$S_i = \frac{W_i(1 - \rho_c)}{\rho_c}$$



# 3. Compute Area Occupied by Lines in Each Bin

$$A_i = W_i \cdot N_i \cdot \bar{L}$$

- $W_i$ is the assigned line width for the $i^{th}$ bin
- $N_i$ is the number of lines in the $i^{th}$ bin
- $\bar{L}$ is the average line length in the grid cell

# 4. Simulate Step and Array Height for Each Bin

$$AH_i = a_A W_i + b_A W_i^{-1} + c_A W_i^{-2} + d_A S_i + e_A W_i \times S_i + Const_A$$

$$SH_i = a_S W_i + b_S W_i^{-1} + c_S W_i^{2} + d_S S_i + e_S W_i \times S_i + Const_S$$

- $a_A$ through $e_A$ and $a_S$ through $e_S$ are the empirically extracted model coefficients for *AH* and *SH*, respectively

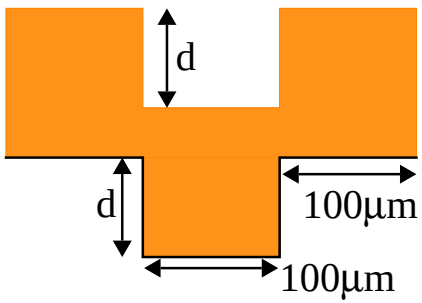


# 5. SH and AH by Area-Weighted Averages

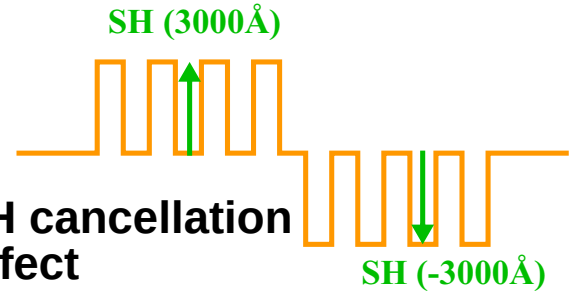
$$AH = \begin{cases} 0 & Total\ \ Count = 0 \quad or \quad \rho_c < 0.01 \\ -H_o\ \ (Trench\ \ Depth) & Copper\ \ Pattern\ \ Density\ \ \rho_c > 0.99 \\ \dfrac{\sum_i (AH_i \cdot A_i)}{A} & Otherwise \end{cases}$$

$$SH = \begin{cases} 0 & Total\ \ Count = 0 \quad or \quad \rho_c < 0.01 \\ 0 & Copper\ \ Pattern\ \ Density\ \ \rho_c > 0.99 \\ \dfrac{\sum_i (|SH_i| \cdot A_i)}{A} & Otherwise \end{cases}$$

- Total area $A$ is the sum of each bin area $A_i$, or $A = \sum A_i$




**Special Cases:**
**Case 1: Cell within field**
**Case 2: Cell within trench**



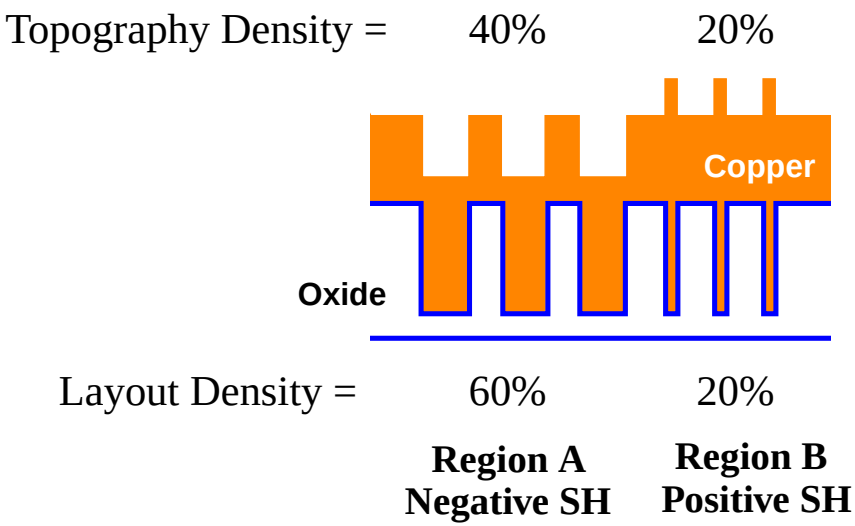

**SH cancellation Effect**

# Topography Pattern Density

- The topography density $\rho_T$ represents the area fraction of "raised" features in each grid cell

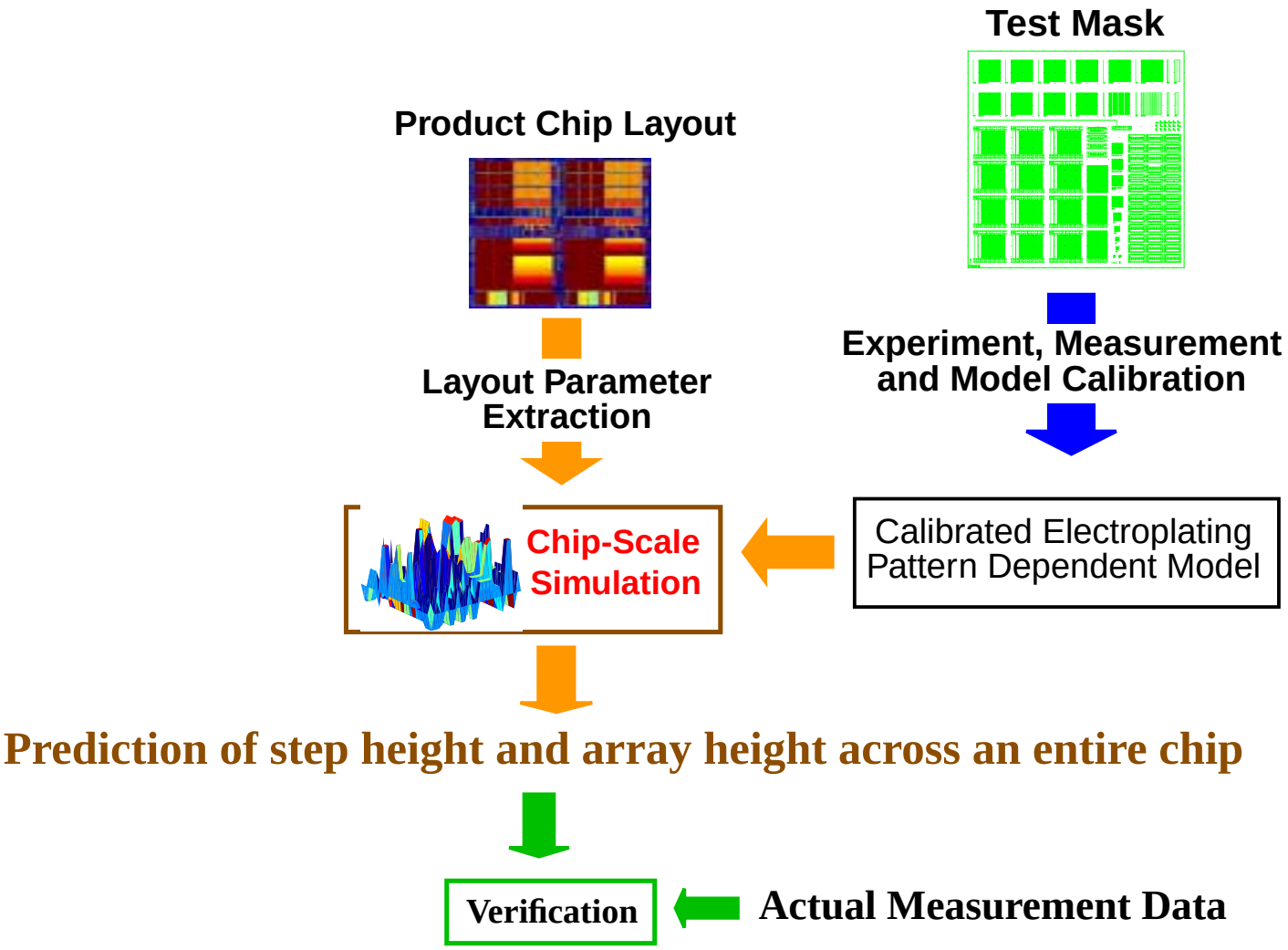
$$\rho_T = \begin{cases} \rho_c & SH > 0 \\ 1 - \rho_c & SH < 0 \\ 1 & SH = 0 \end{cases}$$

- $\rho_c$ is the layout copper pattern density as computed by the layout extractor



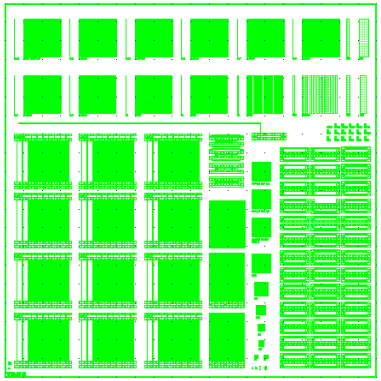
# Outline

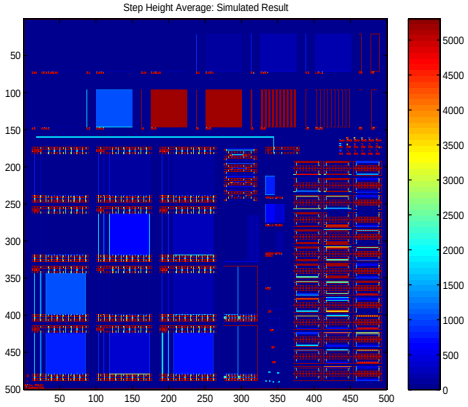
- Chip-Scale Simulation and Prediction Results



# Chip-Scale Simulation Calibration Results

**Test Mask**

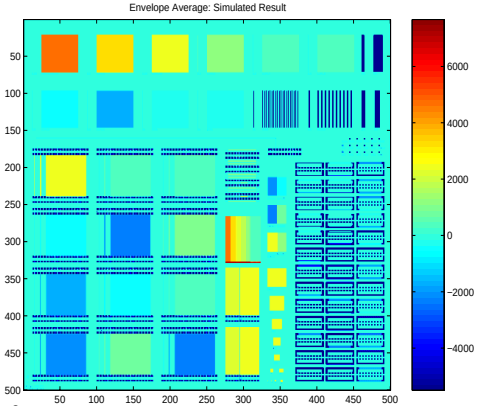




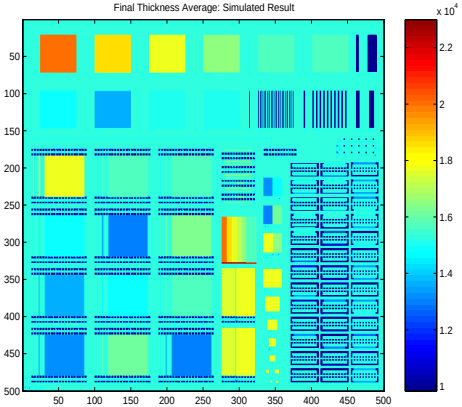

**Step Height**

**RMS Error=420Å**

**Array Height**




**RMS Error=440Å**

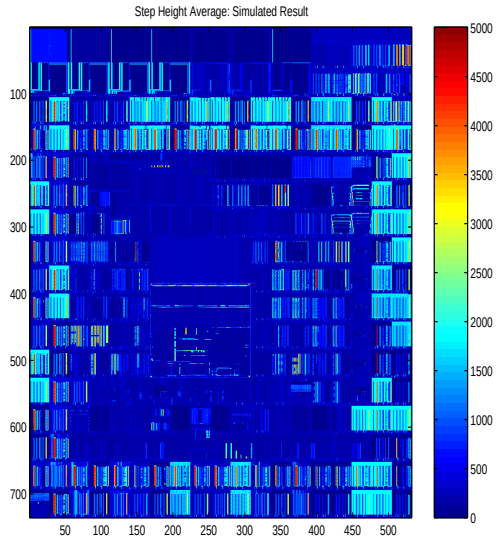



**Final Thickness**

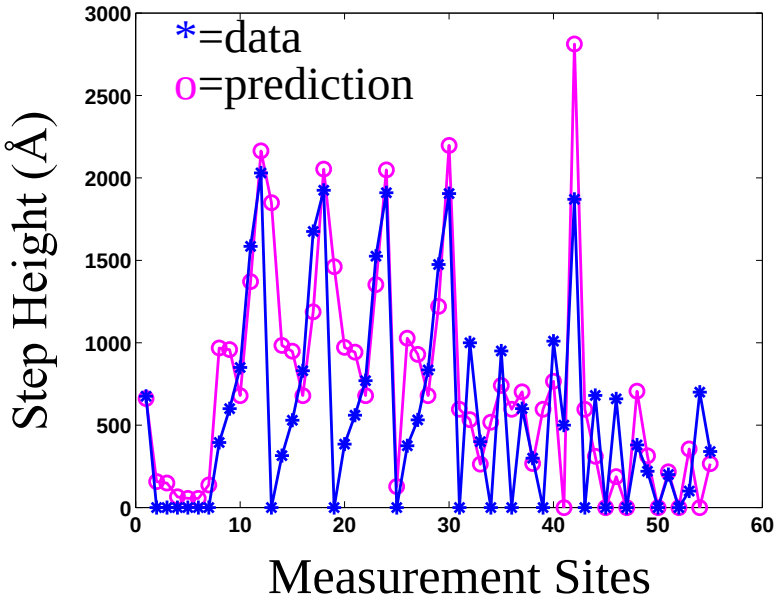
- Simulated over the entire test mask used to calibrate the model
- RMS errors are slightly greater (about 90Å and 10Å more) than fitting RMS errors since distribution values are used



# Chip-Scale Prediction and Verification Result: Arbitrary Chip




**Step Height**

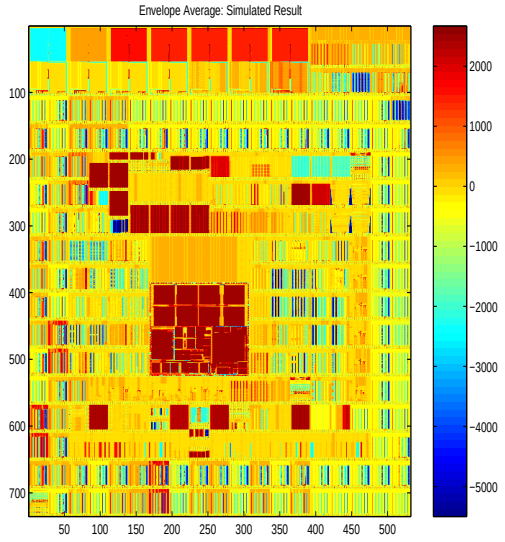



Prediction RMS Error = 479Å

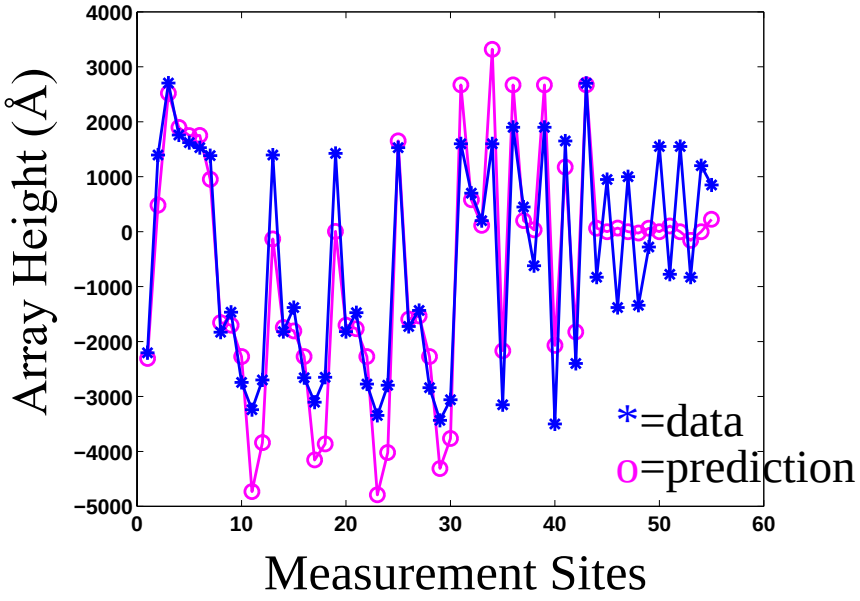
✔ **Chip-scale prediction is achieved!**

■ Step height trend is predicted with RMS error of 479 Å

# Chip-Scale Prediction and Verification Result: Arbitrary Chip




**Array Height**



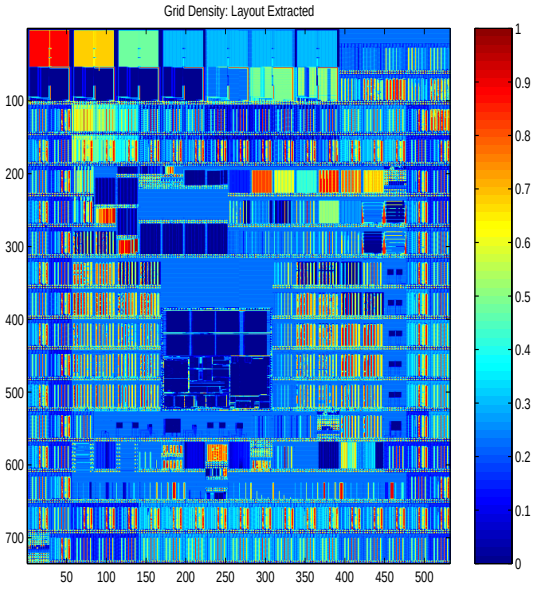

Prediction RMS Error = 870Å

✔ **Chip-scale prediction is achieved!**

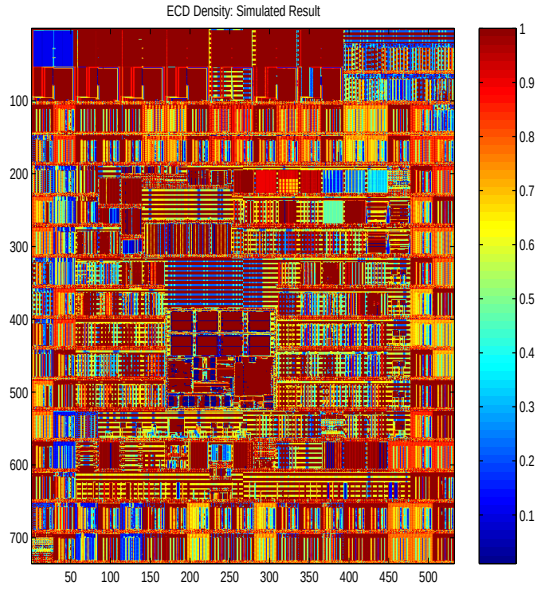
■ Array height trend is predicted with RMS error of 870 Å

# Topography Pattern Density

- Topography density: as-plated surface topography pattern density of raised features
  - Depends on plating characteristics
  - Important as an input for CMP pattern density model




**Layout Density**




**Topography Density**

# Conclusion

- Characterization and modeling methodology has been developed for pattern dependent topography variation of copper plating process
- Test mask design
  - Line/array structures with different layout factors to identify key trends
- Trends of step and array heights
  - Depend on underlying layout parameters of line width and space
- Semi-empirical response surface model
  - Captures overall trend including both conformal fill and superfill
  - Enables effective computation of topography simulation across an entire chip
- Chip-scale simulation and prediction
  - Chip-scale simulation methodology is developed
  - Chip-scale prediction achieved for arbitrary layout



# Acknowledgment


- DARPA & NSF
- SRC/ERC for Environmentally Benign Semiconductor Manufacturing
- Texas Instruments
- International SEMATECH
- PDF Solutions
- Praesagus
- SKW Associates
- Applied Materials