Trends in Dielectric Etch for Microelectronics Processing

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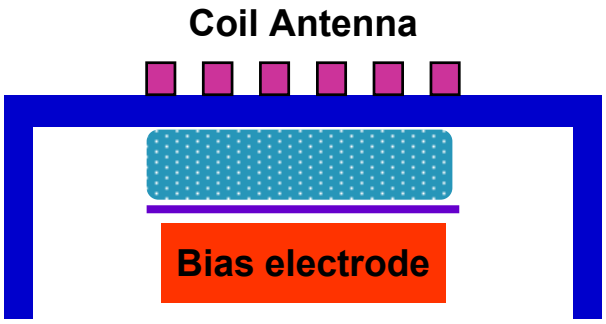
Overview

- Trends in dielectric etch technology
  - Plasma source
  - Confined plasma
  - Integrated processing
  - Process control
  - Knowledge-based development : Diagnostics and modeling
- Trends in dielectric etch applications
  - Reduction of design rule
    - Photoresist issues
  - Front end (FE) applications -- building the transistors and capacitors
    - HARC, Container, SAC, Gate Mask
  - Back end (BE) applications -- making the connections
    - low-*k* dielectric
    - Cu interconnect / dual damascene
    - Integration issues

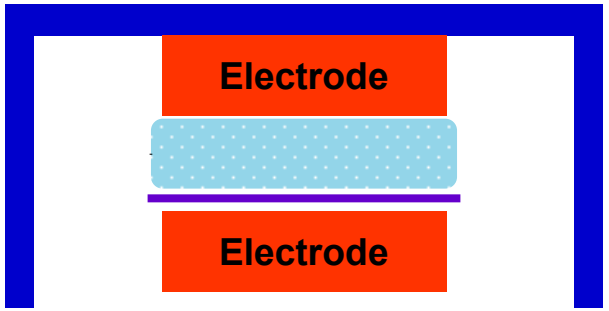
Dielectric etch technology: Plasma source

- Inductively coupled plasma (ICP) sources are no longer used for leading edge dielectric etch
  - ICP source with capacitively coupled bias RF -- still widely used for polysilicon and metal etch
  - ICP approach used for dielectric etch in mid-to-late-1990's
    - "High density"
    - Decoupled control of plasma density and ion energy
    - Some success, but also problems



Inductively coupled

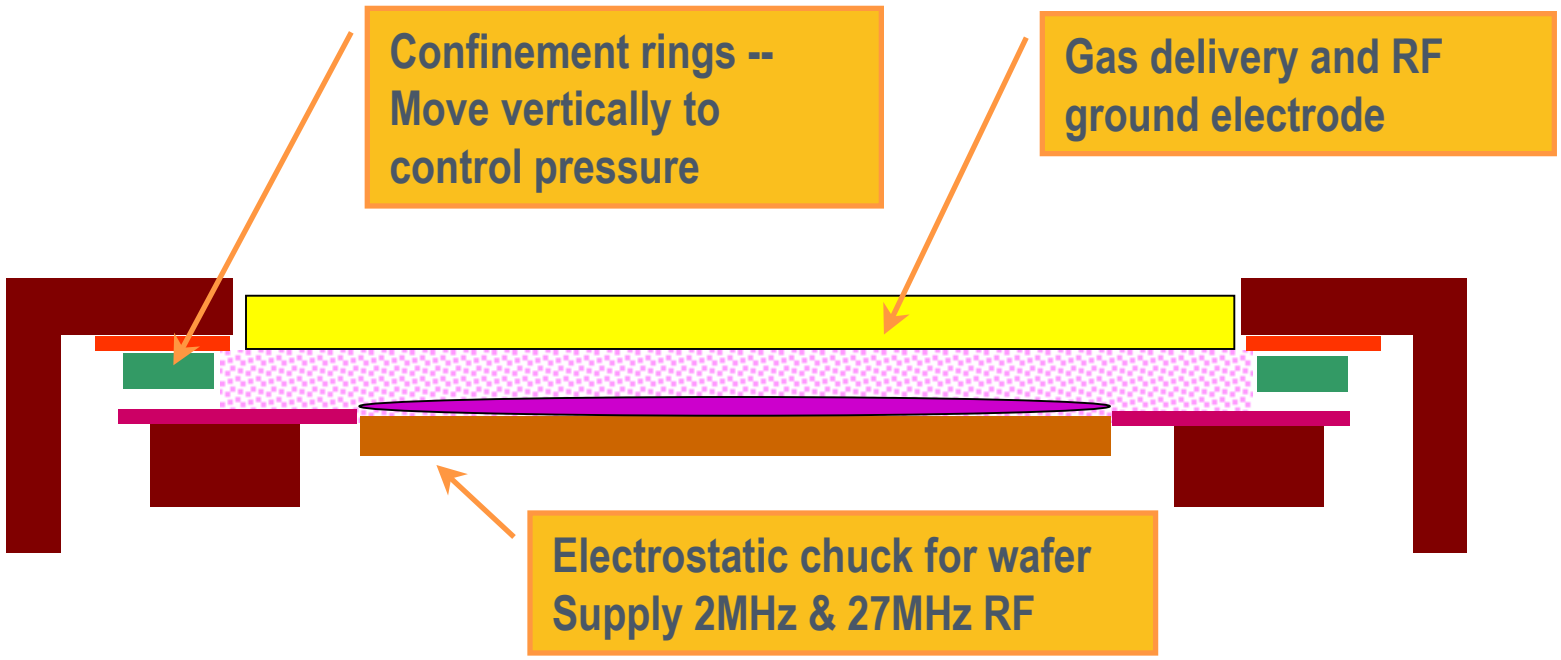
- Dual-frequency capacitive has become the industry standard
  - Parallel-plate configuration
  - Two RF frequencies
    - Some decoupling of plasma density and ion energy
  - "Medium density"
  - Less dissociation of feed gases, more control over radical chemistry



Capacitively coupled dual frequency

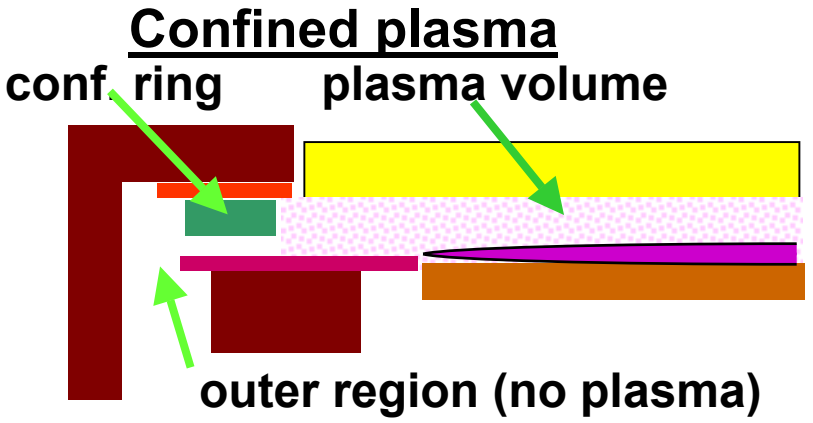
Dielectric etch technology: Dual-Frequency Confined™ (DFC™)

- Use Exelan® family of dielectric etch systems as example of DE technology
- Feed RF at two frequencies to lower electrode
- Physically confined plasma



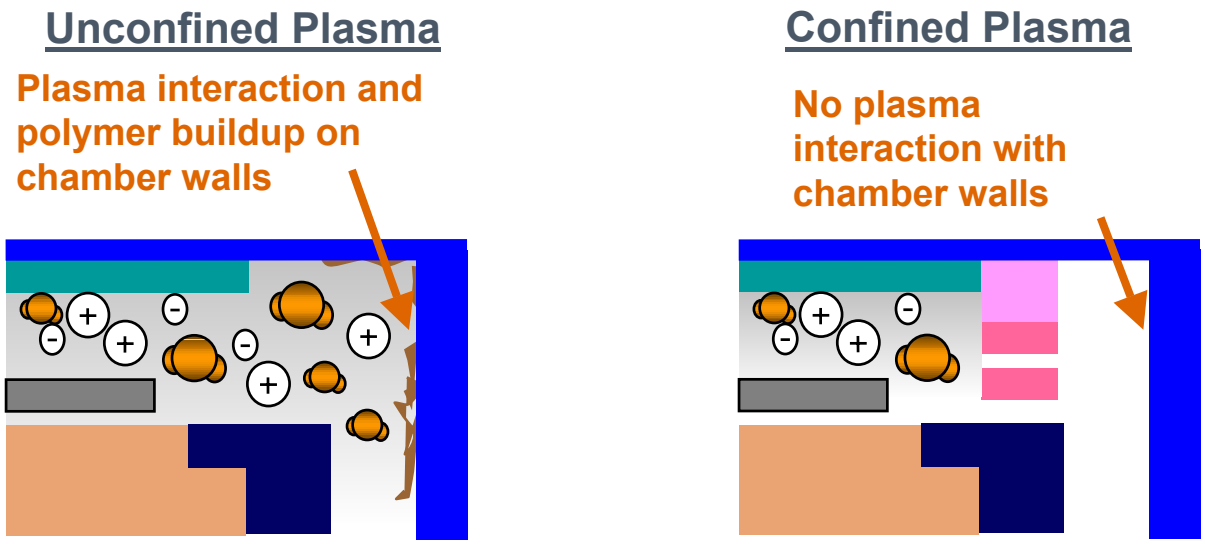
Dielectric etch technology: Confined plasma

- Mechanical confinement ring
  - Neutralizes charged particles as they exit plasma volume
  - Control gas pumping speed out of plasma by adjusting confinement ring position
    - Use feedback for real-time pressure control -- improve process repeatability
- Pressure differential during processing
  - Outer chamber pressure is typically <10% of confined plasma pressure
  - Gas species in outer region are rapidly pumped away
    - Plasma effluent unlikely to interact with chamber walls
    - Species evolved from walls unlikely to diffuse back into plasma volume
  - Gas residence time for processing depends only on plasma volume, not total volume
    - Small volume ⇒ reduces gas residence time in plasma
- Only high-purity materials used in confined region
  - Volatile etch products
  - Minimize sources for metal contamination and particulates



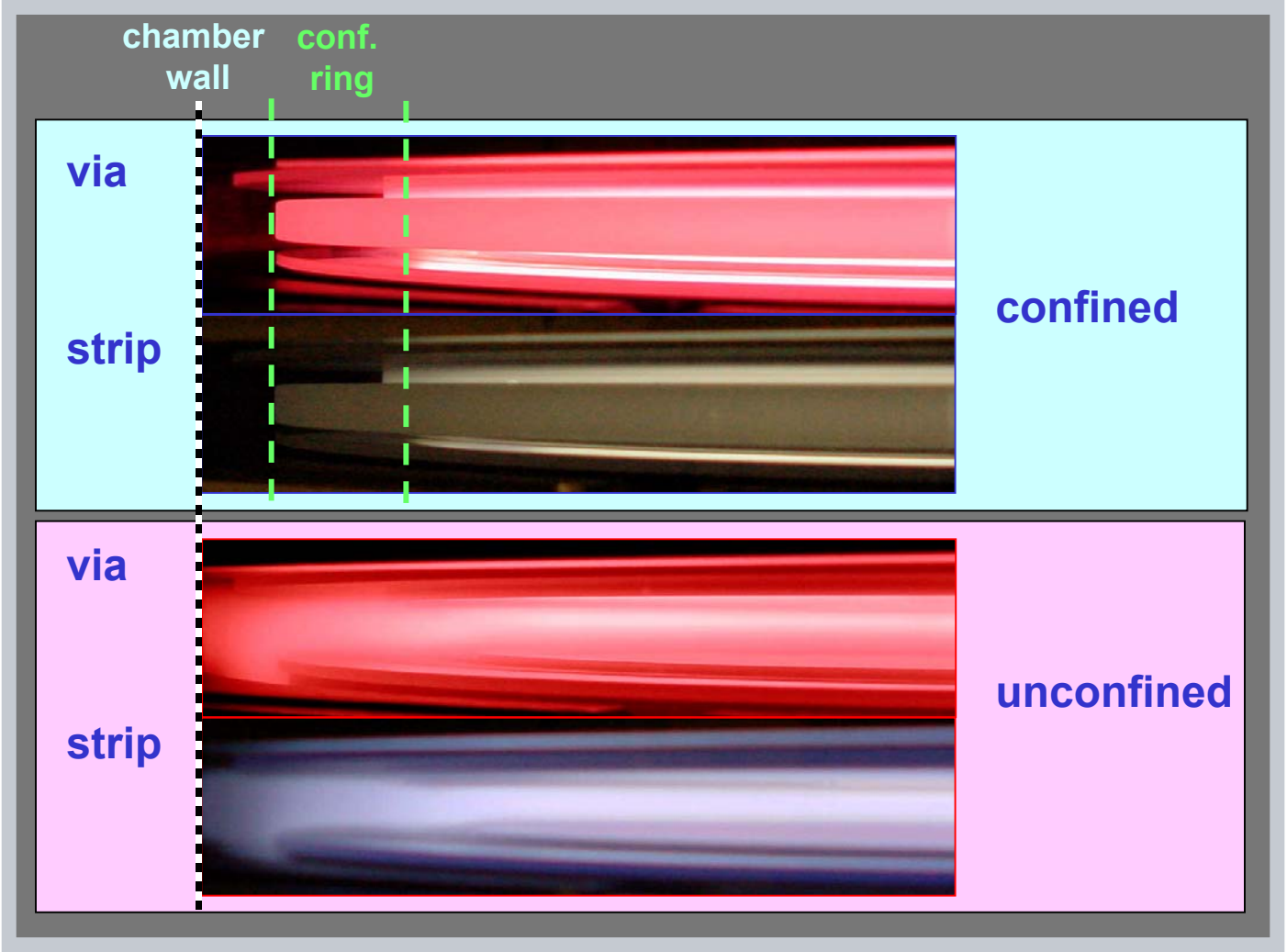
Dielectric etch technology: Confined plasma, con't

- Physically confined plasma
  - Plasma only interacts with small surface area, not with chamber walls
- Fluorocarbon polymer does not deposit on chamber walls
  - Only deposits on those surfaces in direct contact with confined plasma volume
  - Can re-set these surfaces to initial conditions using cleaning plasma, with or without wafer present



Dielectric etch technology: Confined plasma, con't

- Compare confined and unconfined reactor configurations

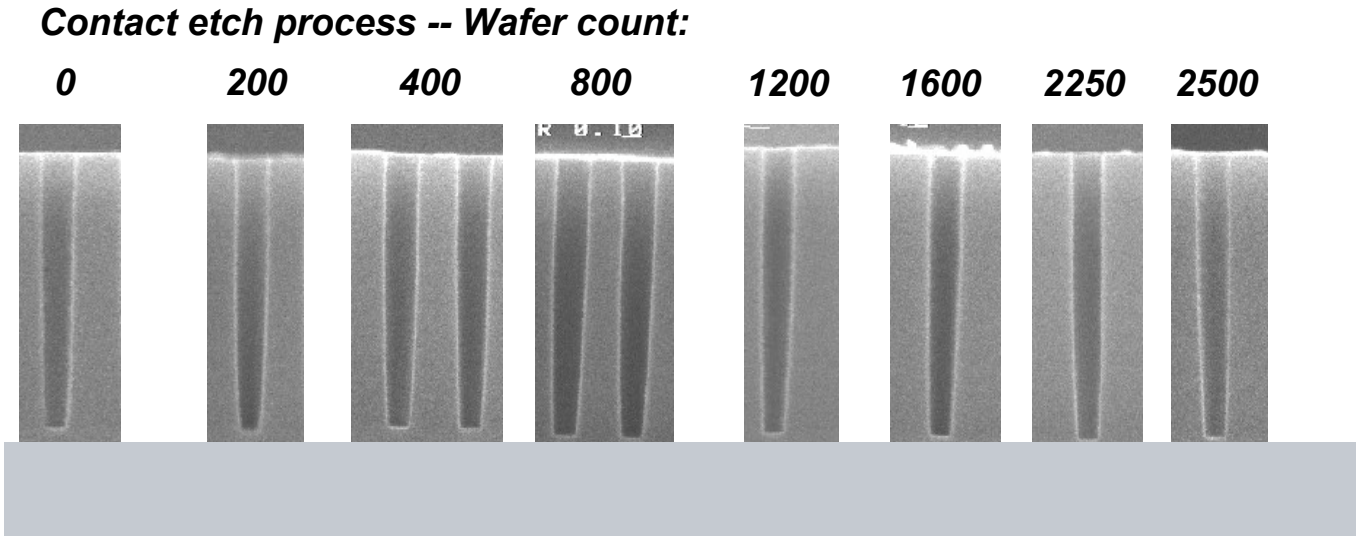


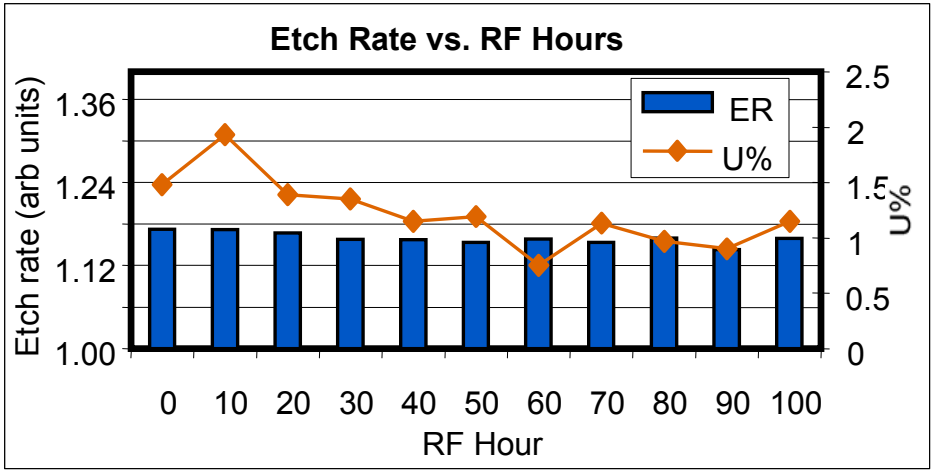
Dielectric etch technology: Process stability

- Process drift: Cumulative effect of wafer processing through production cycle
  - Reactor conditions change leading to drift in process results
- Polymer buildup on surfaces can cause process drift
  - Chemical -- Surface reactions can vary, affecting radicals in plasma
  - Electrical -- RF grounding to chamber walls can be influenced by polymer film
- *In situ* plasma clean
  - Either with no wafer present, or utilize PR strip step on wafer to also clean reactor
  - Effective at removing polymer from inner surfaces of confined volume
    - All reactor surfaces subject to ion bombardment
    - Density relatively high within confined volume
  - Can run short *in situ* clean after every wafer pass
- Provides very repeatable process conditions
- Good process stability
  - Allows more wafers between chamber "wet" cleans -- better tool utilization
  - Larger window for process development
- *In situ* clean also helps to control particulate formation

Dielectric etch technology: Process stability, con't

- Confined plasma and waferless *in situ* clean
  - Very reproducible plasma conditions
- Process results are stable over large number of wafers





<3% (3σ) variation in etch rate

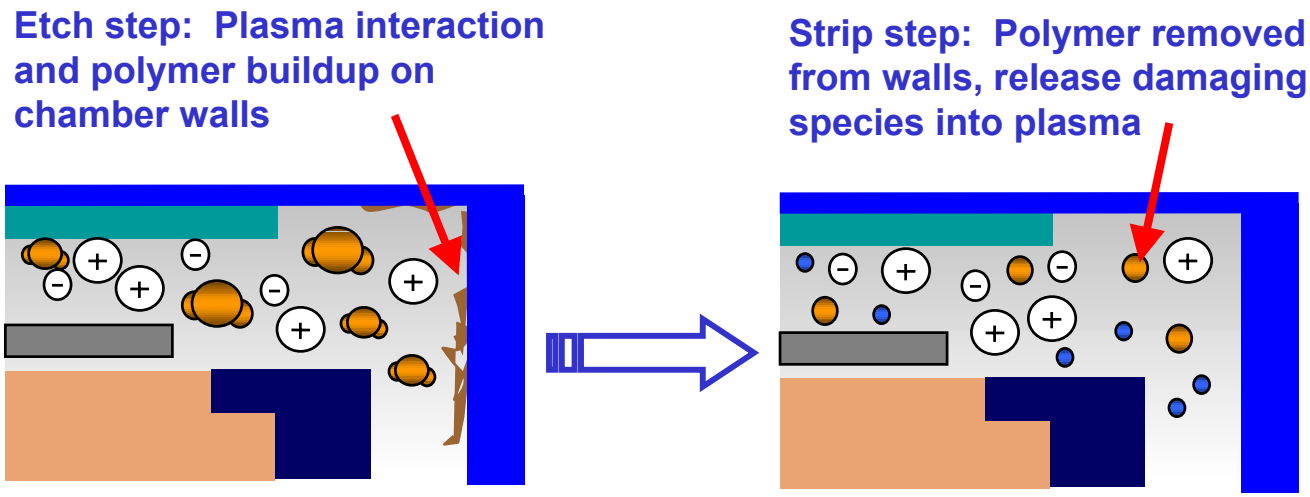
Dielectric etch technology: Integrated processing

- Dielectric etch applications often require successive removal of different films
  - Especially for dual damascene where stacks can be very complicated
- Advantages of multi-step *in situ* processing
  - Combine multiple etch steps into single pass through reactor
  - Reduces wafer handling, manufacturing cost, and cycle time

- But . . . Different types of films require different etch chemistries
  - Etch SiO_2 and other Si-containing films
    - Use polymerizing fluorocarbon chemistry to achieve high selectivity to other films
  - Strip photoresist or etch organic dielectric
    - Use oxidizing or reducing chemistry

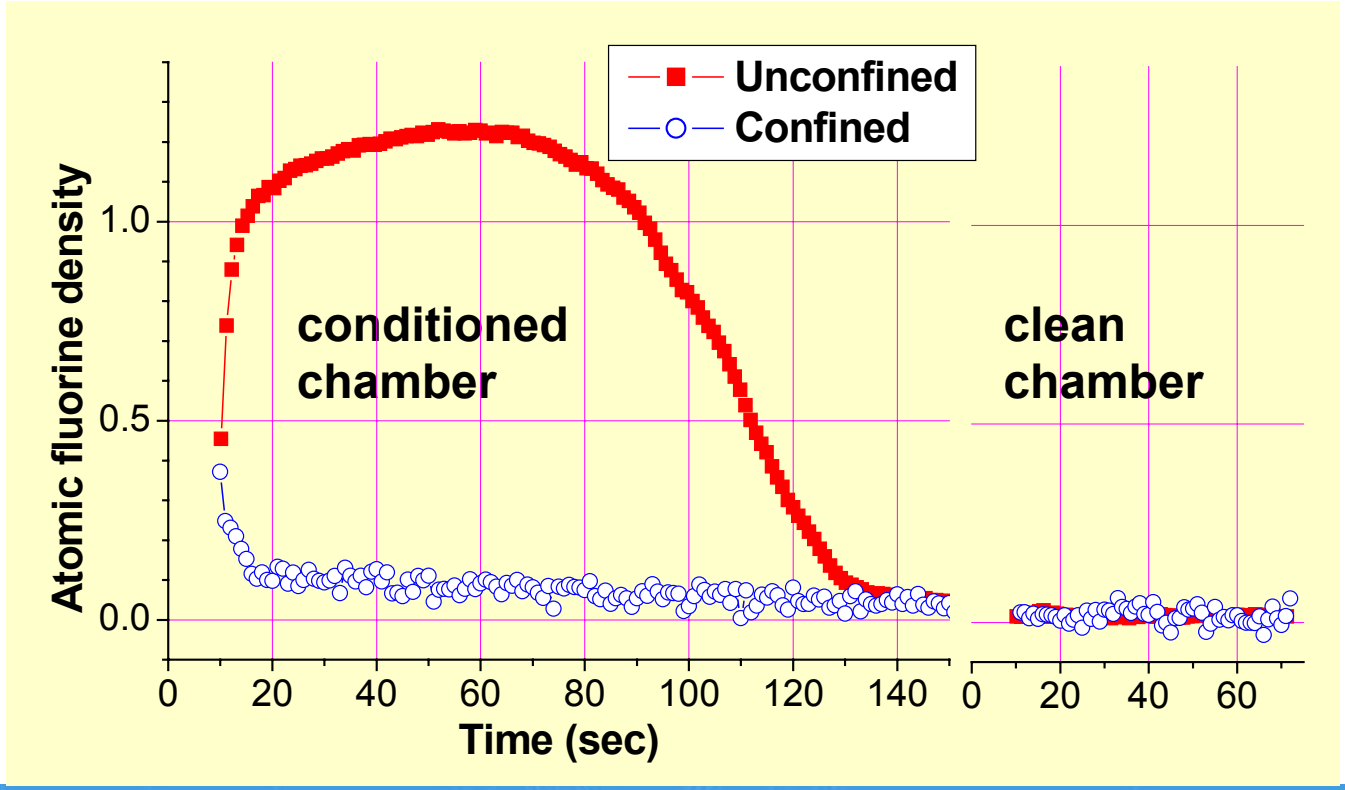
Dielectric etch technology: Chamber memory effect

- Possible issues with multi-step *in situ* processing
  - Chamber memory: Initial step modifies chamber condition, influences results of later process step
- Common situation which may lead to memory effect
  - Etch step: Polymerizing fluorocarbon conditions -- leave polymer residue on chamber surfaces
  - Resist strip step: Oxidizing chemistry which removes PR also removes polymer residue from chamber surfaces
    - liberates fluorine to plasma, which can modify or remove films on the wafer
    - "fluorine memory effect"



Dielectric etch technology: Fluorine memory effect

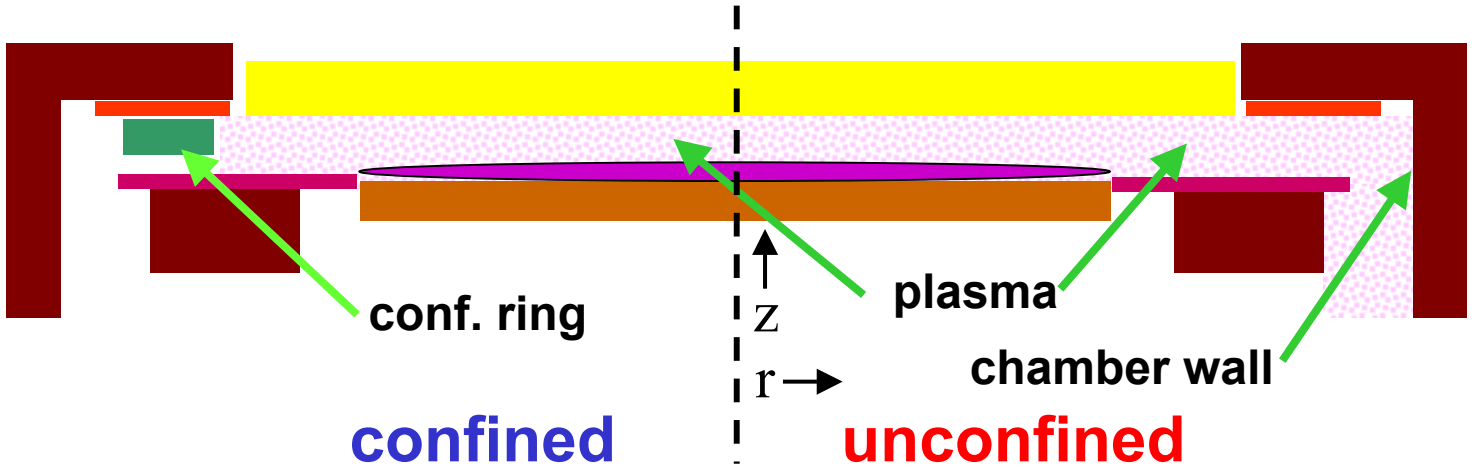
- Direct comparison of confined and unconfined configurations, on same test reactor
- Run PR strip after 300 sec conditioning with polymerizing via process
  - Use optical emission spectroscopy (OES) / actinometry to measure F density
- Unconfined case produces much higher F density
  - Clean chamber produces no F signal, confirms this is memory effect



"Memory effects for multi-step *in situ* plasma processing"
Eric A. Hudson, Rao Annapragada, Douglas Keil, Jie Zhou, and Kenji Takeshita
Dry Process Symposium proceedings (2003)

Dielectric etch technology: Fluorine memory effect, con't

- Why does unconfined case have worse memory effect?
- Gas residence time -- determines how long the strip by-products affect wafer
  - Unconfined, strip process, τ_{res} ~ 305 msec
  - Confined, strip process, τ_{res} ~ 11 msec (~28 times less than unconfined case)
- Surface area
  - Due to cylindrical symmetry, area of chamber surfaces outside confined volume is large
  - Unconfined plasma interacts directly with roughly 3.5x larger surface area than confined
  - More polymer is deposited in outer region in unconfined case, releases more fluorine during strip



Dielectric etch technology: Advanced process control

- Automatic correction of systematic process error
  - General trend in wafer processing, not just for dielectric etch
- In-line metrology for process monitoring and control
  - Integrate metrology and processing
  - Pre-etch measurement of wafer properties
    - Use to optimize etch process for current wafer: Feed forward approach
  - Post-etch measurement of wafer properties
    - Use to optimize etch process for following wafers: Feed back approach
    - Screen for problems -- Stop processing if results are out of specification
- Endpoint detection
  - Very small exposed areas for some etch applications (<0.5%), need high sensitivity methods
- Multivariant analysis of tool sensor data
  - Detect failures
  - Predict failures
  - Diagnose failures

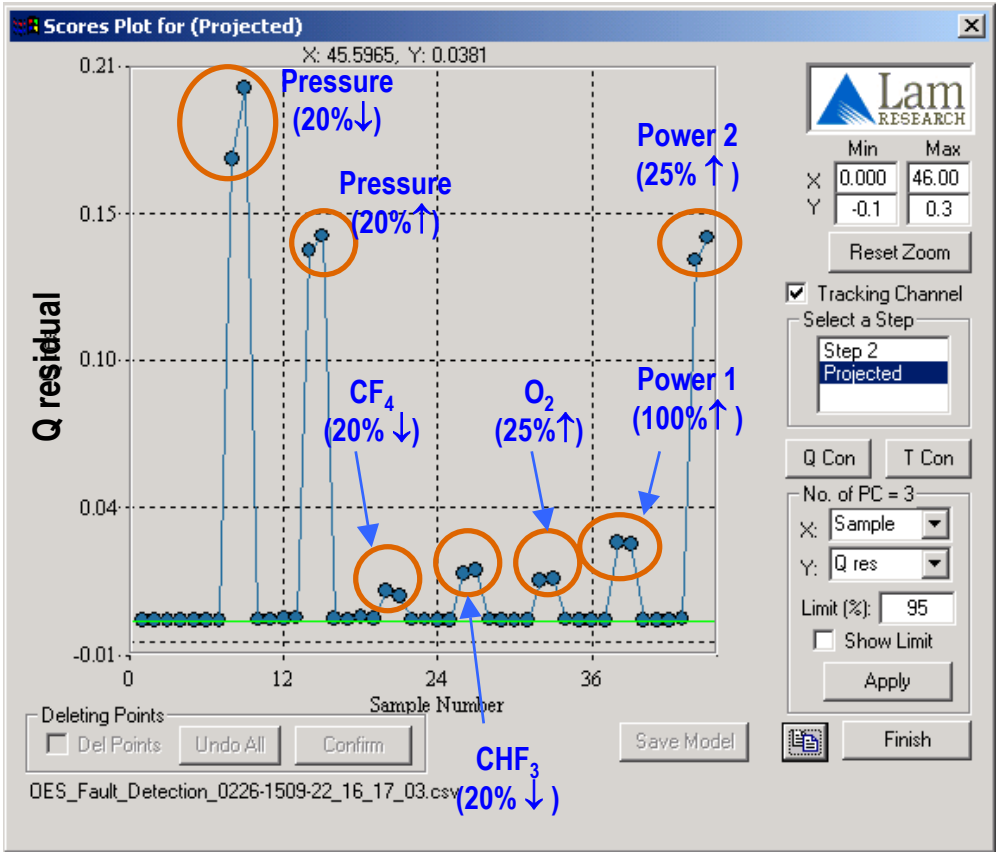
Dielectric etch technology: Fault Detection

- Example -- Fault detector for errors in process or recipe parameters
- Use Principal Component Analysis (PCA) of optical emission spectra (OES)
  - Show results of test
- Build PCA model using baseline wafers
  - Apply model to subsequent runs
  - Project real-time data onto model and examine Q-residual statistic
- Run series of wafers with normal and “fault” recipes
  - Vary pressure, power, flows in recipe to simulate tool fault

“Application of PCA / PLS to Optical Emission Spectra for Plasma Etch Process Monitoring”
Hyun-Ho Doh, Phoebe Wang, Ning Xu, Puneet Yadav, Enrico Magni, and Brian McMillin
2003 AEC / APC Symposium XV, Colorado Springs.

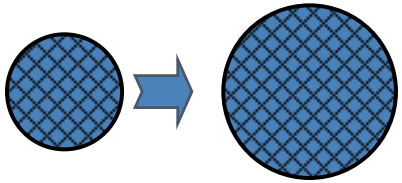
Dielectric etch technology: Fault Detection, con't

- Build model using OES full spectra acquired from normal recipe wafers
  - 31 wafers, 3PCs, 99.9% variance
  - Run recipes variations, track Q residual

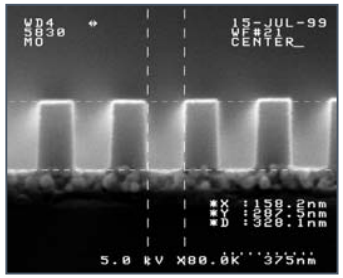


- Q-residual detects all induced faults in oxide trench recipe
  - Q is reflecting change in plasma chemistry rather than simple intensity change since all spectra were normalized prior to PCA
- Results show sensitivity of this method
  - Can easily detect much smaller changes

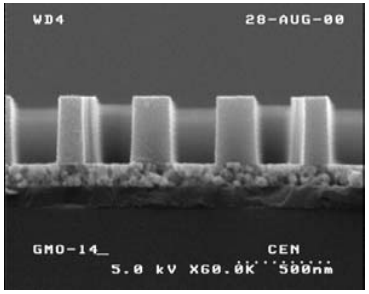
Dielectric etch technology: 300 mm wafers



- Industry change from 200 to 300 mm wafers
  - ~2.3x more die/wafer, but requires all new equipment
  - Some companies in large scale production, many others in preparation
- Larger capital investments ⇒ better risk management
  - 200 ⇒ 300 transition using same reactor, same platform, to minimize risk
- Challenges for all critical fabrication steps including etch
  - Tightening specifications: e.g. for defects
  - Transition to 300 mm at ~130 - 65nm nodes, which have their own challenges
- Scaling issues for etch
  - Transfer results from 200 to 300 mm with minimum change to process and hardware



200 mm

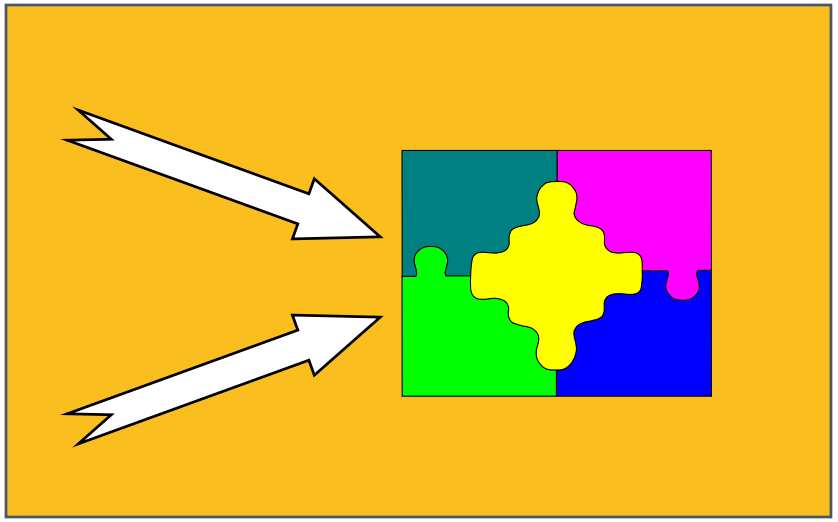


300 mm

Gate Mask Open:
--Same gas chemistry
--Similar pressure
--Increased RF power

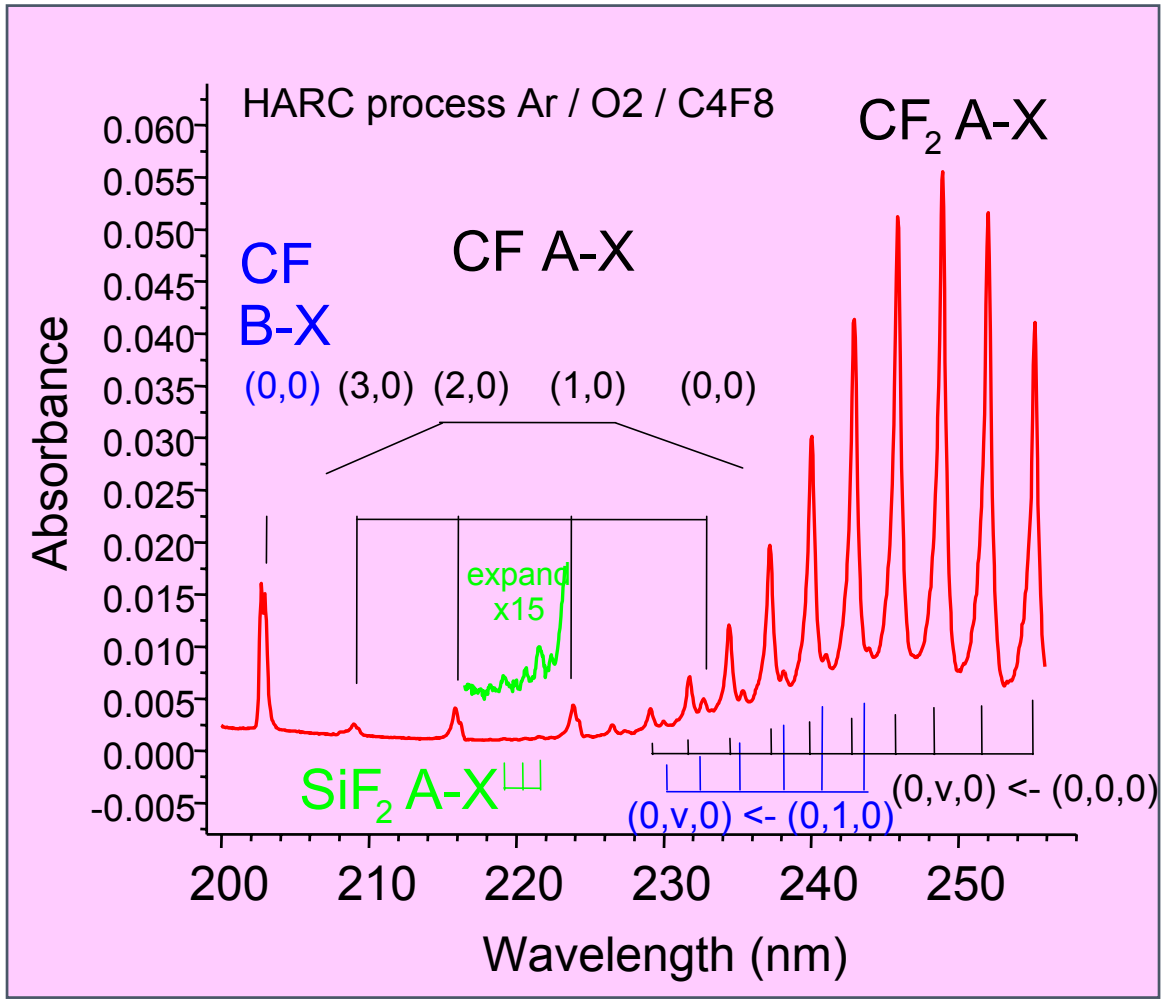
Dielectric etch technology: Product development

- Change in approach to product development
  - Less reliance on empirical methods, trial-and-error development
  - More emphasis on basic understanding of plasma properties and etch mechanisms
  - Reduce development cycle time, improve final performance
- Apply methods from academic and government labs directly to commercial etch systems
  - Need results from real industrial configurations, not just idealized cases
- Modeling
  - Particle and global plasma
  - Gas transport
  - Etch profile evolution
  - Chemical kinetics
- Plasma diagnostics
  - Electrical probes
  - Optical spectroscopy
  - Mass spectrometry



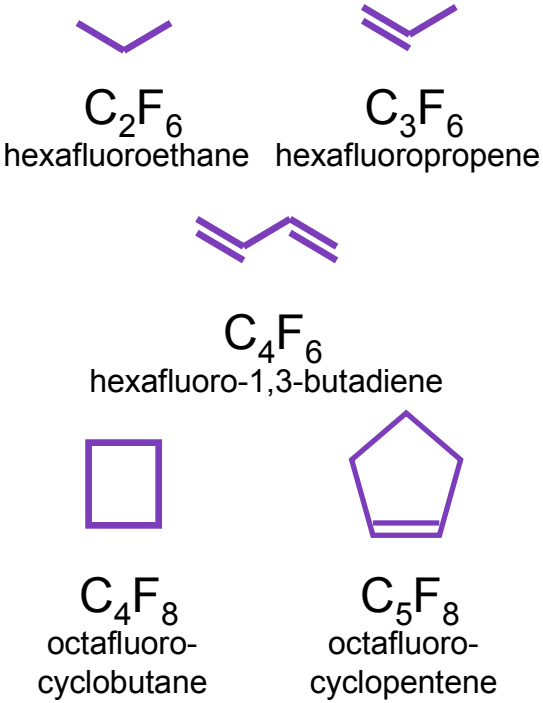
Dielectric etch technology: Optical diagnostics

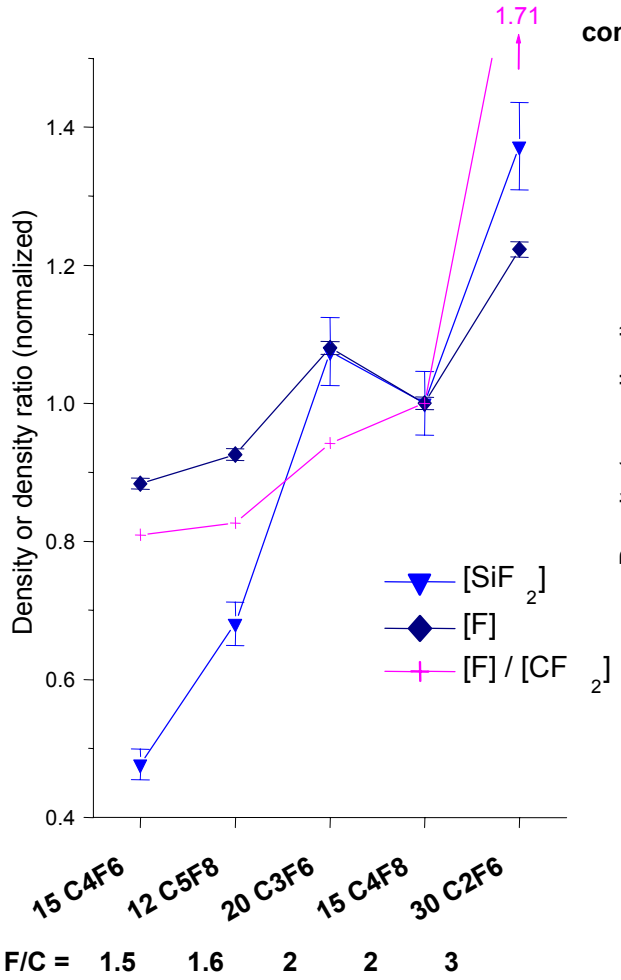
- UV absorption spectroscopy (UVAS)
  - Measure absolute radical densities in plasma
  - Detect multiple species
  - Non-invasive method
- Study variation of radical densities
  - Relationship between radical densities and:
    - Process parameters
    - Reactor hardware
    - Reactor conditions
    - Etch results

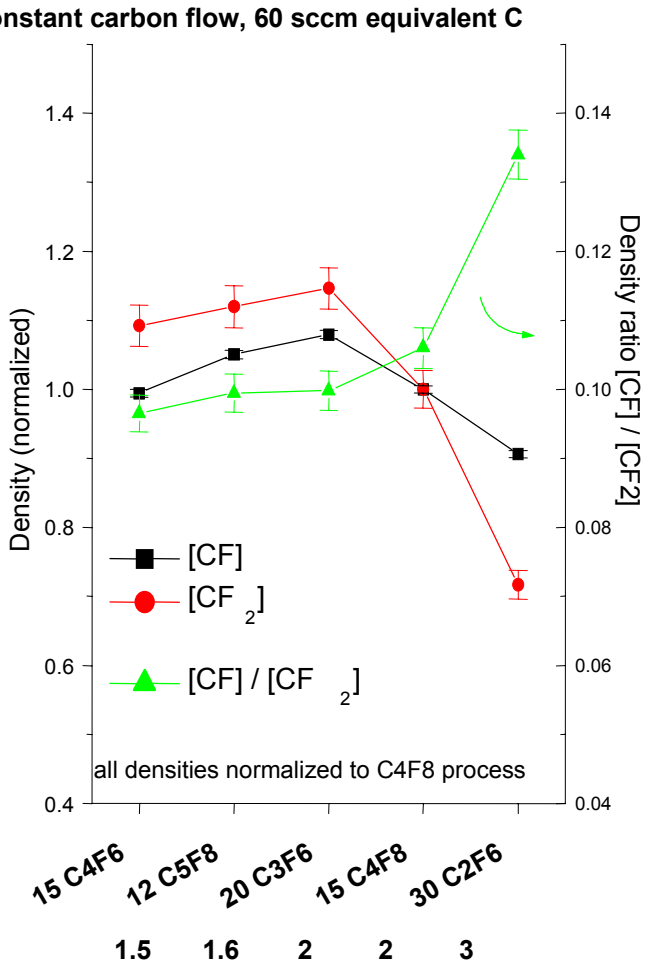


Dielectric etch technology: Diagnostic study of feed gas

- Use baseline process typical for contact etch
- Measure radical densities using UVAS and OES
- Compare different fluorocarbon feed gases







"Dependence of radical densities on fluorocarbon feed gases in a dielectric etch plasma"
E. A. Hudson, J. Luque, N. Bulcourt, J. P. Booth
American Vacuum Society 49th Int'l Symposium, November 2002

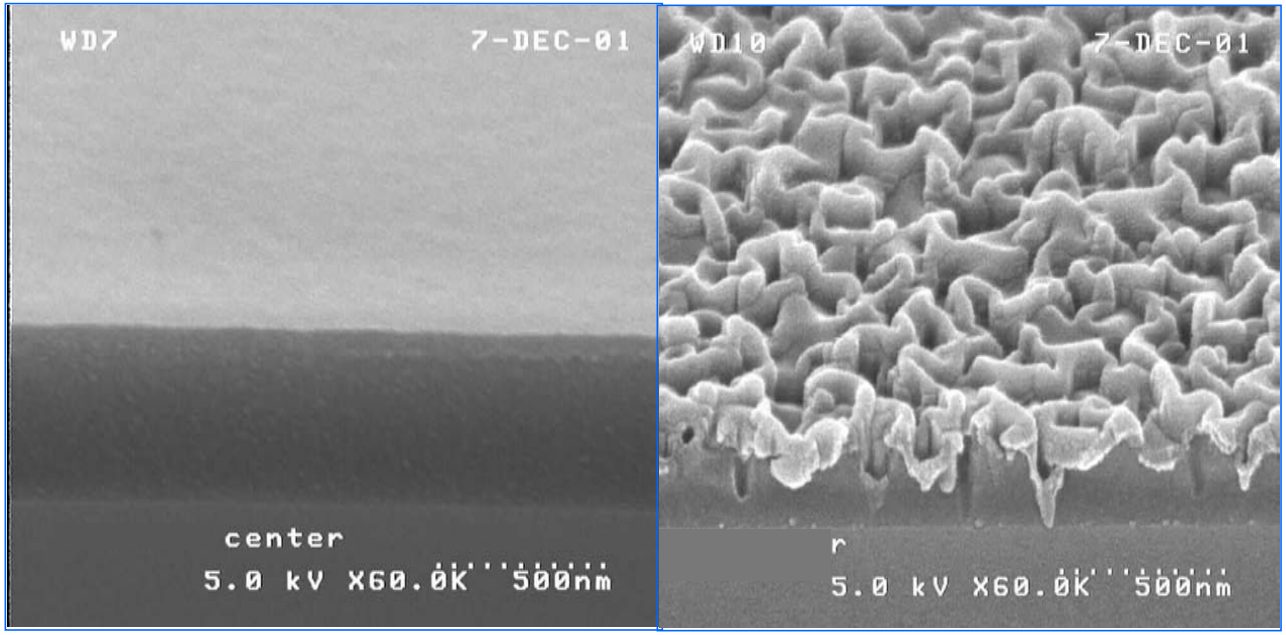
Applications: Continual reduction of design rule

- Smaller nodes ⇒ Changing requirements for etch
  - Tighter CD and profile control
  - Larger aspect ratio structures (film thickness does not scale with CD)
  - General need to provide much tighter control of process due to demanding requirements
- 90nm ⇒ 65nm ⇒ beyond
  - 193nm photolithography may be required for 90 and 65nm nodes
  - 157nm photolithography may be required for 65 and 45nm nodes
  - Bilayer resist approach can extend PL by one node (e.g. 193nm PL for 65nm node)
    - But introduces its own challenges, adds dry develop as new etch application
- New photoresist materials required for 193nm and 157nm
  - Challenges for etch (and for lithography)
  - 193nm PR materials are very different from previous generations
    - Must be thinner due to wavelength limitations
    - Require higher selectivity to photoresist than for previous generations
    - Lower resistance to etch conditions -- tendency to roughen and distort

"Integrating dielectric etching with 193nm resists"
S. Lassig and E. Hudson, *Solid State Technology* Vol. 45, No. 10 (October 2002)

Roughening of 193nm PR

- 193nm PR is much more sensitive to plasma exposure, compared to DUV PR (248nm)
  - Same process, optimized for DUV, gives very different result



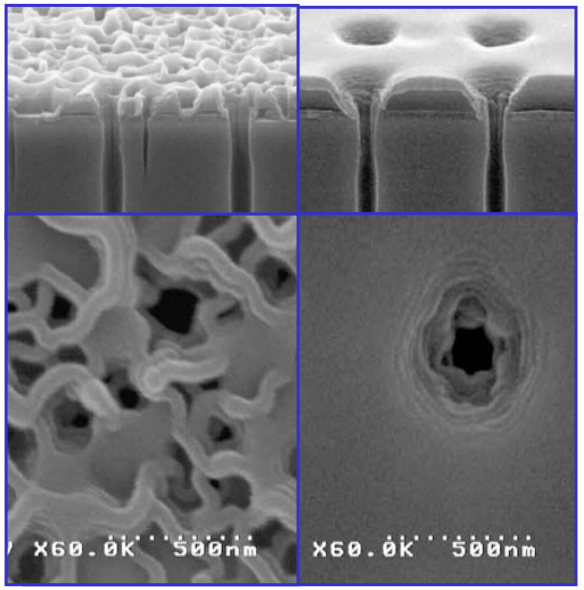
248nm PR

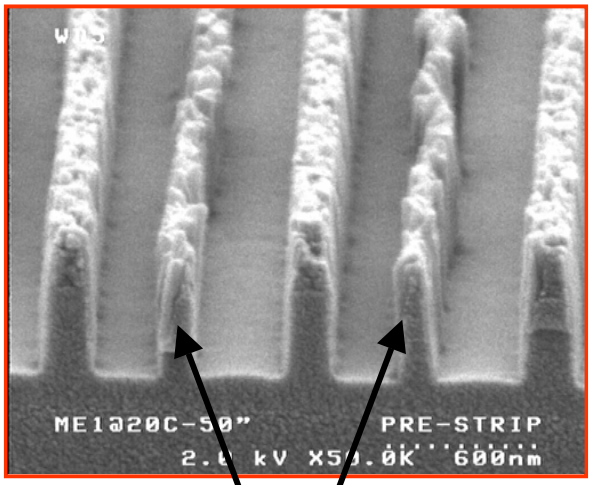
193nm PR

Polymerization can prevent roughening . . . but cause distortion

- Shifting to more polymerizing plasma conditions can sometimes prevent roughening of 193nm PR
  - Example shown for contact etch

More polymerizing →



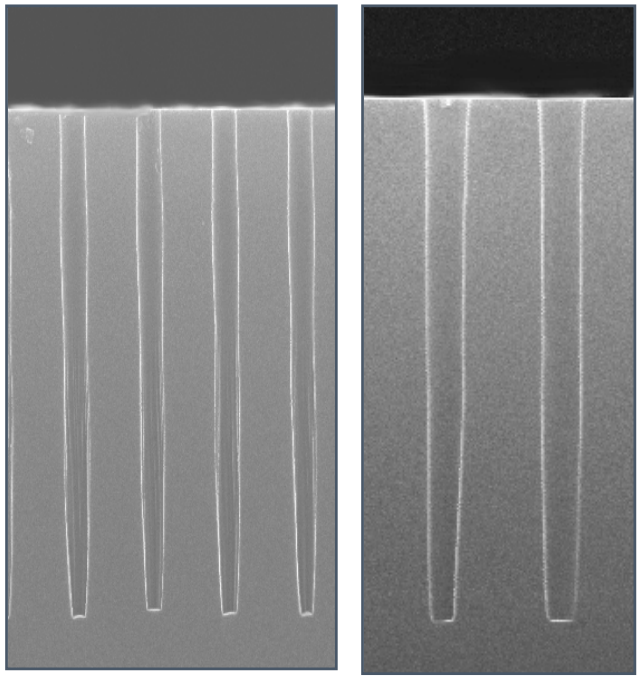


Wiggling

- But thin lines of 193nm PR tend to distort if process is too polymerizing
- Causes line wiggling or weaving
  - Example shown for trench etch, for thinnest lines

FE Applications: High Aspect Ratio Contact (HARC)

- Memory applications --
  - Often include tall capacitive storage structures
    - Require very thick dielectric film (>2.5μm)
  - Aggressive design rules to maximize die/wafer
    - Decreasing lateral dimensions
  - Aspect ratios ~15:1 are now in production worldwide
- Challenging requirements
  - Tight CD control (Δ<10nm)
  - Vertical profile (89-90º)
  - High oxide : photoresist selectivity
    - >8:1, increasing to 15:1 (at facet)
    - ∞:1 bulk selectivity (do not etch PR)
  - Avoid striations, etch stop and process drift
- Rely mainly on unsaturated fluorocarbon feed gases

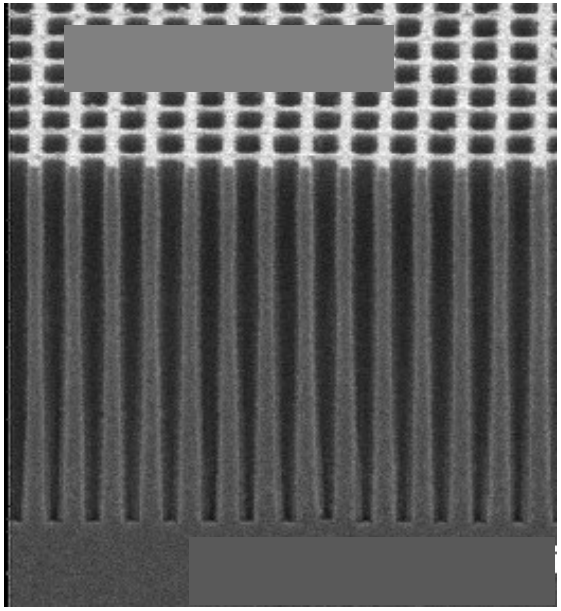


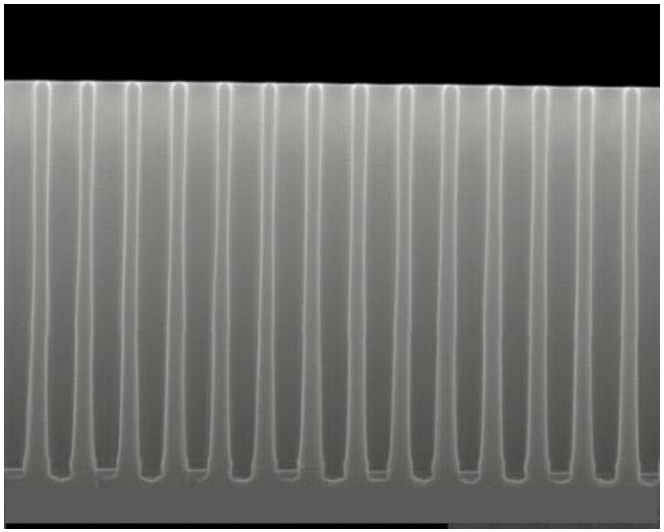
BPSG HARC
17:1

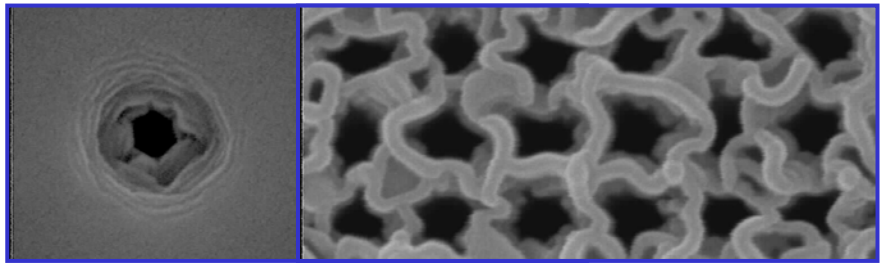
TEOS HARC
10:1

FE Applications: Container

- Container structures -- similar to HARC
  - Etch high-aspect ratio holes
  - To be filled with polysilicon, used as memory capacitors
- Large, dense arrays of structures
  - Very small spacing between holes
  - Wall thickness less than hole size
- Tight spacing ⇒ challenging application
  - Cannot tolerate profile bowing or CD blowout
  - Thin PR between holes etches at accelerated rate
  - Small width can also cause PR to distort
    - Can use novel plasma conditions to prevent this

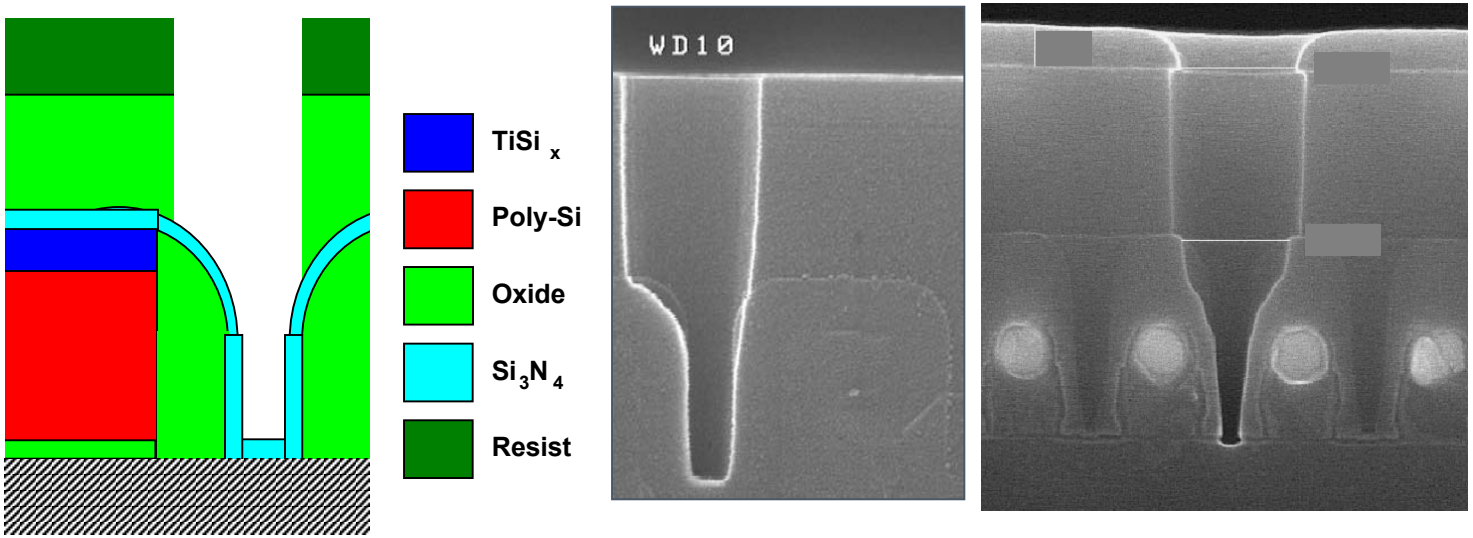






isolated dense (same process)

FE Applications: Self-Aligned Contact (SAC)

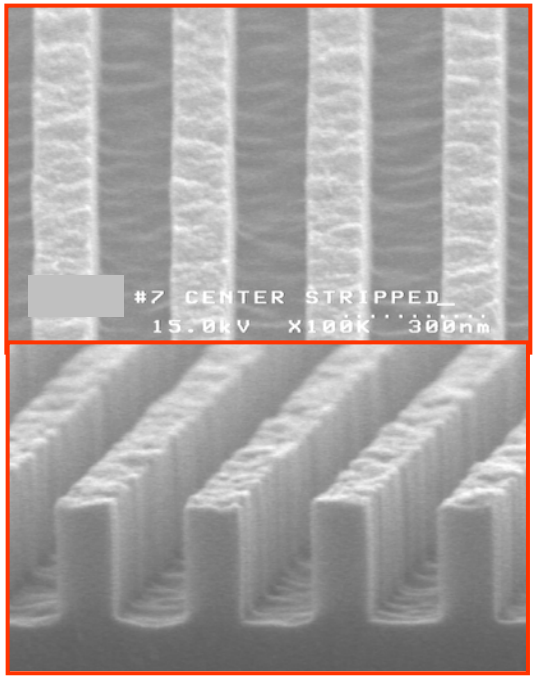


>25 : 1 selectivity

- Structure allows some misalignment of lithographic pattern
- Need high selectivity to corner nitride
  - This shoulder is exposed while oxide etch finishes
    - Sloped surface is prone to sputtering, difficult to protect
  - Typical requirement is 20:1 selectivity (oxide : corner nitride)
- Avoid etch stop in bottom feature which has very small CD

FE Applications: Gate Mask Open

- Nitride hard mask
  - Used to define pattern for polysilicon gate etch
  - Pattern PR, etch nitride, before etching polysilicon
- Becoming more challenging application due to thinner PR and small CD
  - Large exposed nitride area -- different process regime as compared to HARC and SAC
  - 193nm photoresist presents difficulties due to possible roughening and distortion of resist mask during etch



- 110nm gate mask
- <3nm CD bias
- Profile Angle 90-89º
- Minimal line edge roughness

Key requirements:

CD control

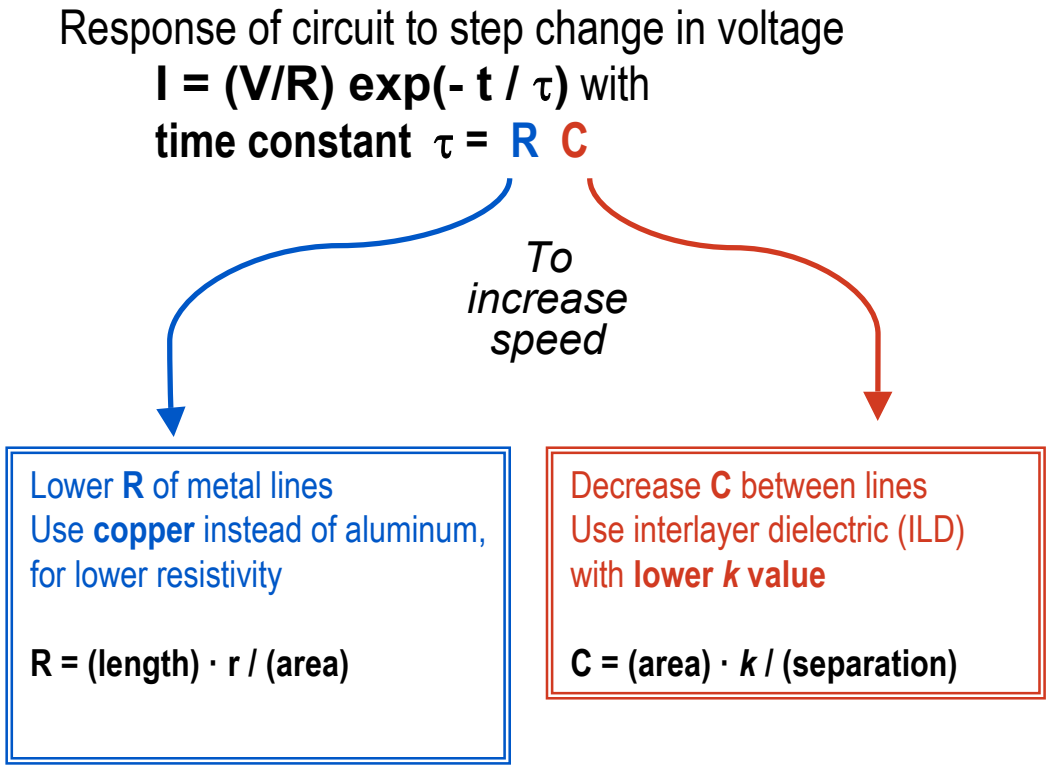
No line edge roughness

Vertical profile

"Control of Line Edge Roughness for Etching with 193nm Photoresist"
Eric A. Hudson, Zhenxi Dai, Zongyu Li, Sean Kang, Sangheon Lee, Wan-Lin Chen, and Reza Sadjadi
Dry Process Symposium proceedings (2003)

BE Applications: Low-*k* dielectric / copper interconnect

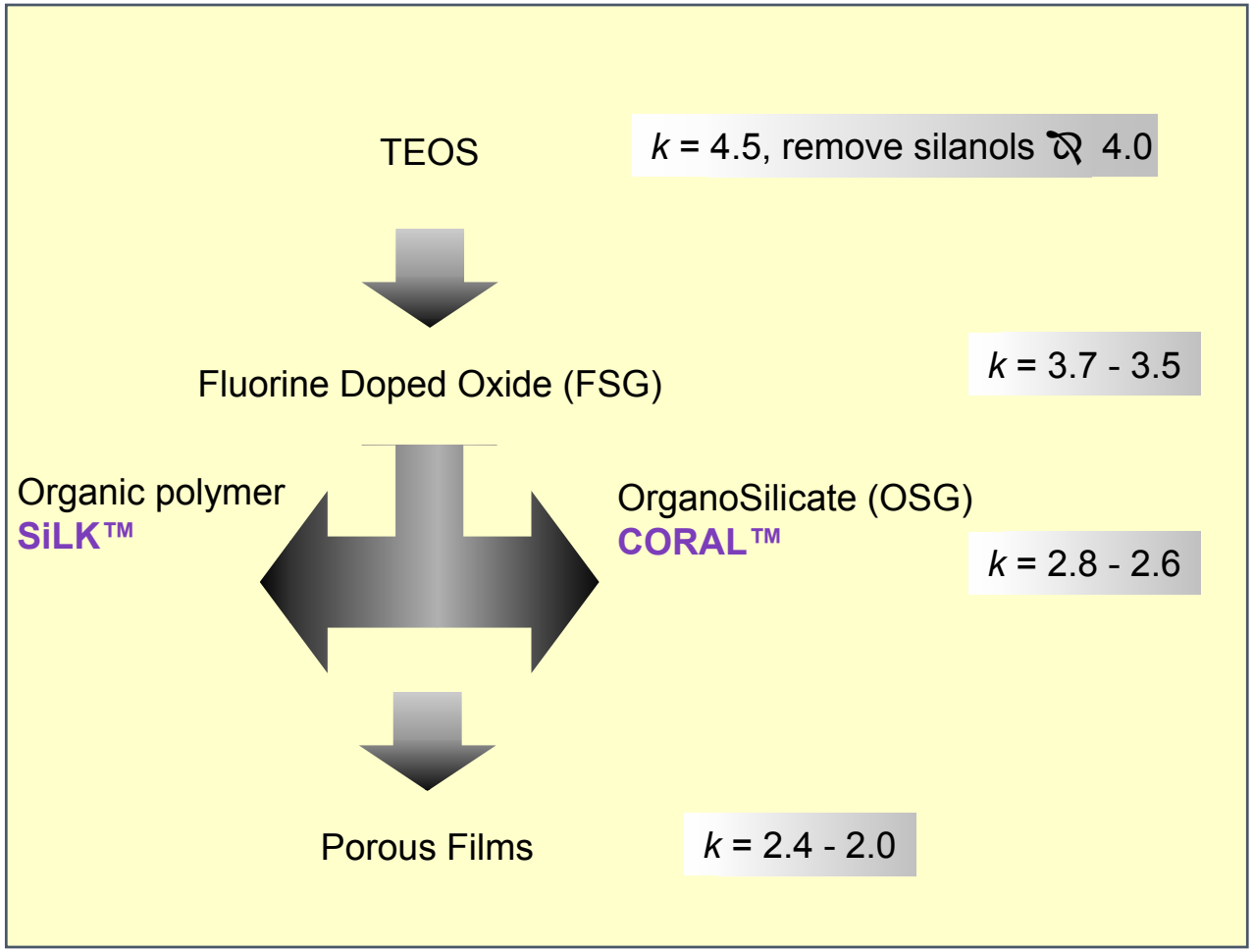
- **Focus on back end to improve IC speed**
  - **Transistors have improved switching time, less of a limitation**
  - **More interconnect layers, longer paths in IC designs**
  - **Smaller design rule**
    - **Drives smaller cross-section area of interconnects**
    - **Smaller separation between lines, more chance for crosstalk as frequency increases**



These are both MAJOR changes to IC fabrication and both transitions are happening in parallel

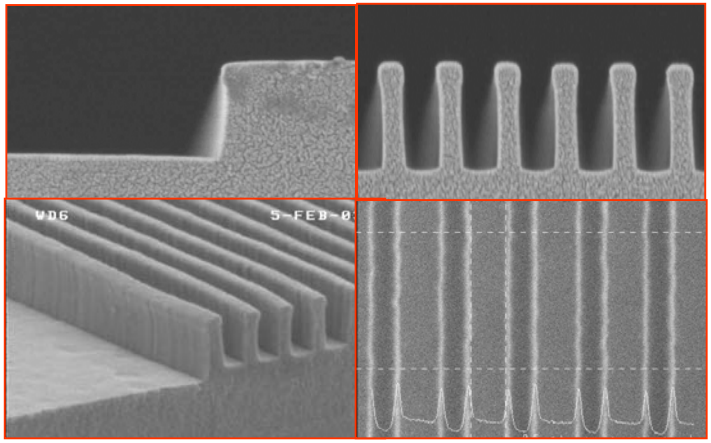
BE Applications: Low-*k* dielectric materials -- examples

- **FSG**
  - **Widely used in production**
- **OSG**
  - **In production**
- **Organic**
  - **In production**
- **Porous**
  - **Still in R&D**

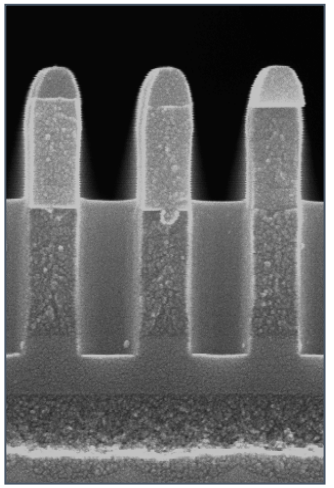


BE Applications: Etching low-*k* dielectrics

- FSG: Minor changes from SiO_2 (TEOS) processes
- OSG: Larger changes from TEOS process
  - N_2 often used instead of O_2
  - Carbon produced during etch, can promote etch stop
  - Typical issues -- bowing, residue at etch front (grass)
  - Conversion of OSG to oxide on sidewall (damage)
- Organic polymer: Use reducing chemistry, e.g. N_2 / H_2
  - Not a fluorocarbon process!
  - But integration involves etching Si-containing masks and barriers, still need fluorocarbon for those steps
  - Typical issues -- faceting, bowing, residue at etch front
- Porous films
  - Similar to non-porous version of film (organic vs OSG)
  - Etch front control more difficult, need DD trench stop layer
  - Main challenges lie in formulation and deposition, to control pore size and structure

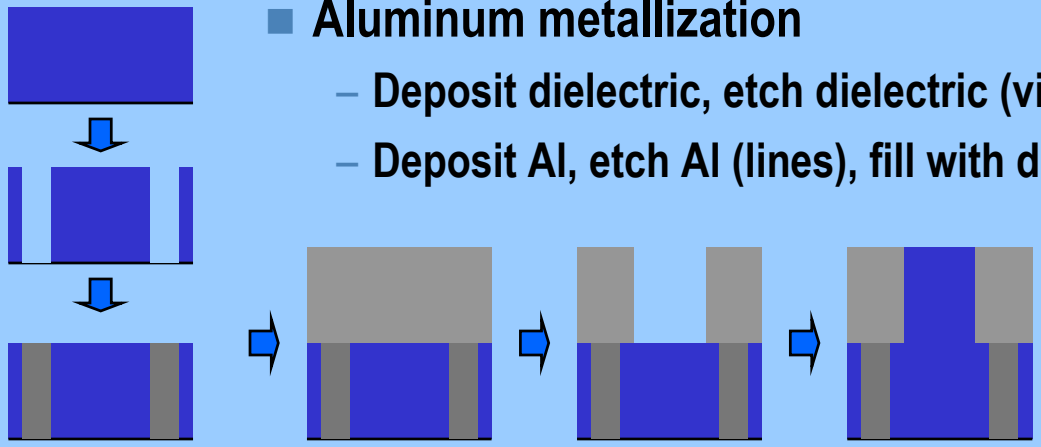


OSG trench



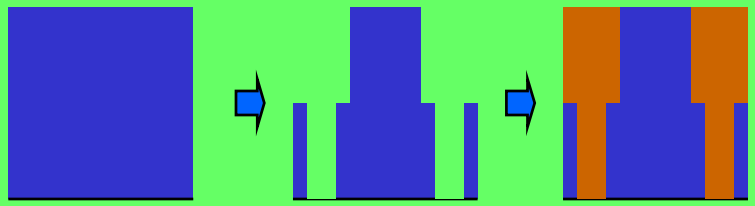
Organic DD

BE Applications: Copper and Dual Damascene concepts



- Aluminum metallization
  - Deposit dielectric, etch dielectric (via holes), fill with W
  - Deposit Al, etch Al (lines), fill with dielectric

- Copper metallization
  - Can't dry-etch Cu
  - Deposit dielectric, etch trenches & vias
  - Fill with Cu
  - Reduces number of fabrication steps

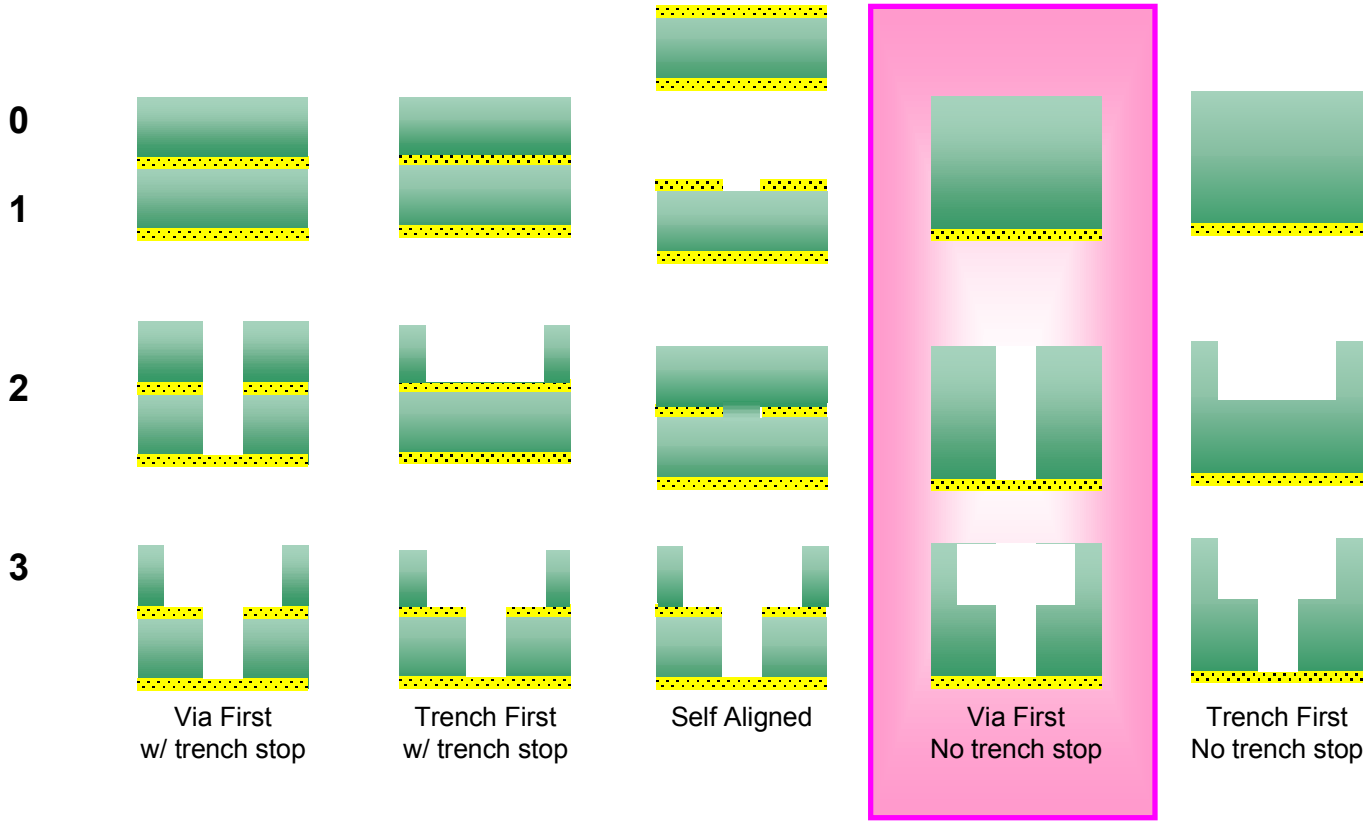


Trade metal etch for dielectric etch

Create new class of dielectric etch applications

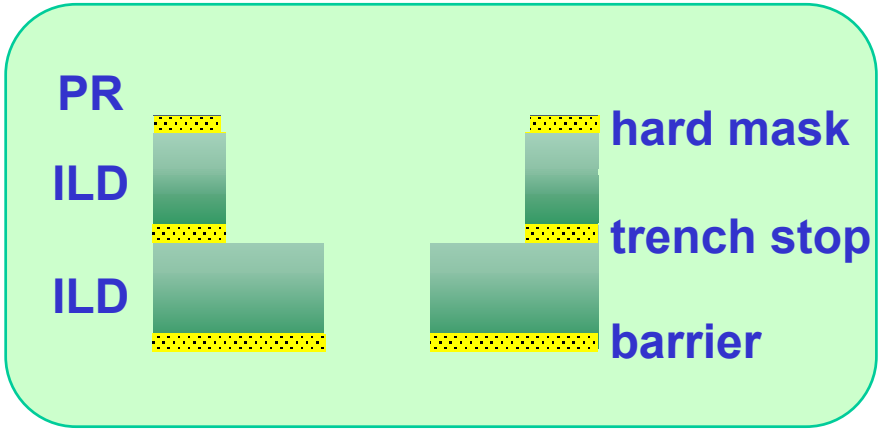
BE Applications: Dual Damascene integration schemes

- A few simple examples
  - Via First with no trench etch stop layer is a popular approach
  - Schemes can be much more complicated than those shown here



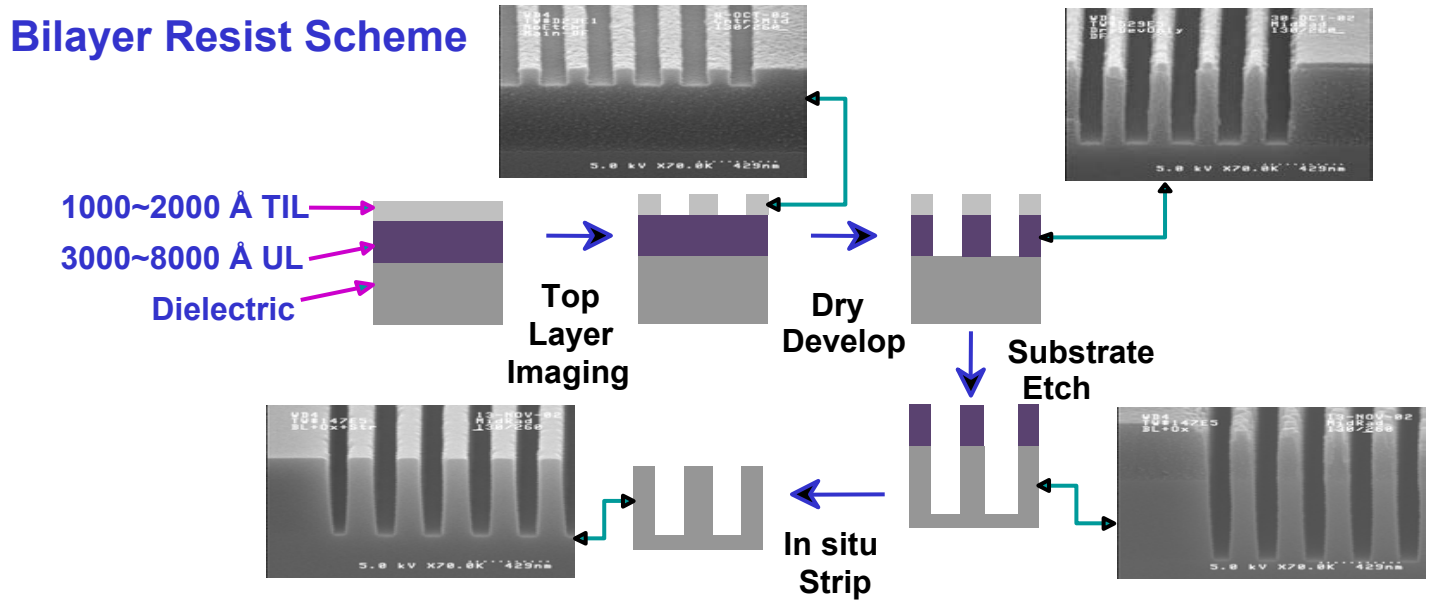
BE Applications: Dual Damascene integration, con't

- Barrier and trench stop dielectric layers
  - SiC is replacing SiN_x due to lower *k* value
  - Etch selectivity for OSG:SiC and OSG:SiN_x is a challenge
  - Need reverse selectivity to remove SiN_x or SiC with selectivity to OSG or oxide
  - If there is no trench etch stop layer
    - etch front must be very flat
    - etch rate must be uniform across wafer



- Hard masks
  - Multiple hard masks may be used to transfer pattern from resist to low *k* dielectric
  - Metallic hard masks are being introduced to avoid some problems of 193nm photoresist
    - This can be challenging due to metal-containing residues in chamber

BE Applications: Multi-layer resist



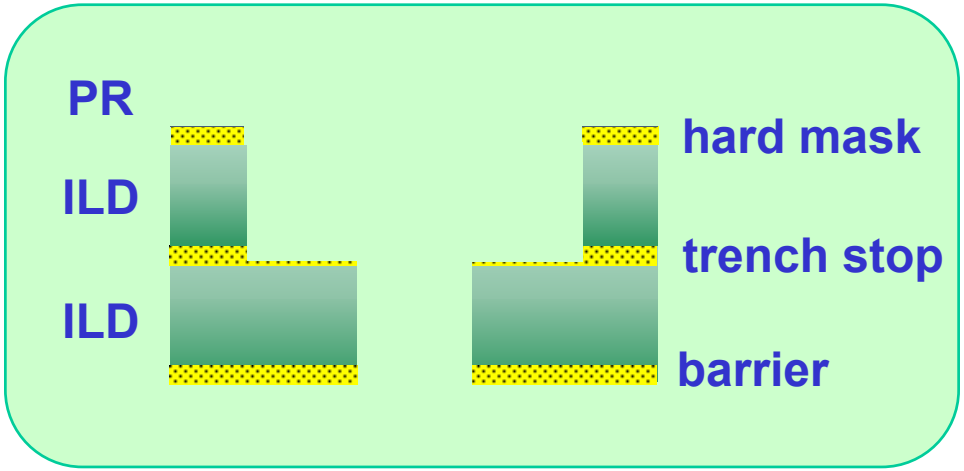
"Bilayer Material and Process for Dual Damascene Processes and Manufacturing of Advanced Devices"
P. Cirigliano, R. Sadjadi, A. Athayde, G. Barclay, J. Wandell, and F. Fischer
(To be published)

- **Multi-layer photoresist -- may become important approach**
  - **Separates the roles of photolithography and etch resistance**
- **Bilayer approach**
  - **Spin on top imaging layer (TIL) and under layer (UL), pattern TIL using photolithography**
  - **Use etch tool to "dry develop" the pattern from TIL to UL (TIL contains silicon)**
  - **UL acts as mask for subsequent etching**
  - **Lowers cost by delaying transitions to 193nm, 157nm lithography**
  - **Avoid some issues of single-layer resist -- roughening, line edge roughness**

BE Applications: Multi-step processing

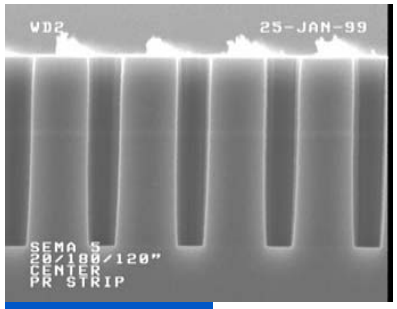
- DD applications often require successive removal of different films
  - Dual damascene (DD) trench example:

⑦open SiN_X or SiO_2 hard mask / masks
⑦etch FSG or OSG interlayer dielectric
⑦strip photoresist
⑦open SiC or SiN_X diffusion barrier at via bottom / remove trench stop layer



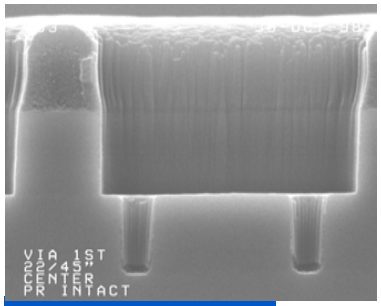
- Combine multiple etch steps into single pass through reactor
  - *in situ* process approach reduces manufacturing cost and cycle time
  - Becomes very important for advanced logic integration schemes, where there can be more than 10 distinct films in a single stack which need to be etched!
  - Control of chamber memory effects is critical
  - Need very flexible etch system, to meet different requirements of each step
    - Tend to use variety of different etch gases

BE Applications: Via 1st Integrated DD Etch: FSG film

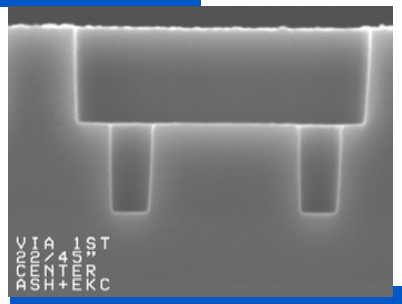


1. Via etch

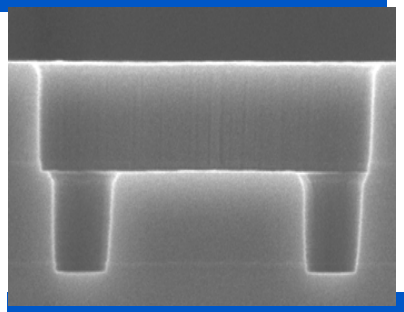
After photolithography for trench pattern



2. Trench etch



3. *In-situ* photoresist strip



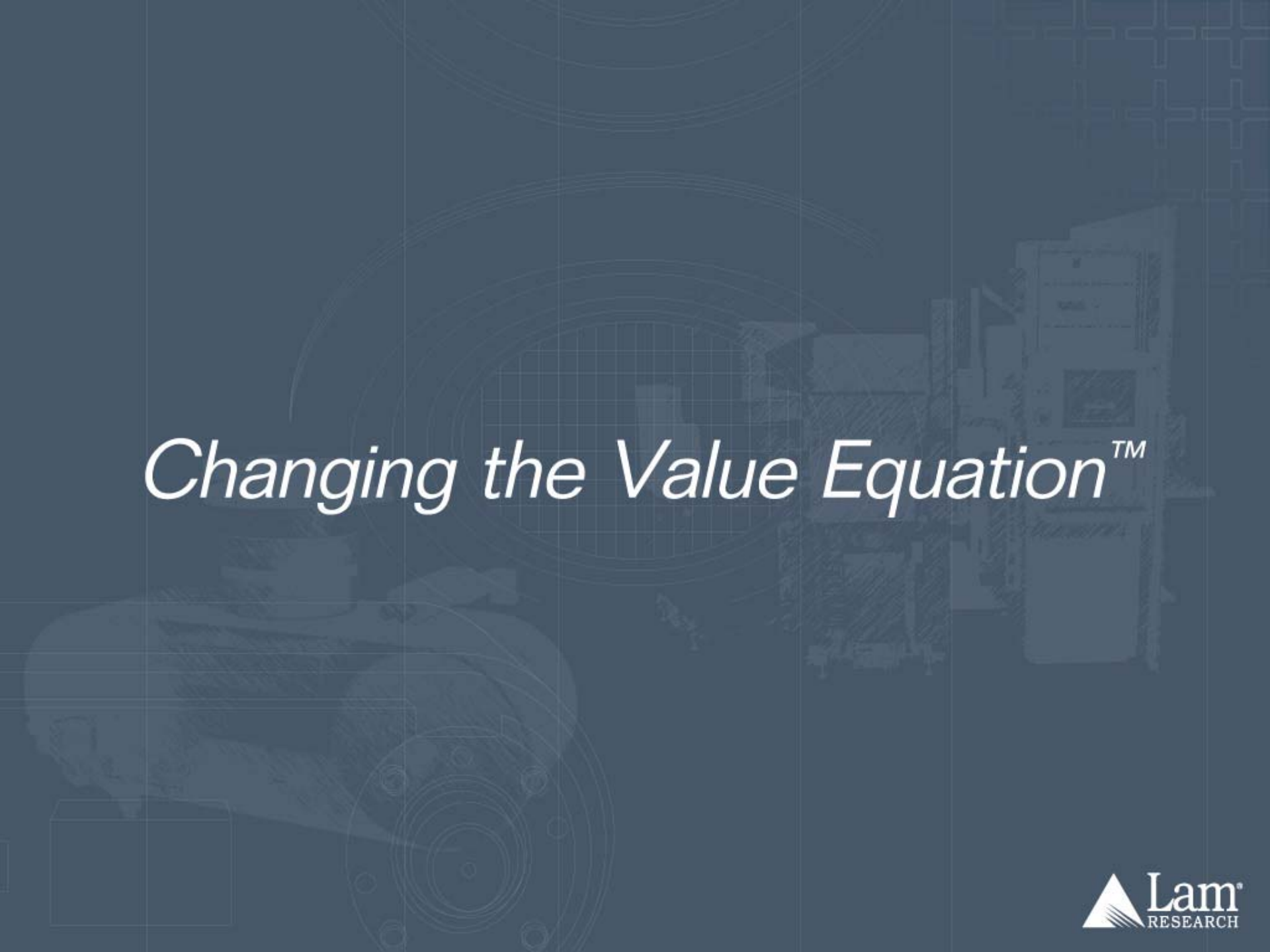
4. *In -situ* barrier removal

- Integrated process for steps 2-4
  - Strip must occur *before* barrier removal, to protect Cu from O_2 plasma
- Etch Issues
  - Avoid residue around top of via
  - Minimize rounding at top of via
    - More difficult without trench stop layer
  - Remove barrier without damaging Cu or coating via walls with Cu

Conclusions

- Dielectric etch technology
  - Dual-frequency capacitive RF
  - Confined plasma for process stability and minimal chamber memory effect
  - Diagnostics and modeling play growing role in product development
  - Advanced process control
- Trends in DE applications
  - New photolithography methods introduce etch challenges -- photoresist stability
  - Front end
    - High aspect ratio structures (HARC , Cell) and Gate mask open are critical
  - Back end / interconnect
    - Major changes due to low-k dielectrics and Dual-Damascene integration
    - Integrated processing -- complicated film stacks
    - Need flexibility to handle many different materials in single etch tool

- Acknowledgements:
  - Dielectric Etch and New Product Development groups at Lam Research Corp.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