

# **The Demands of Advanced Lithography - ESH issues in the Lithographic Process**

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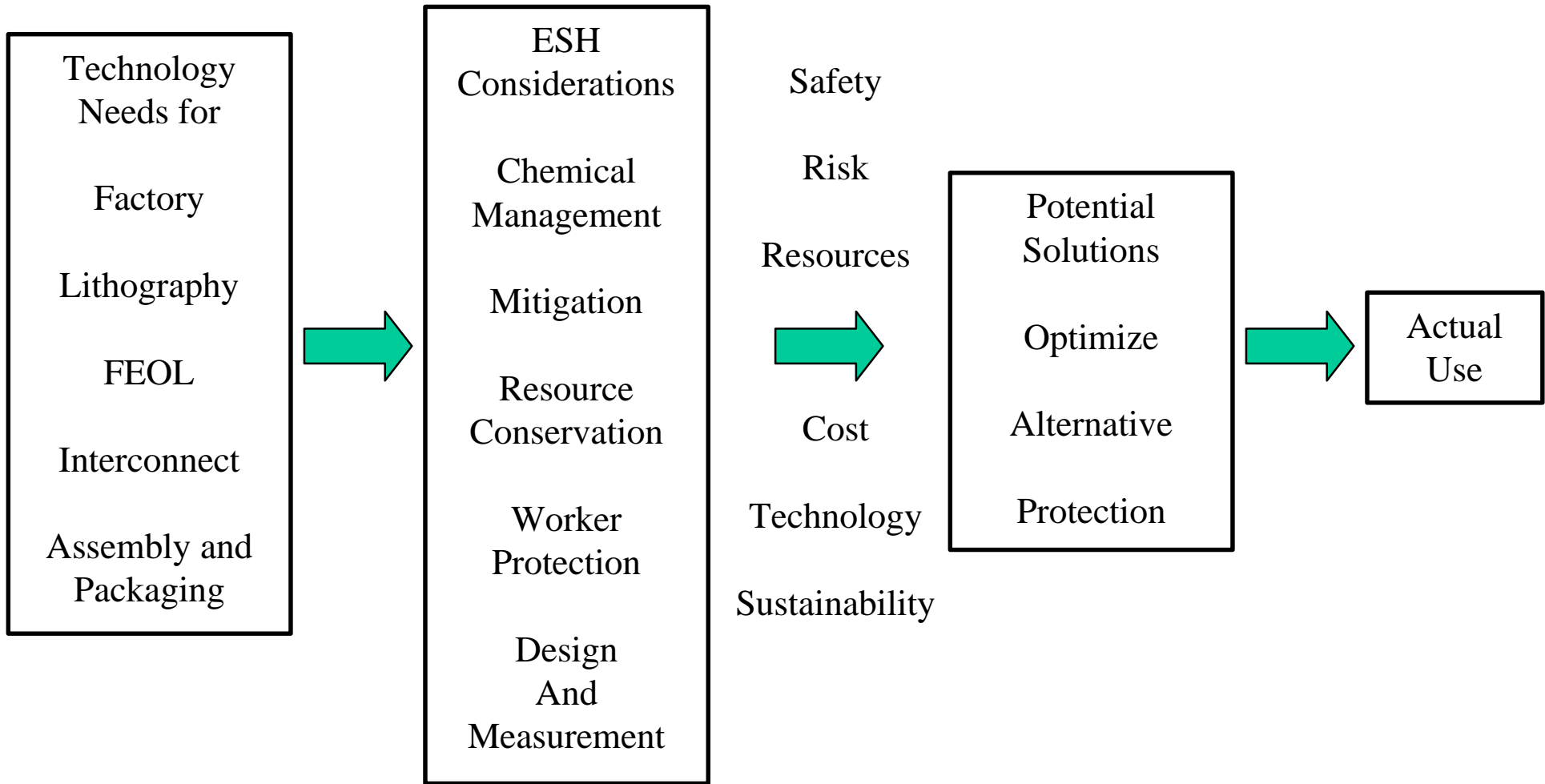
# Background

The semiconductor industry views responsible performance in environment, safety and health (ESH) as critical to success.

The International Roadmap for Semiconductors (ITRS) extensively addresses ESH needs, therefore giving direction to research centers, suppliers and semiconductor manufacturers, helping to integrate ESH into manufacturing and business practices.

## Five Difficult Challenges

- Chemicals, Materials, and Equipment Management
- Resource Conservation
- Workplace Protection
- Climate Change Mitigation
- Design for ESH



Source: Future ESH Trends in the Semiconductor Industry (7/1/2000) Future Fab Intl. Volume 8

# Some examples of good ESH practices

## PFC Emissions

In 1999, the World Semiconductor Council announced an international goal to reduce PFC emissions by 10% by 2010, relative to the 1995 baseline.

As a result, semiconductor manufacturers have been actively pursuing strategies to reduce PFC emissions from etch and CVD chamber cleaning processes, which account for up to 90% of emissions from a modern 200 mm fab ( $C_2F_6$ )

The industry developed remote plasma clean technology using  $NF_3/Ar$ , which has demonstrated >99%  $NF_3$  destruction efficiency, virtually eliminating PFC emissions from chamber cleaning. (Voluntary Agreement)

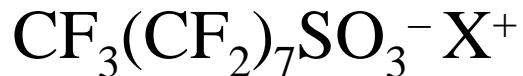
## Water Management

Water recycling practices in U.S. fabs have lagged behind those in other parts of the world because of the regional abundance and low cost of water.

Recycling provides cost savings, due to the lower level of maintenance on the ultrapure water (UPW) system (lower load on the reverse osmosis membranes and the ion exchange resins), less chemicals required for regeneration, less wastewater, lower discharge costs.

# ESH Issues in Advanced Lithography

## PFOS – A Case Study



Perfluorooctane sulfonate (PFOS)-based chemicals are useful in key areas of photoresist development and manufacturing

- PFOS is highly persistent in the environment, with a strong tendency to bioaccumulate.
- Although it is not fully known what toxicity implications PFOS holds, the EPA is concerned that it could have considerable adverse effects in people and wildlife if it continues to be produced, released and built up in the environment.
- It is estimated that in 2001 US. chipmakers released ~12 kg/yr of PFOS into the environment through top ARCs, ~3 kg/yr through resist surfactants, and ~15 kg/yr through resist PAGs.  
(Source: AZ Clariant)
- The Environmental Protection Agency (EPA) conceded to an exemption for photolithography, based on the extremely low impact, volume, usage, exposure and negligible environmental release produced by the semiconductor industry.

# The Advantage of using PFOS

## Top Antireflective Coatings (TARCs)

Top ARCs are used to reduce the photoresist swing curve (it helps to print over topography with minimum CD variation). Index matching conditions require optical tunability, achieved through the use of fluorinated materials.

TARCs are also useful barriers that prevent airborne contaminants (amines) from poisoning the photoresist. They have also proved to be effective at reducing post-develop defects on patterned resist surfaces.

$$d_{TARC} = \frac{\lambda}{4n_{TARC}}$$

$$n_{TARC} = \sqrt{n_{RESIST}}$$

zero reflectivity at the resist/air interface  
 $d$  = thickness  
 $n$  = refractive index

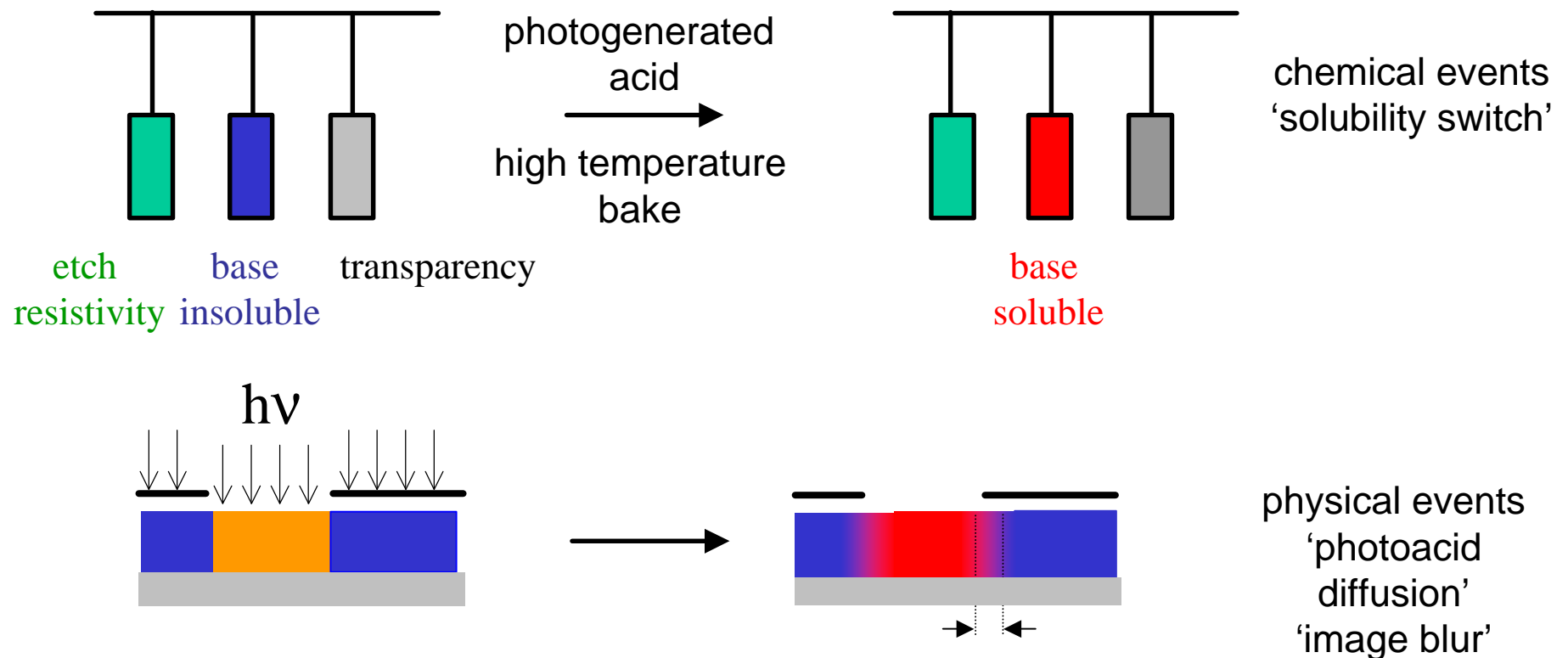
Typically, a non-fluorinated water-soluble binder resin (e.g. polyacrylic acid) is used to provide the film-forming properties, while a water-soluble fluorocomponent provides the low refractive index (e.g. PFOS salt).

Replacements of PFOS include shorter chain homologues or high-Mw fluoropolymers with film forming properties and low refracting index combined into one molecule. Solutions are available for 248nm lithography, while for 193nm new TARCs are under development.

The advent of immersion lithography poses an extra difficulty, due to the need to find water-insoluble TARCs. Best available immersion TARC to date is based on a fluorinated solvent, polymer and stripper, posing higher ESH concerns compared to 248nm TARCs.

## Photoacid Generators (PAGs)

Resists for 248 nm and shorter wavelengths rely on the principle of chemical amplification (CA), in which a primary photoevent causes the formation of an acid catalyst from a photoacid generator (PAG). The acid is able to catalyze a deprotection reaction in the resist matrix, altering the solubility in a developer solution. PAGs used for this purpose are typically perfluoroalkane sulfonates (PFAS) due to their high acid strength.

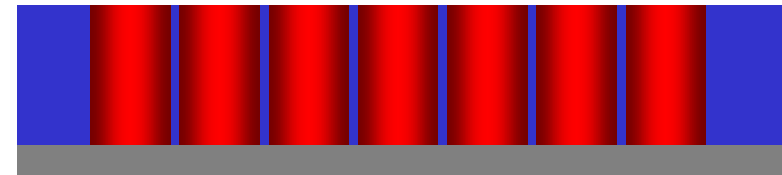


Deprotection reaction controls CD resolution

## Exposure



## High Temperature Bake



## Develop



Total Blur

**Thermally Induced Blur  
degrades Resolution**

For 193 nm lithography and next-generation lithography (NGL), the simultaneous combination of photospeed and resolution is essential for the successful implementation of a CA resist in a semiconductor manufacturing process.

For 193 nm lithography, PAGs using PFAS acids are indispensable due to their strong acidity and more effective deprotection kinetics compared to non-fluorinated analogs (high photospeed)

Bulky fluorinated PAGs can generate a strong photoacid with low diffusivity at high temperature, yielding better CD control (low image blur).

Today, basically all new resist development is moving away from PFOS, and the non-bioaccumulating perfluorobutane sulfonate (PFBS) has become the industry workhorse.



## PFBS vs. PFOS

- The shorter fluorinated chain length on PFBS results in lower bioconcentration factors (BCFs) compared to PFOS.
- PFBS-based surfactants are practically non-toxic, with low mammalian toxicity and low ecotoxicity. Unlike PFOS, PFBS does not fit within the EPA's persistent, bioaccumulative and toxic (PBT) chemical policy. It is classified as an insignificant hazard by the U.S. National Institute of Occupational Safety and Health (NIOSH), and requires no label warning by the European Union.

### Resist Developers

- PFOS salts were added to resist developers to decrease surface tension of liquid and improve resist wettability.
- Uniform resist development is essential for critical dimension (CD) control. It can impact across-the-chip-linewidth-variation (ACLV), thus affecting the performance of the integrated circuit, due to dissimilar performance of individual devices within the chip.
- Developer suppliers are removing product voluntarily and finding suitable replacements.

# What are the resist requirements for future lithographic nodes?

## Photolithography at the 65 nm node and beyond

### Wavelength of Choice

Immersion lithography will potentially extend the 193 nm lithography infrastructure to the 45 nm technology node or beyond without any apparent additional environmental implications. The industry does not yet know enough about 193 nm immersion technology to say whether there will be serious showstoppers.

#### 65 nm node

193 nm + RET + litho-friendly designs  
193 nm immersion lithography (193IL)

#### 32 nm node

Extreme Ultraviolet (EUV) lithography ?  
157IL + RET + litho-friendly designs ?  
EPL ?, imprint lithography ?  
Maskless Lithography (ML2) ?

#### 45 nm node

193IL + RET + litho-friendly designs  
Electron Projection Lithography (EPL) ?

#### Sub-32 nm nodes

EUV ?, EPL ?, ML2 ?  
imprint lithography ?  
Innovative technologies (self-assembly, polymer brushes, carbon nanotubes, ...)

Source: ITRS 2003

# Resist requirements at the 65 nm node and beyond

Transparency  
Resolution  
Sensitivity  
Aspect Ratio  
Line Edge Roughness  
Etch Selectivity  
Outgassing  
Environmental Stability (airborne sensitivity)  
Defectivity  
Post-Exposure Bake Sensitivity

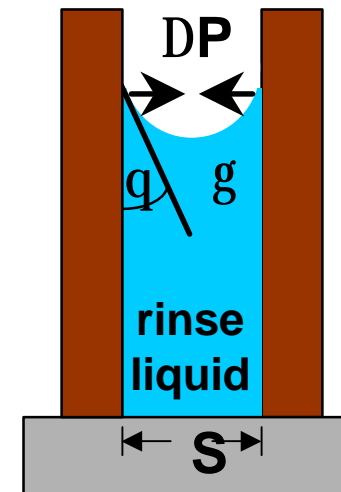
# Film thickness

Film thickness will have to decrease due to higher radiation absorption at shorter wavelengths from the resist matrix, and to prevent pattern collapse of densely packed structures.

Surfactant-containing rinses will be used to decrease the surface tension of the rinse liquid, in order to mitigate the mechanical failure during the drying step.

Aspect ratios (AR) achievable by the use of surfactant at the 32 nm node might not exceed the AR values used today for device manufacturing (achievable with a DI H<sub>2</sub>O rinse)

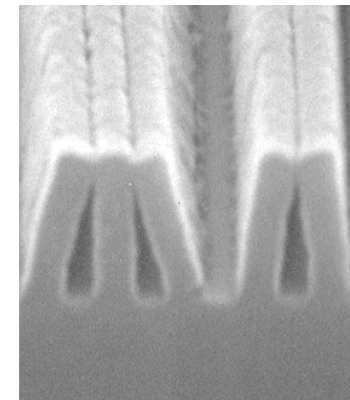
Consequently, film thickness for  $\leq 32$  nm nodes will be  $\leq 100$ nm.



$$\Delta P = f(\gamma, r, \theta)$$

$\gamma$  = surface tension  
 $S/2 = r$  = radius  
 $\theta$  = contact angle

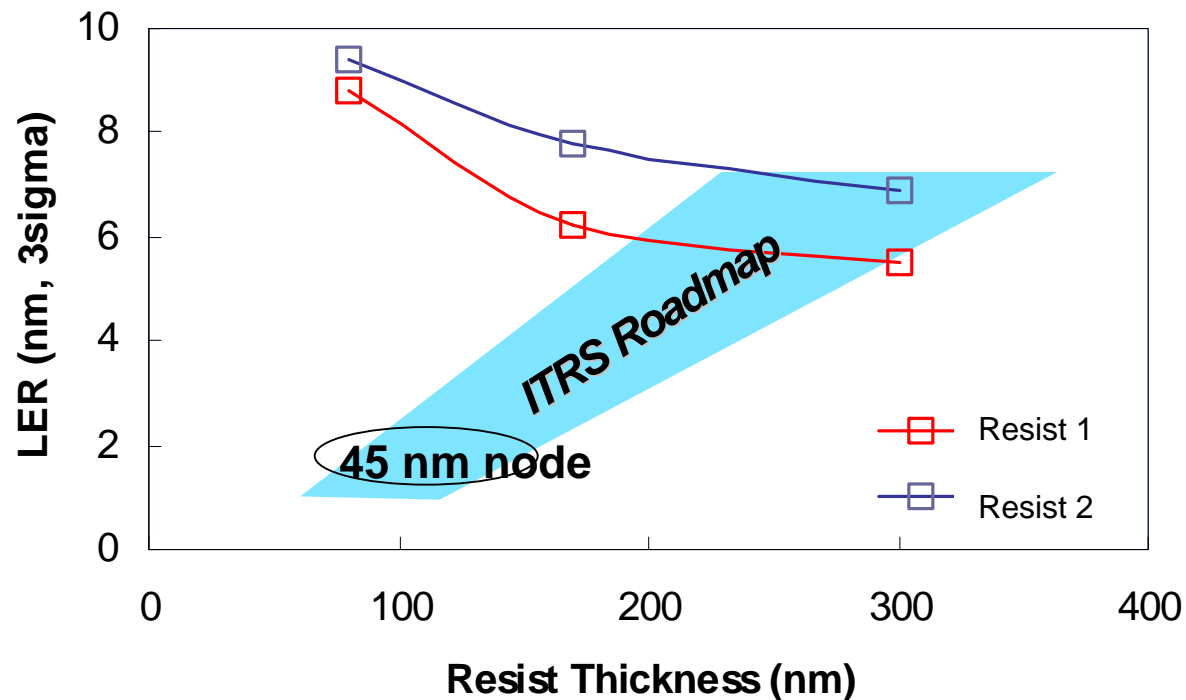
$$DP = \frac{g \cos q}{r}$$



Collapsed resist lines  
 75 nm L/S  
 Aspect Ratio = 4

# Line Edge Roughness – Critical Dimension Control

Decreasing resist film thickness can impact the LER budget severely, especially for sub-100nm thick films. Uneven distribution of resist components or poorly tuned process parameters need to be taken into account as films are thinned down.

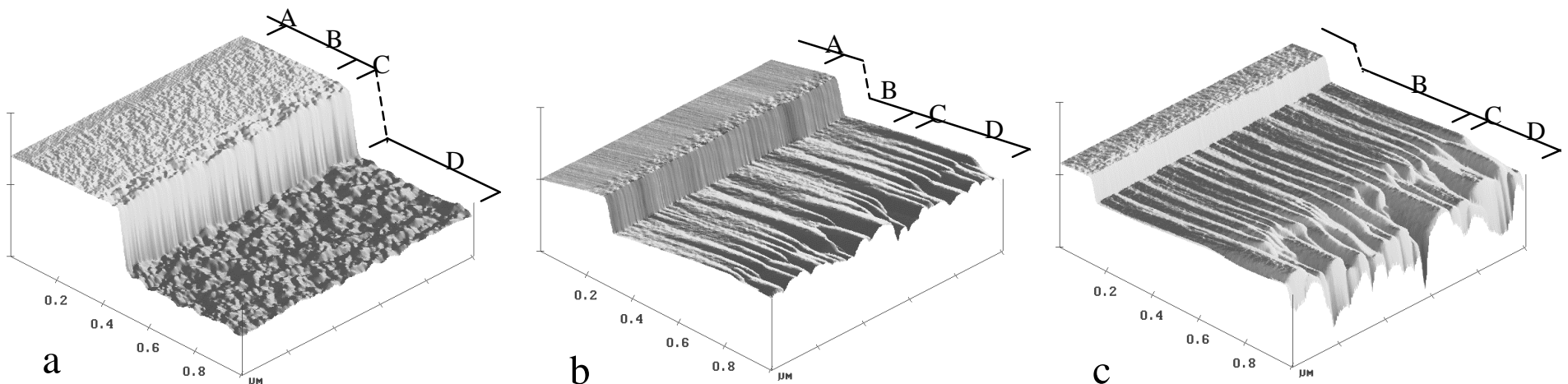


193nm resists printed @ 60 nm L/S, variable thickness

# Etch Selectivity

The use of ultrathin films (sub-100nm) poses stringent requirements on resist-to-underlayer etch selectivities, with the risk of severe roughening during the etching process.

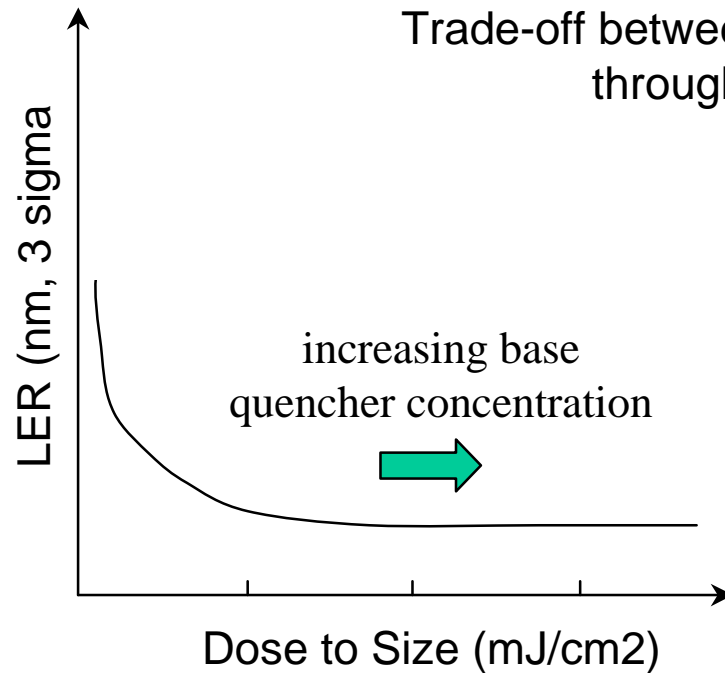
Propagation of resist roughness to underlayers (organic/inorganic BARC, SiOx, Si) can occur under aggressive (fast) etching chemistries.



AFM imaged sidewalls of patterned 248 nm resist. a) After resist development. b) 0.2 μm oxide etch (CF<sub>4</sub> -CHF<sub>3</sub> plasma); c) 0.5 μm oxide etch (CF<sub>4</sub> -CHF<sub>3</sub> plasma) . Layer nomenclature: A- Si substrate; B- SiO<sub>x</sub>; C- BARC; D-photoresist. Height scale: 200 nm/div. D.Goldfarb et al. JVSTB, 22 (2004), p. 647

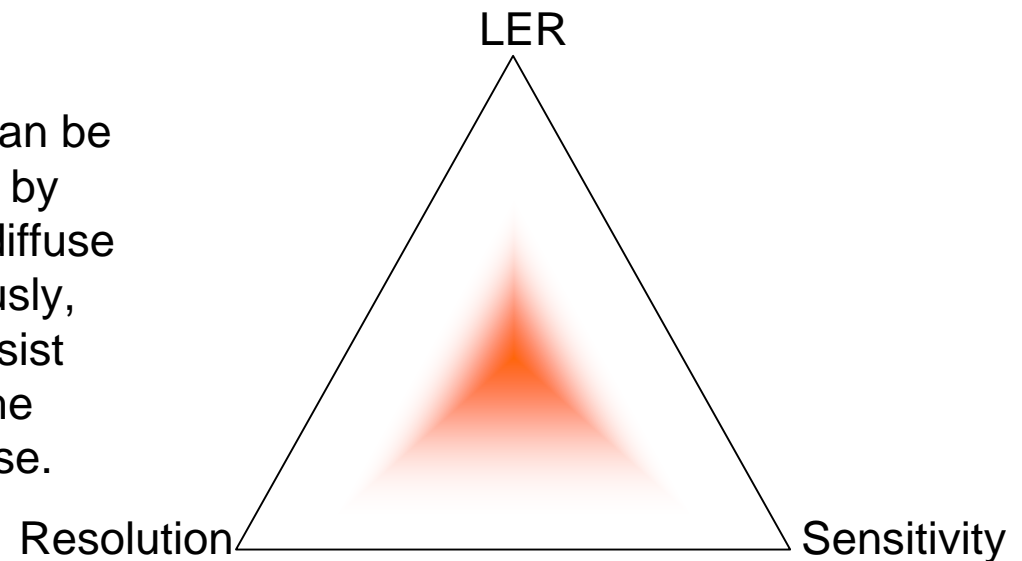
# Resist Resolution - Sensitivity

Trade-off between Spatial Resolution and Sensitivity could limit throughput for advanced lithographic nodes.



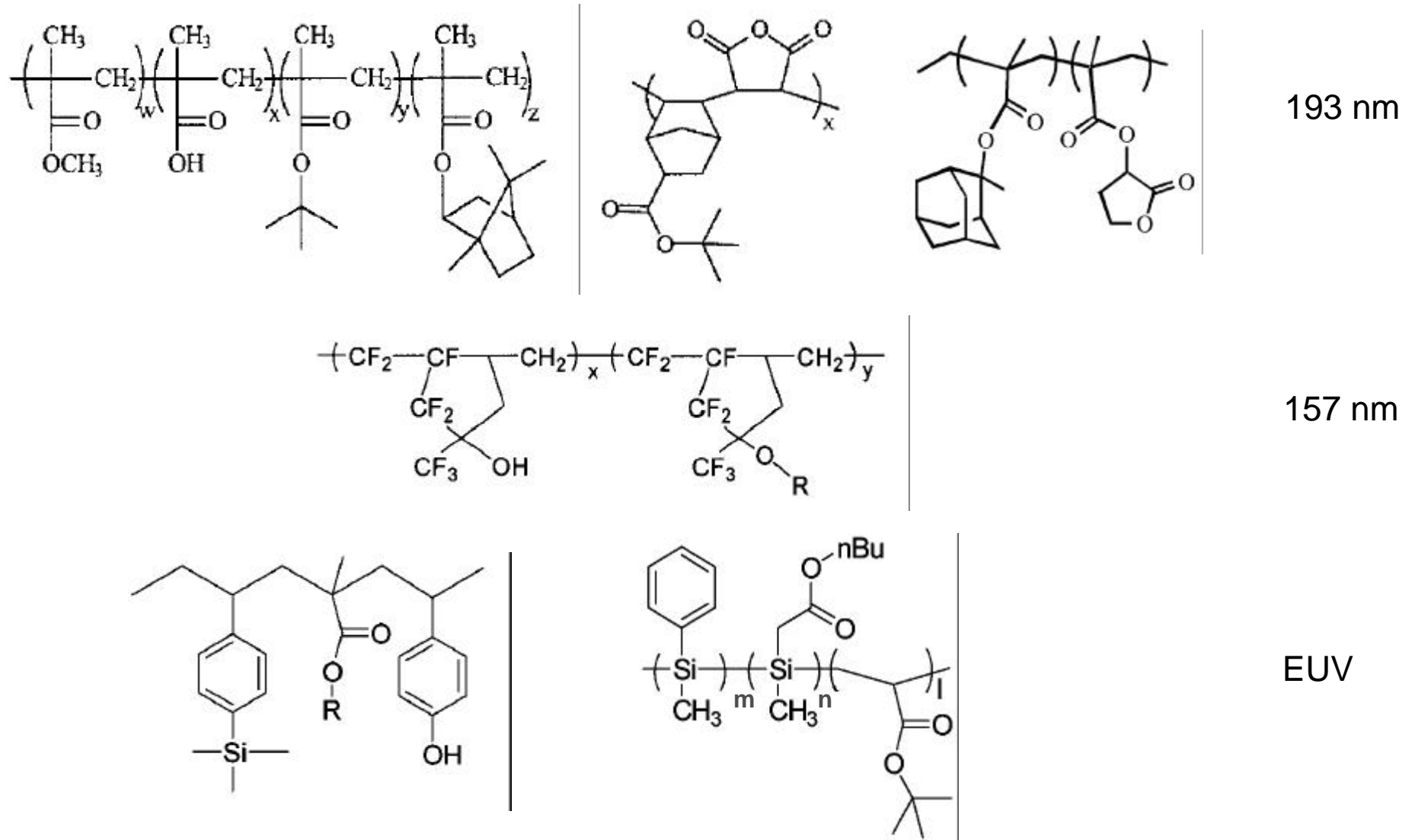
<i>Exposure Technology</i>	<i>Sensitivity</i>
248 nm	20–50 mJ/ cm <sup>2</sup>
193 nm	10–30 mJ/ cm <sup>2</sup>
157 nm	5–15 mJ/ cm <sup>2</sup>
EUV (13.5 nm)	2–15 mJ/ cm <sup>2</sup>

An increased base quencher loading can be used to control lateral image spread by neutralizing photoacid molecules that diffuse into unexposed regions. Simultaneously, enhanced LER is observed at the resist edge. However, the sensitivity of the formulation can significantly decrease.



# Resist architectures at the 65 nm node and beyond

Photoresist chemistry depends on wavelength of choice





# Conclusions

New lithographic materials are constantly brought into the manufacturing environment

Resists  
PAGs  
Rinses

BARCs  
Strippers  
Topcoats

Casting Solvents  
Developers  
Adhesion Promoters

Historically, the lithographic industry has progressed through evolutionary changes applied to well established protocols.

Stringent requirements for advanced semiconductor manufacturing might require highly innovative technologies (revolutionary changes?) in a not so distant future, which could bring an unprecedented number of new chemicals and processes into the fabs, resulting in new byproducts, new emissions, different composition of wastewater, slurry waste, etc

Early comprehension of ESH issues is essential for designers to reduce start up schedules and avoid costly retrofits and changes.

# References and Acknowledgments

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Semiconductor International

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International Technology Roadmap for Semiconductors