Infineon

Nano Interconnect Technology - Looking at the End of the Roadmap

Werner Pamler
Infineon Technologies, Corporate Research CPR NP
Munich, Germany

Never stop thinking.

Outline

- *Introduction*
  - Infineon‘s Corporate Research (CPR)
  - ITRS Roadmap
- *Nano Interconnect Activities at IFX CPR*
  - Resistivity
  - Cu Diffusion Barriers
  - Air Gaps

    - State of the Art

    - Ozone/TEOS CVD

    - Measurements

    - Simulation

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Corporate Research (CPR)

A Mix of Blue Sky, High Risk, and Roadmap Extension Projects

Nano Devices	Nano Processes	Photonics	High Frequency Circuits	Few Electron Devices	Systems Technology	Emerging Technologies
Double Gate Transistors	Nano-interconnects	Advanced Laser Diodes	CMOS Circuits	Fully Electronic Biochip	60 GHz Broadband Access Systems	Wearable Electronics
Quantum Devices	Carbon Nanotubes	> 40 Gb/s Components	SiGe Bipolar Circuits	35nm Device Circuits	Innovative Cell Phone Architectures	Polymer Electronics

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Interconnect Problems


Complexity


Reliability


Integration

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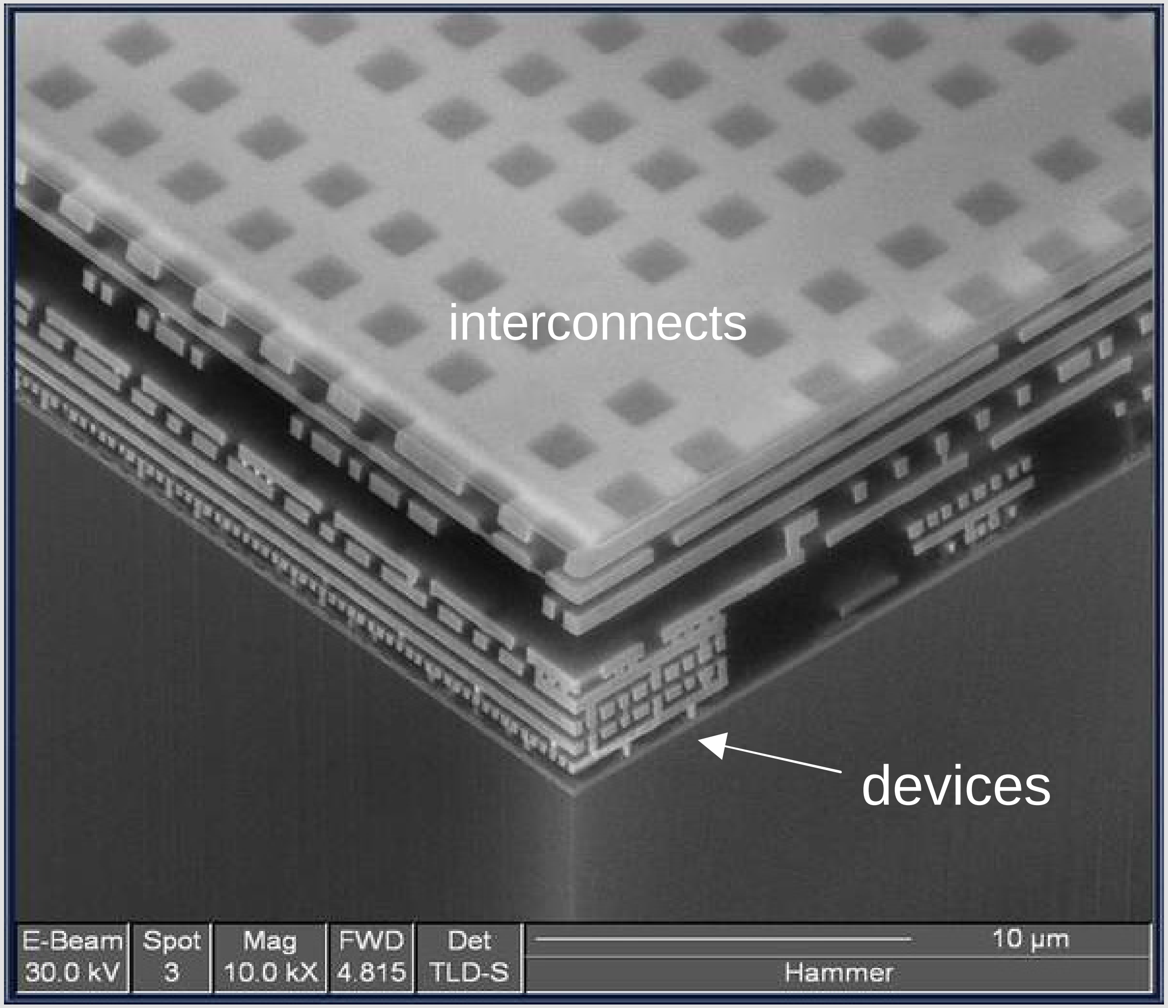
Interconnects



SEM image of AMD‘s microprocessor (“Hammer”) in 130 nm CMOS technology with 9 copper layers

E. Zschech et al., AMD Dresden, E-MRS Spring Meeting, Strasbourg 2002

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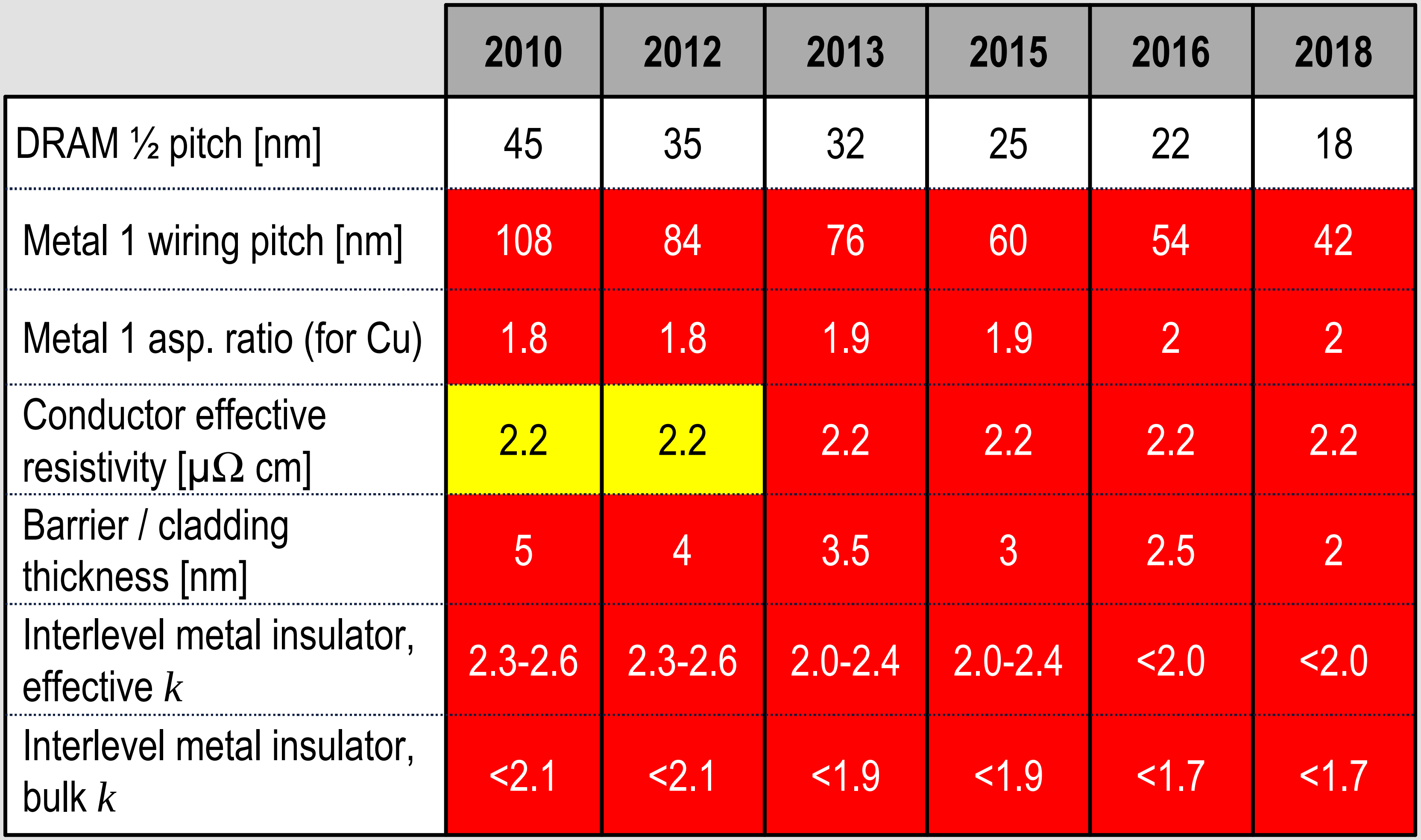
ITRS Roadmap 2003

Interconnect Technology Requirements (MPU, long-term)



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DRAM ½ pitch [nm]	45	35	32	25	22	18
Metal 1 wiring pitch [nm]	108	84	76	60	54	42
Metal 1 asp. ratio (for Cu)	1.8	1.8	1.9	1.9	2	2
Conductor effective resistivity [µΩ cm]	2.2	2.2	2.2	2.2	2.2	2.2
Barrier / cladding thickness [nm]	5	4	3.5	3	2.5	2
Interlevel metal insulator, effective *k*	2.3-2.6	2.3-2.6	2.0-2.4	2.0-2.4	<2.0	<2.0
Interlevel metal insulator, bulk *k*	<2.1	<2.1	<1.9	<1.9	<1.7	<1.7

🟨 manufacturable solutions known 🟥 no known solutions

http://public.itrs.net

ITRS Roadmap 2003

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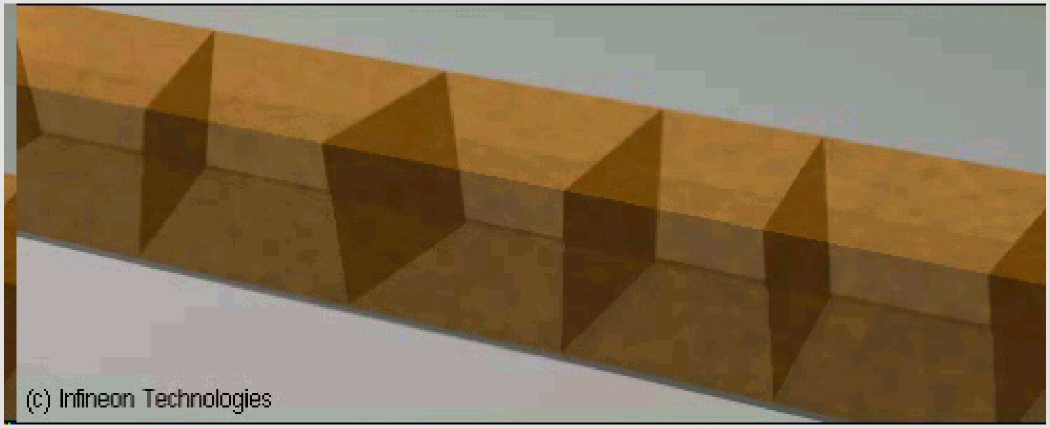
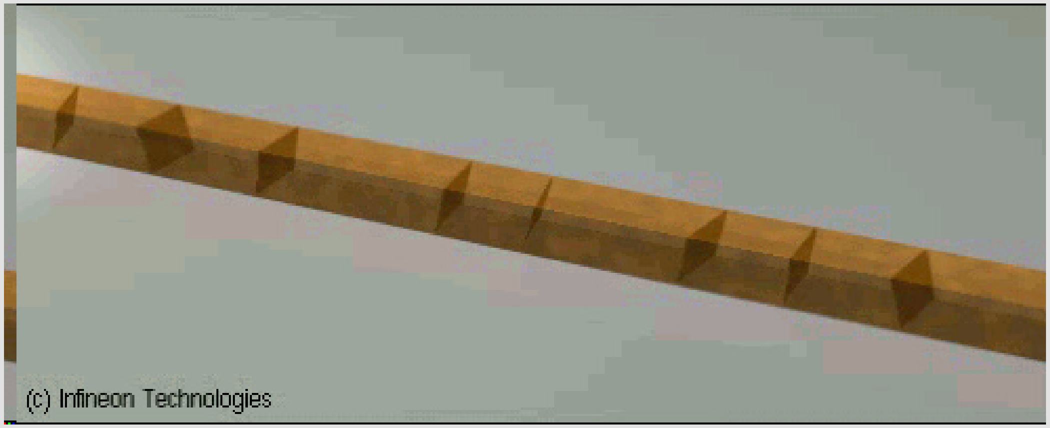
Dependence of Cu Resistivity on Line Width


(c) Infineon Technologies

- Wide conductor
- Weak scattering
- Low resistivity


(c) Infineon Technologies

- Narrow conductor
- Strong scattering
- High resistivity

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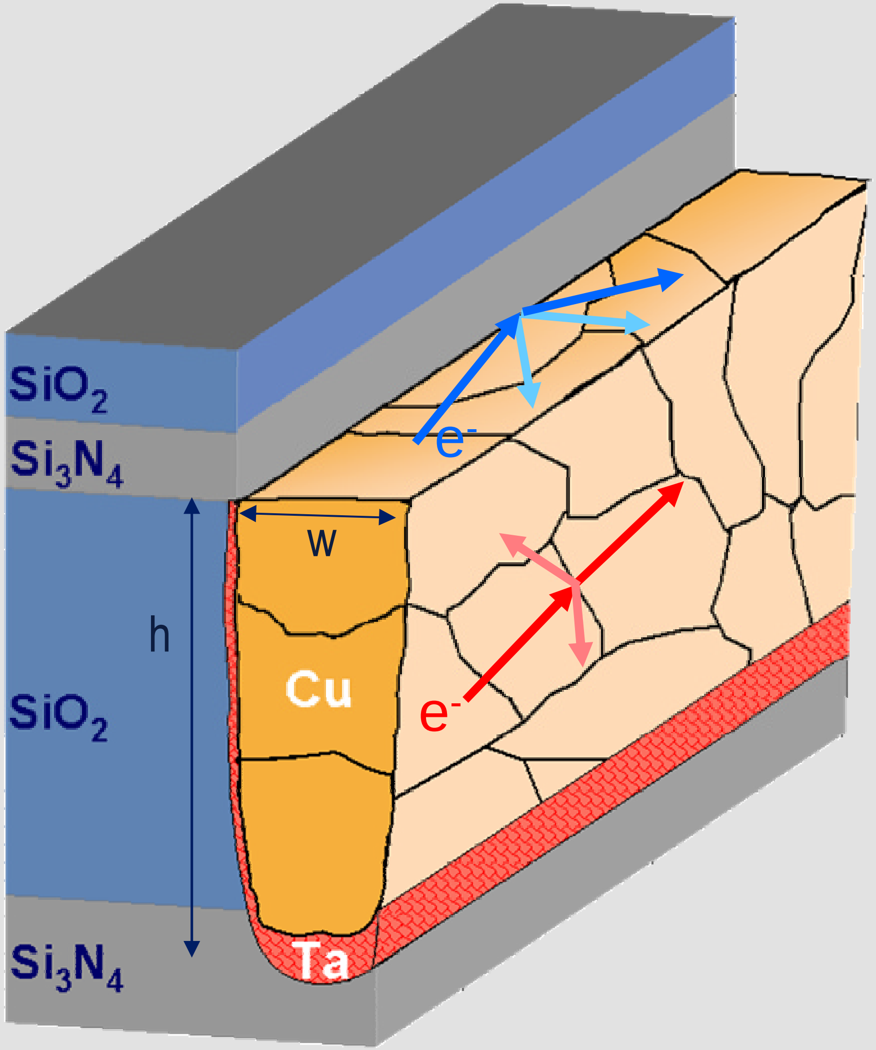
Dependence of Cu Resistivity on Line Width



W. Steinhögl et al., Phys. Rev. B66 (2002)

Surface Scattering

Fuchs-Sondheimer model

$$r_{surf} = r(h, w, p, l)$$

h, w: conductor height and width
p: specularity parameter
λ: electron mean free path

Grain Boundary Scattering

Mayadas-Shatzkes model

$$r_{g.b.} = r(d, R, l)$$

d: ave. grain boundary distance
R: Reflection coefficient at g.b.
λ: electron mean free path

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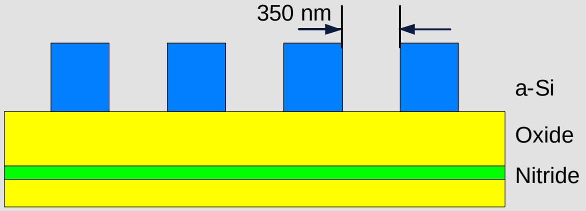
45 nm Cu Lines in i-line Lithography

a-Si patterning



G. Steinlesberger et al., Proc. IITC 2002

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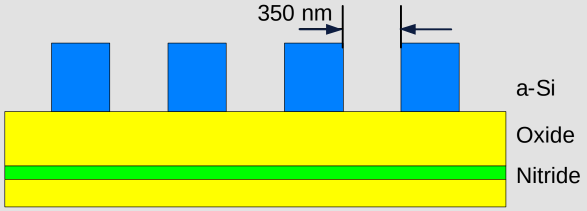
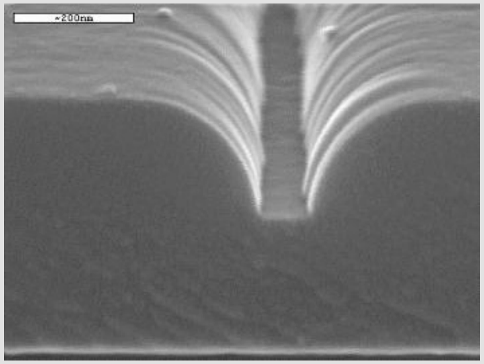
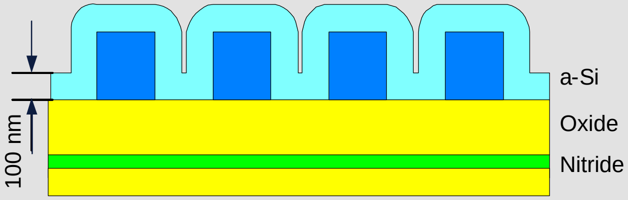




comformal a-Si
deposition



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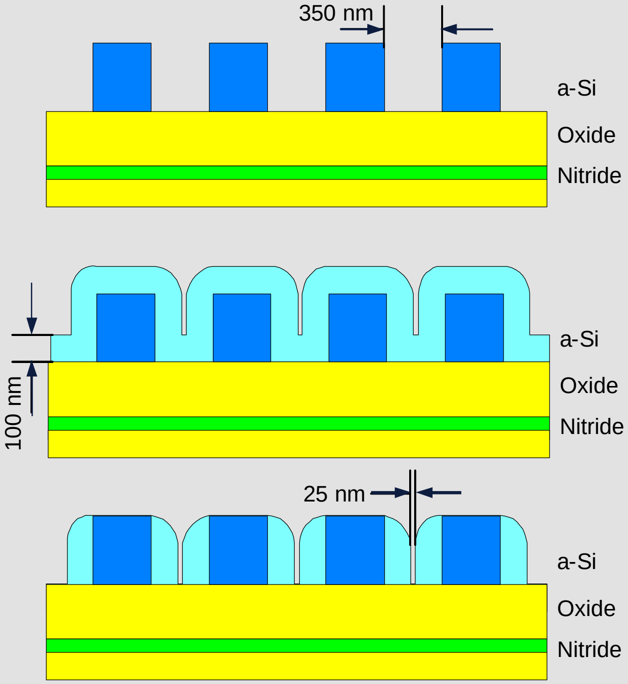
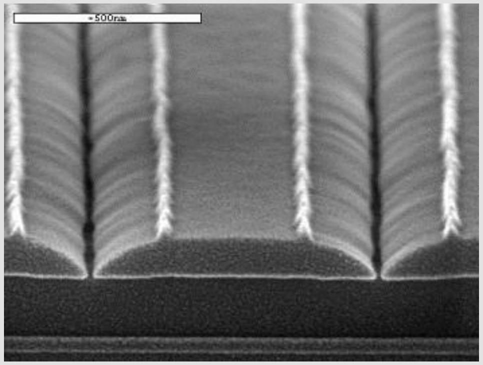


a-Si patterning

comformal a-Si deposition

spacer etch



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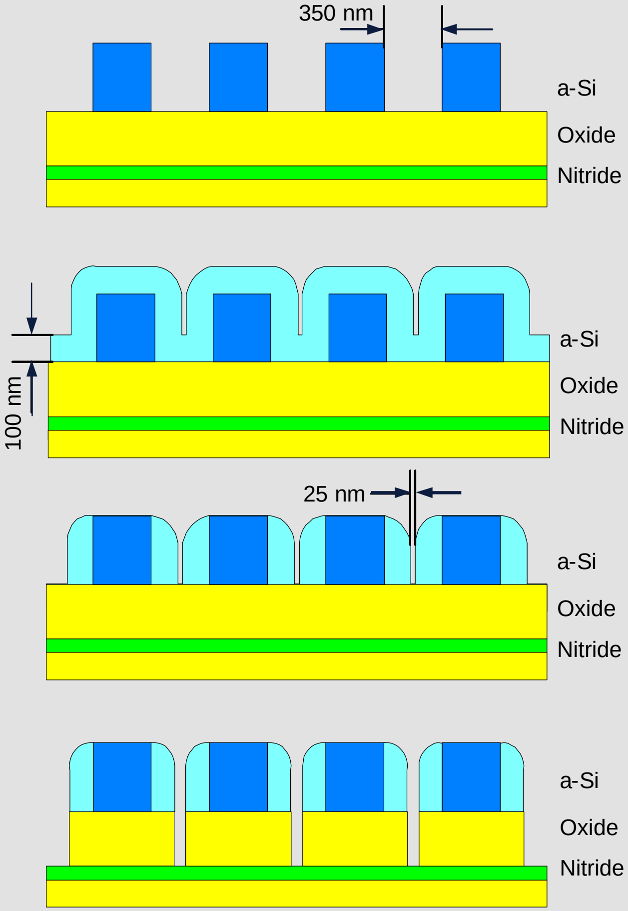
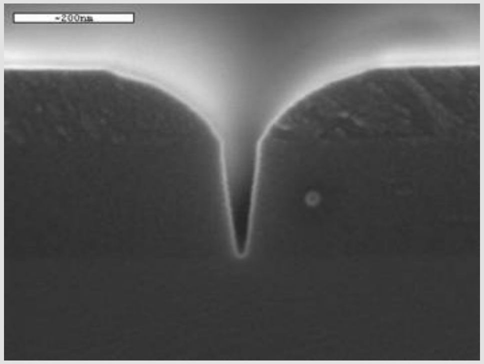


a-Si patterning

comformal a-Si deposition

spacer etch

oxide etch with a-Si hardmask



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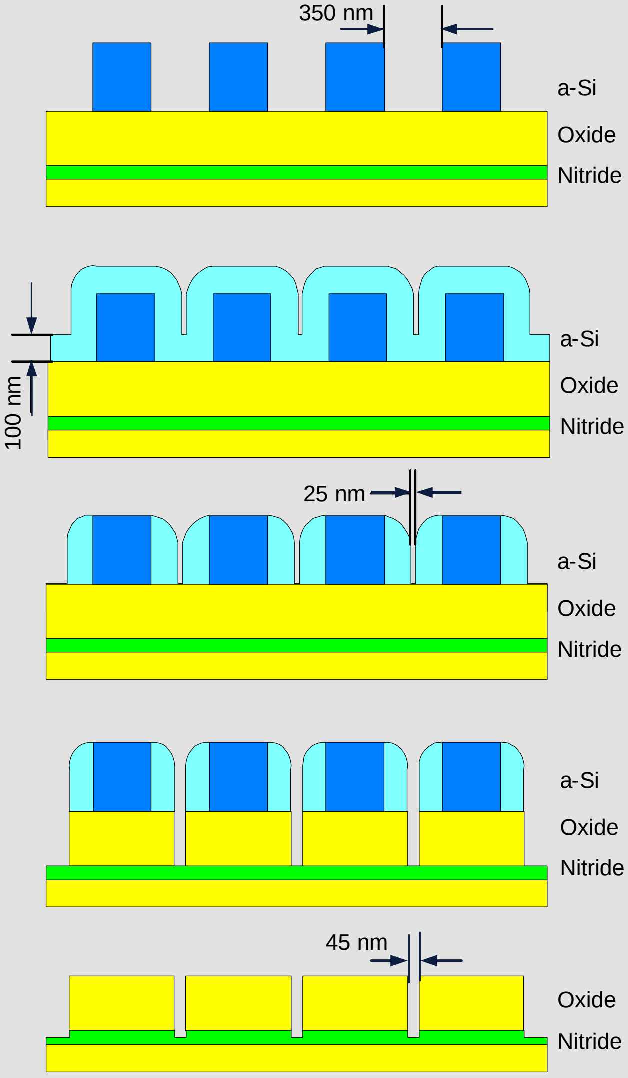


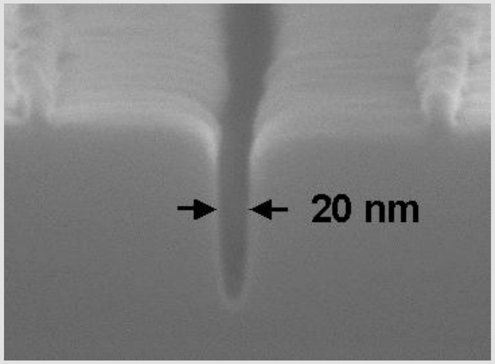
a-Si patterning

comformal a-Si deposition

spacer etch

oxide etch with a-Si hardmask

hardmask removal



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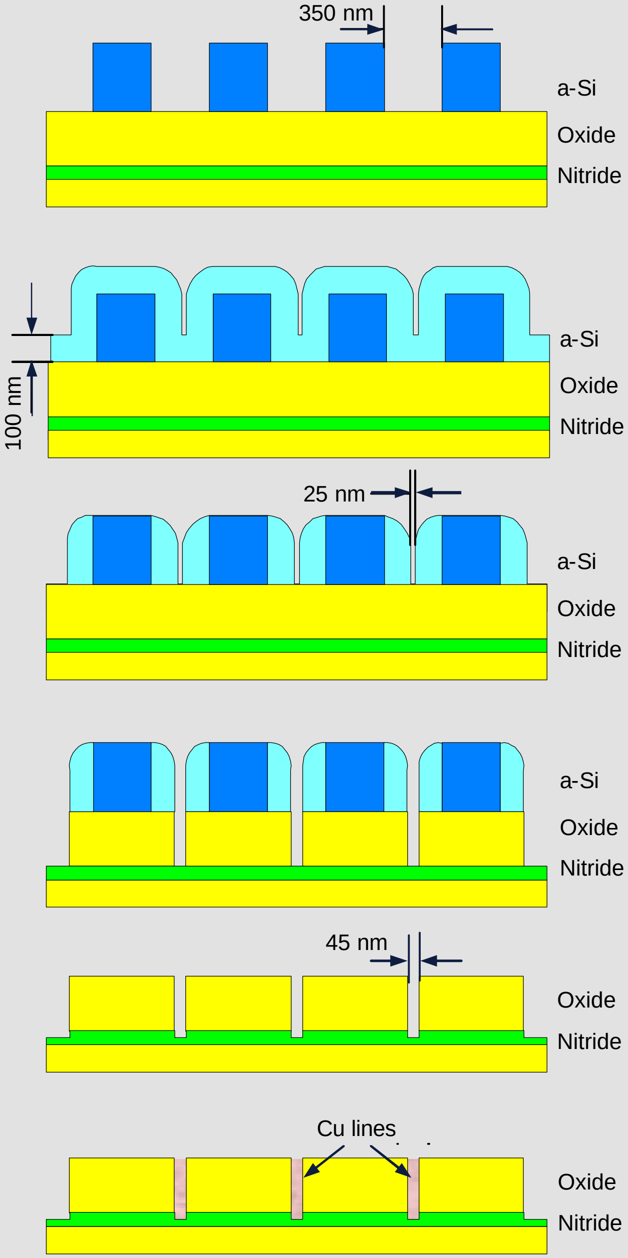

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Cu damascene

G. Steinlesberger et al., Proc. IITC 2002

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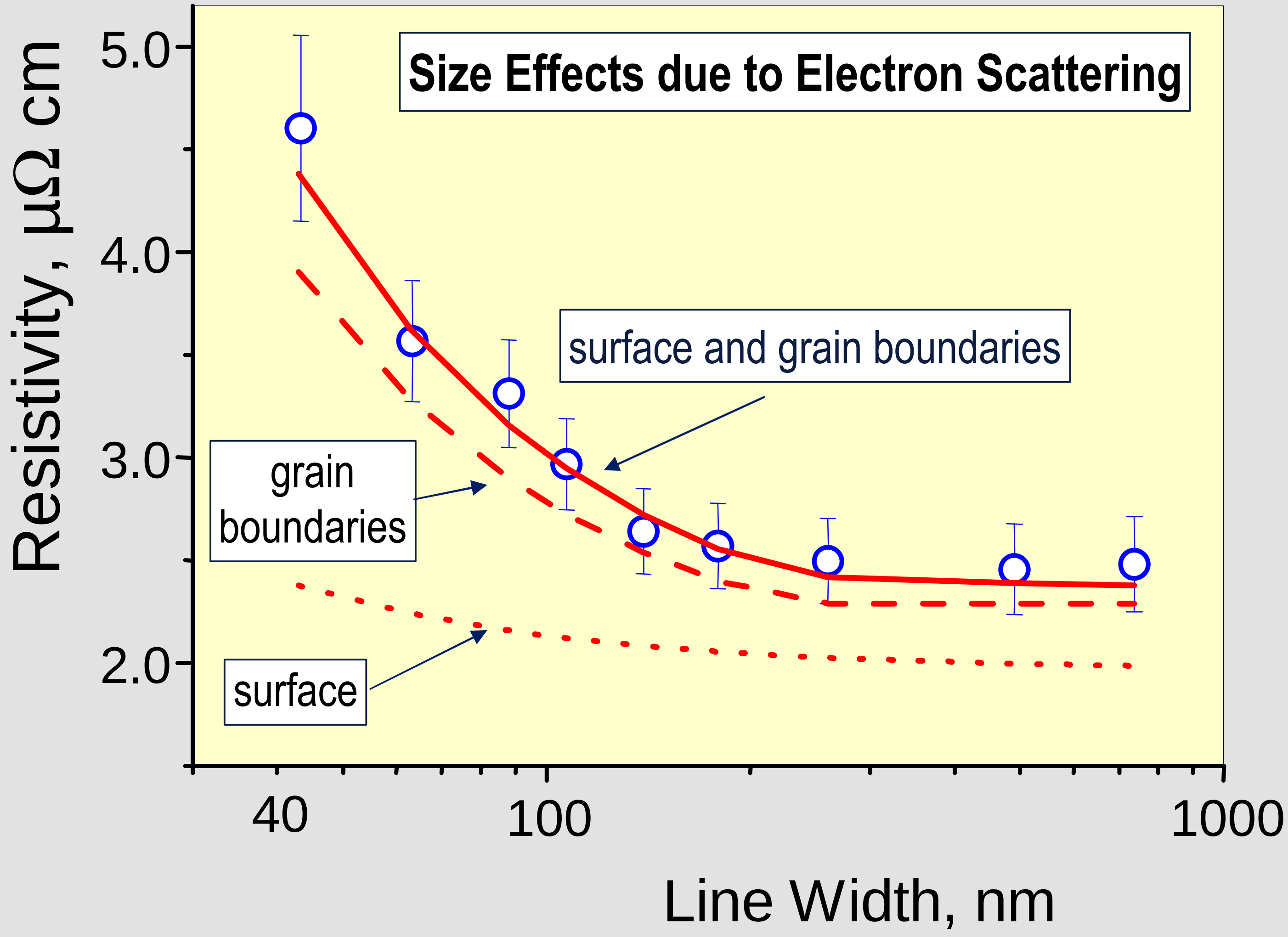
Cu Resistivity

Dependence on Line Width



W. Steinhögl et al., Phys. Rev. B66 (2002)

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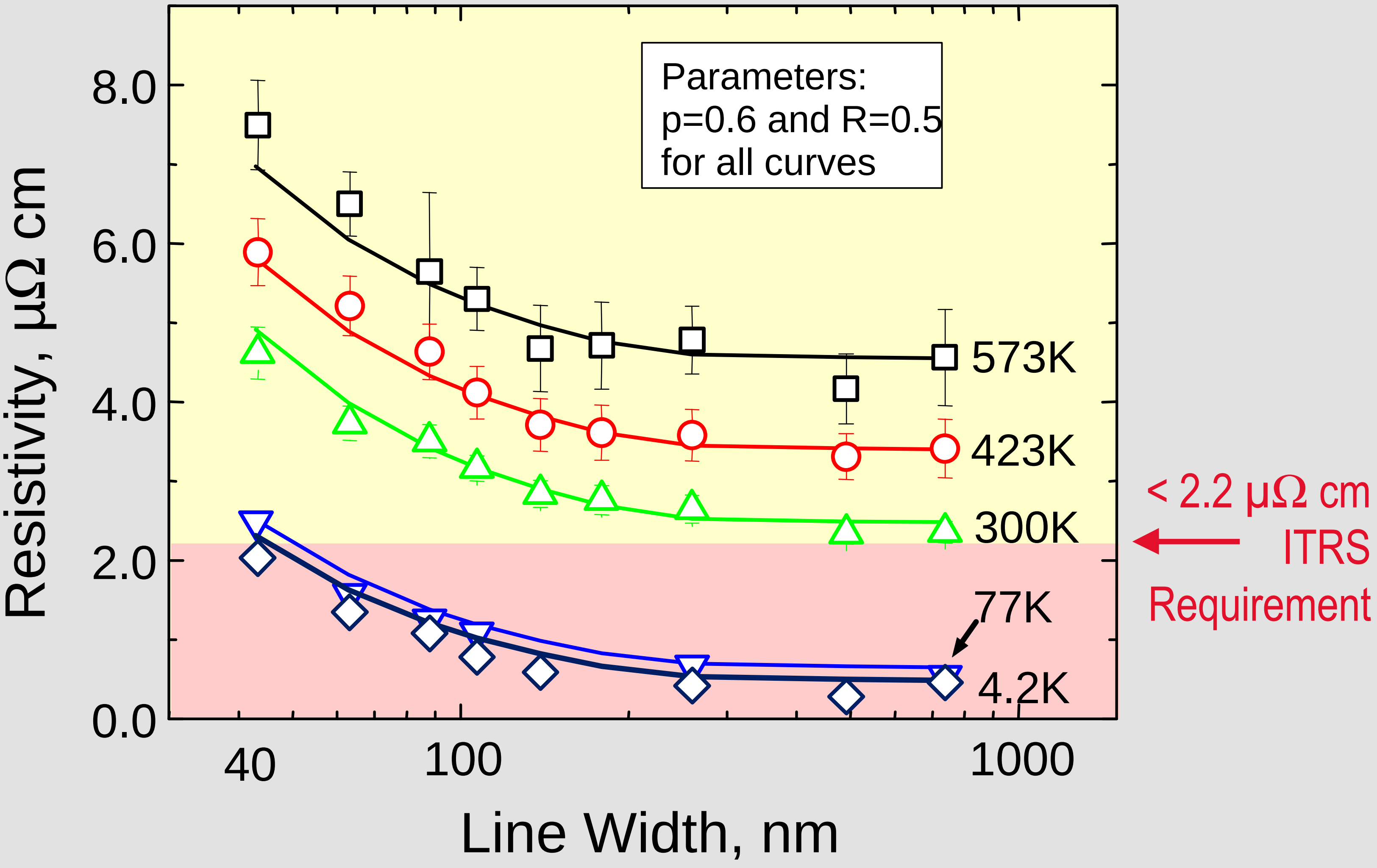
Cu Resistivity: Reduction of Temperature?

ITRS Requirement ρ_{Cu} = 2.2 µΩ cm will not be met below 40 nm



G. Schindler et al, proc. AMC 2002

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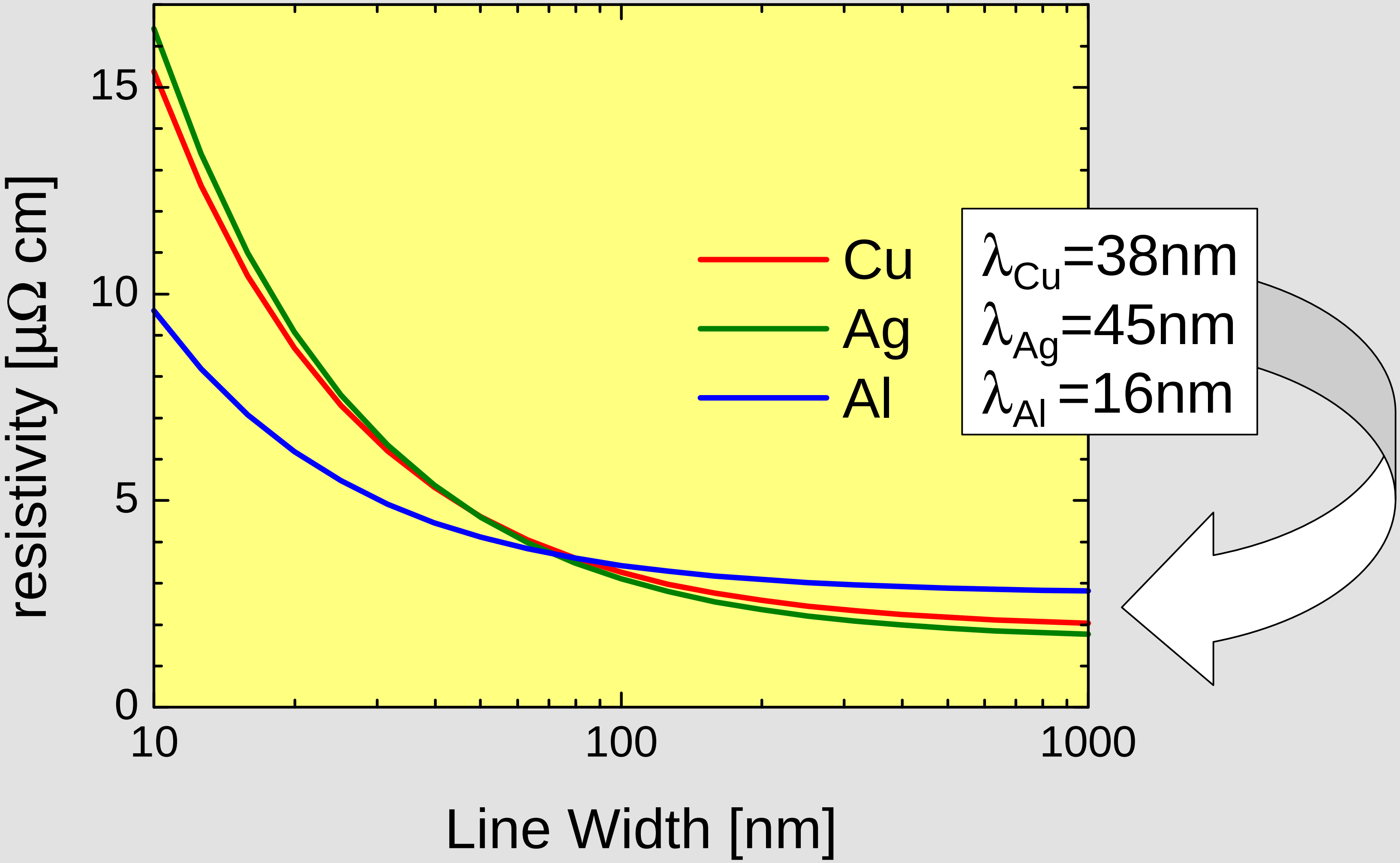
Resistivity

Will Al get a second chance?



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Resistivity

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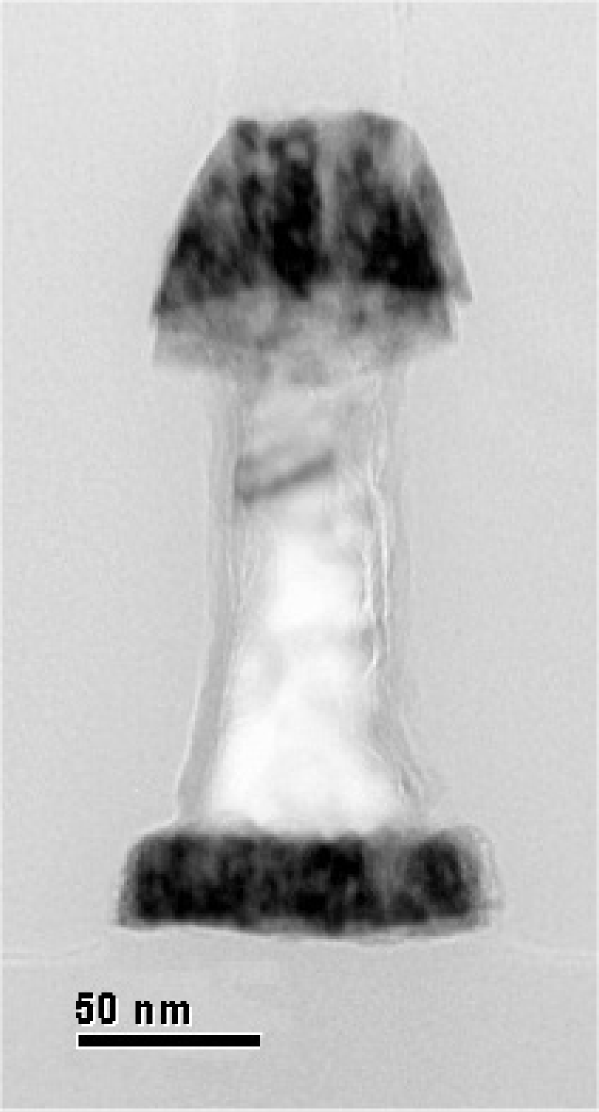

The World‘s Narrowest Al Conductor Lines

G. Steinlesberger et al., IITC 2004

Electrical measurements to be made…

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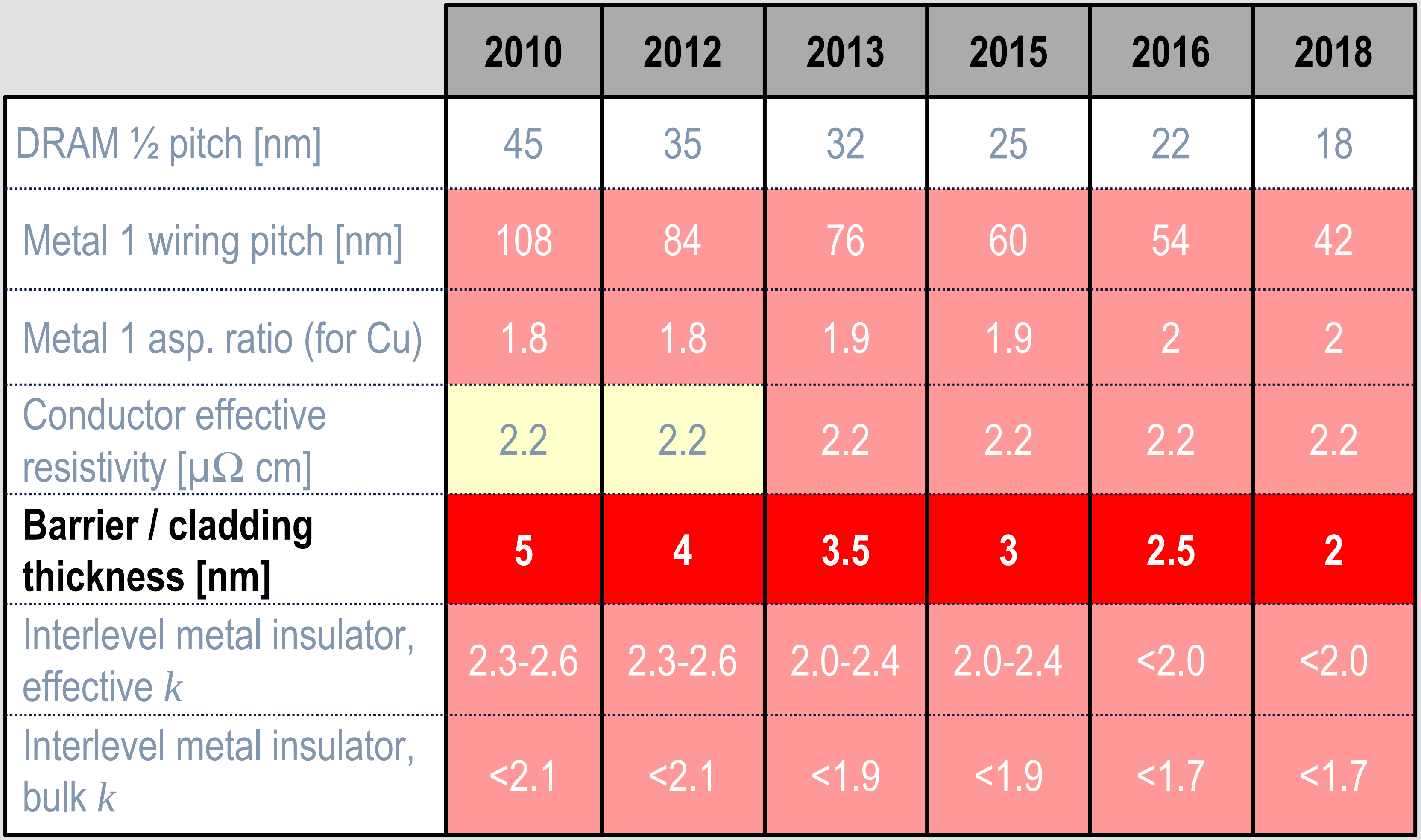

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🟨 manufacturable solutions known 🟥 no known solutions

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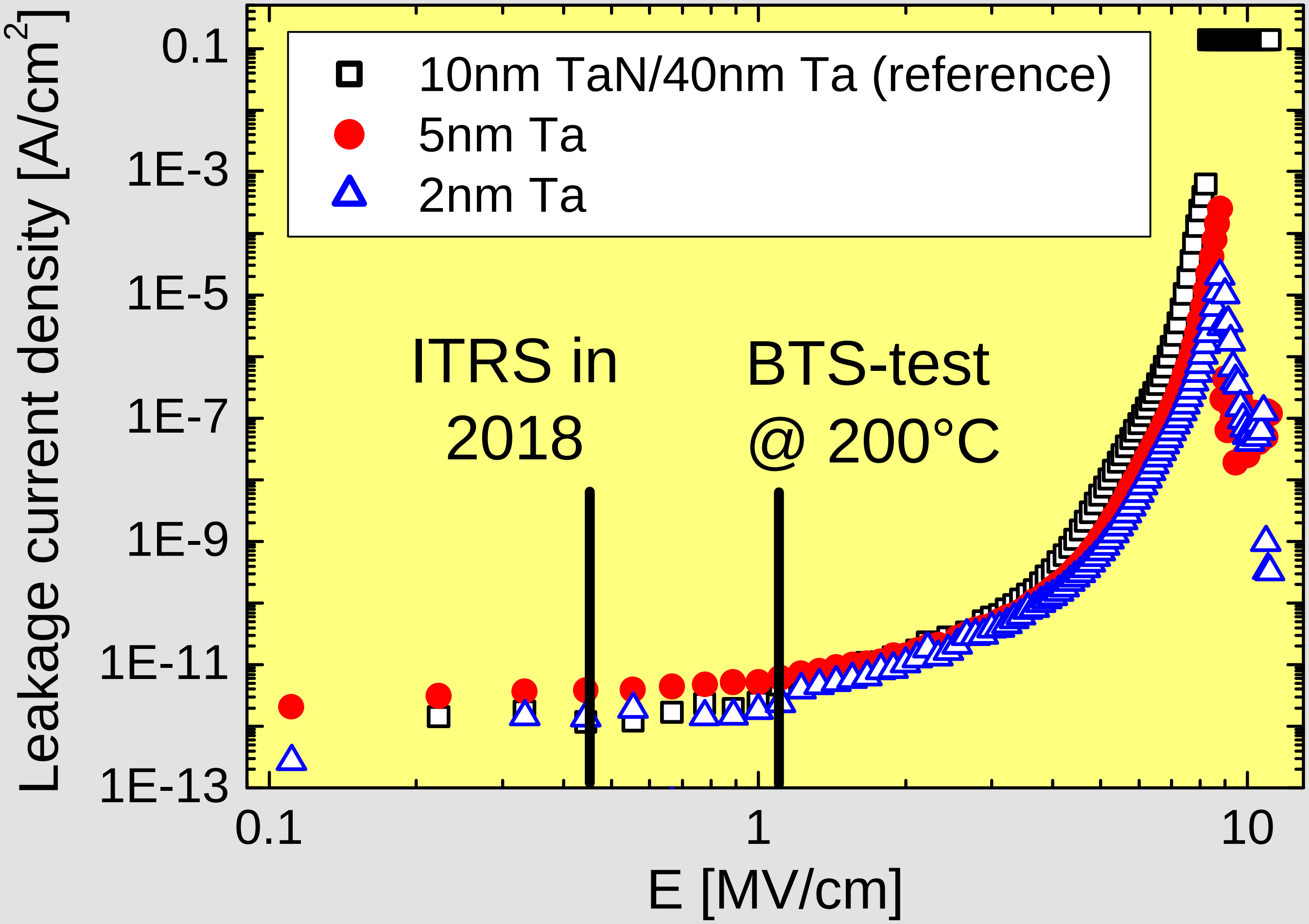
Barriers



No degradation of dielectric

M. Traving et al., Proc AMC 2003

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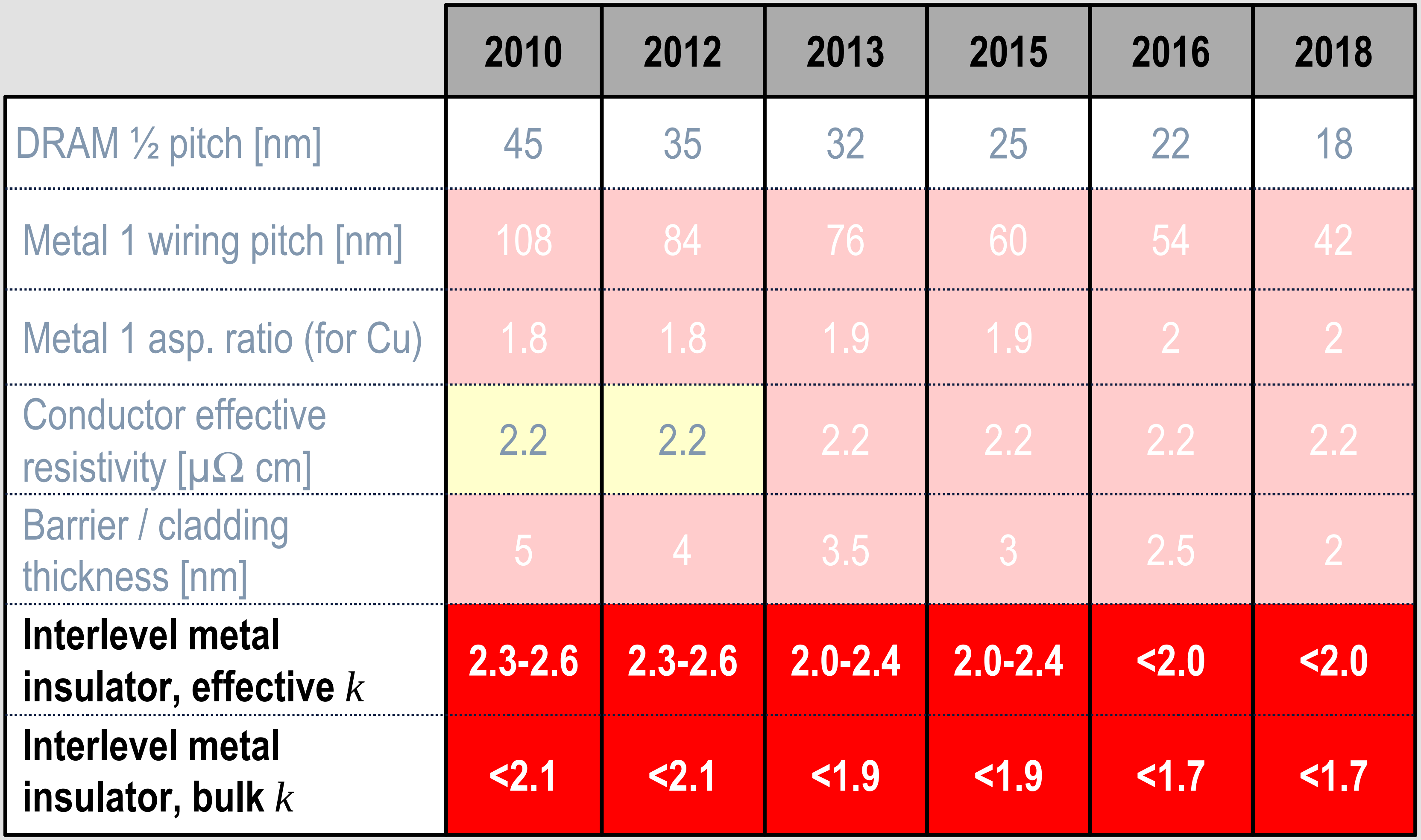

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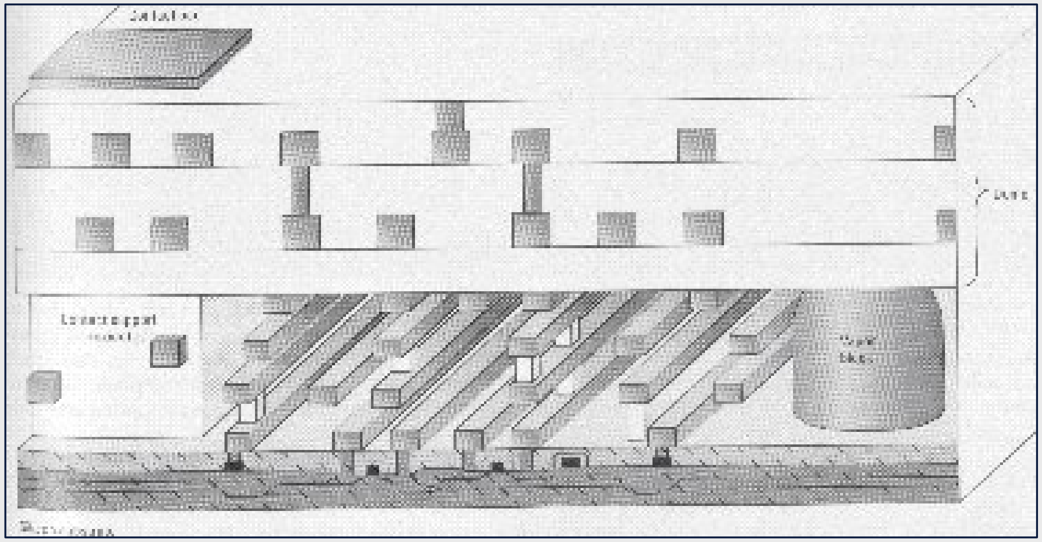
Concepts for Air Gap Technology

“Gas Dome“ Concept

- Processing of metallization system in organic dielectric
- Vaporization of dielectric after finishing layers



Gas dome concept

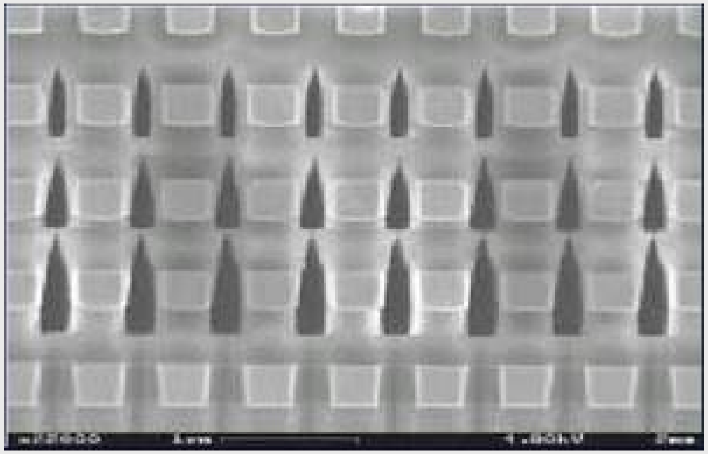
Source:
Wade, Semiconductor International, 1999, no.7, p.125

- Highest k_{eff} achievable
- But: Stability issues, poor thermal conductivity

Concepts for Air Gap Technology

Seal-off Approach

- Remove dielectric material between Cu lines after each metal layer
- Deposit non-conformal dielectric to close the air gap for subsequent processing



Arnal et al., Proc. IITC 2001

- Better stability, better thermal conductivity
- Less k_{eff} reduction

- High needle-like features at the top of the air gap top
- Danger for subsequent CMP

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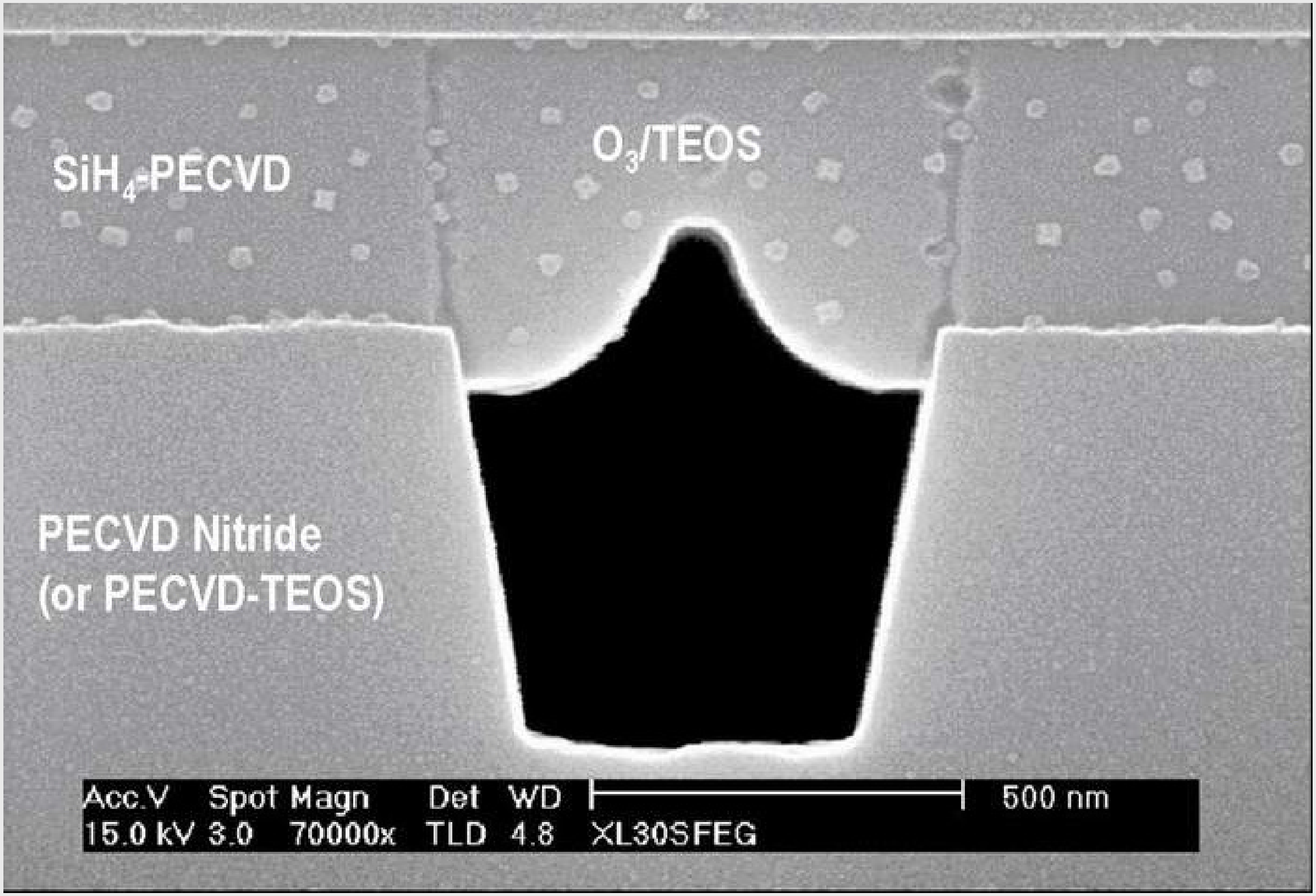
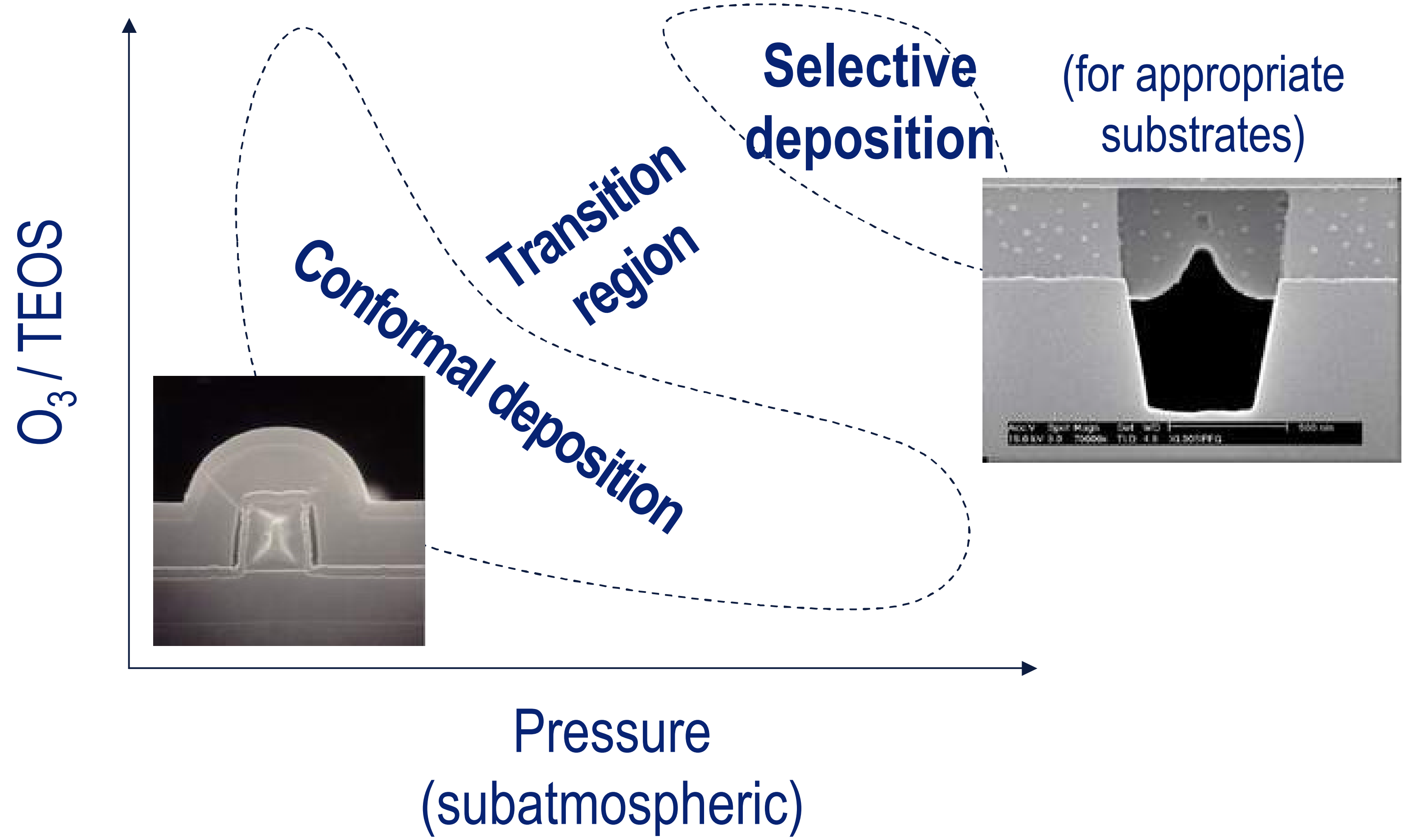
Infineon‘s Approach

Airgap Formation by Selective Ozone / TEOS Deposition



Ozone / TEOS CVD

Process regimes



O_3 / TEOS

Conformal deposition

Transition region

Selective deposition

(for appropriate substrates)

Pressure
(subatmospheric)

W.Pamler and Z.Gabric, Proc. ECS, 2001

Selective Ozone / TEOS CVD

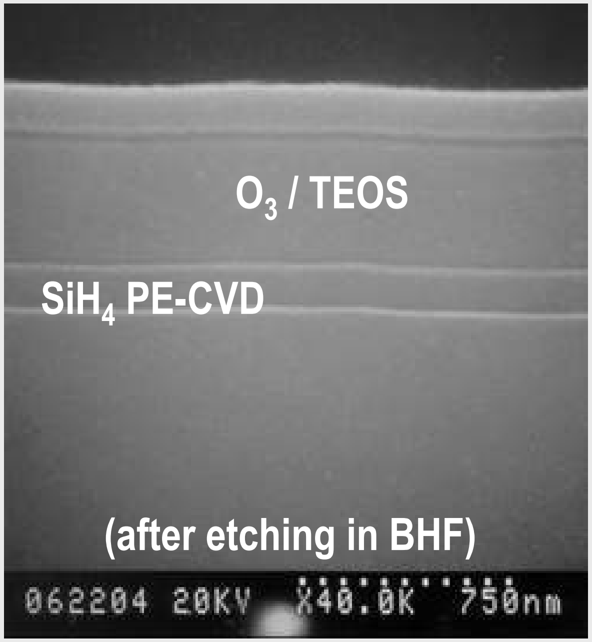
Substrate Dependence

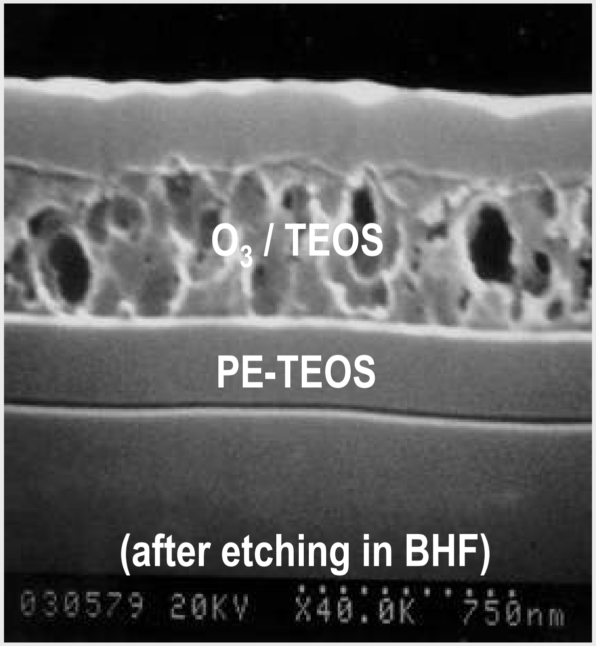
Silicon, aluminum, SiH_4-based PE-CVD oxide:

- high deposition rate
- low wet etch rate
- dense microstructure

Silicon nitride, Ti nitride, PE-TEOS, thermal oxide:

- low (no) deposition rate
- high wet etch rate
- porous microstructure ("swiss cheese")





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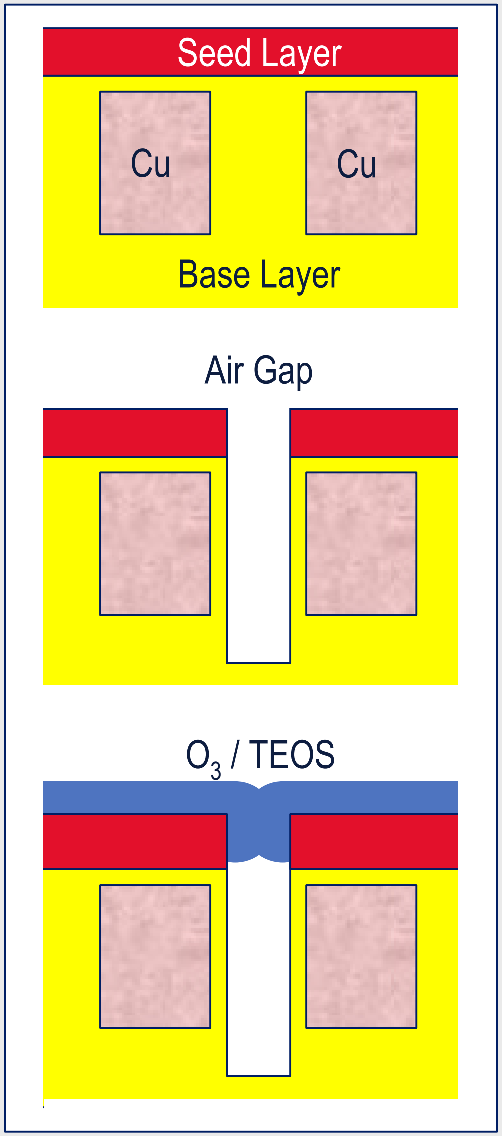
Process Flow for Airgap Creation



- **Dielectric Layer Deposition**
  - Base Layer → no O_3 / TEOS growth
  - Seed layer → good O_3 / TEOS growth
- **Cu Damascene Technology**
- **Air Gap Lithography**
- **Air Gap Etch**
- **Selective O_3 / TEOS Deposition**

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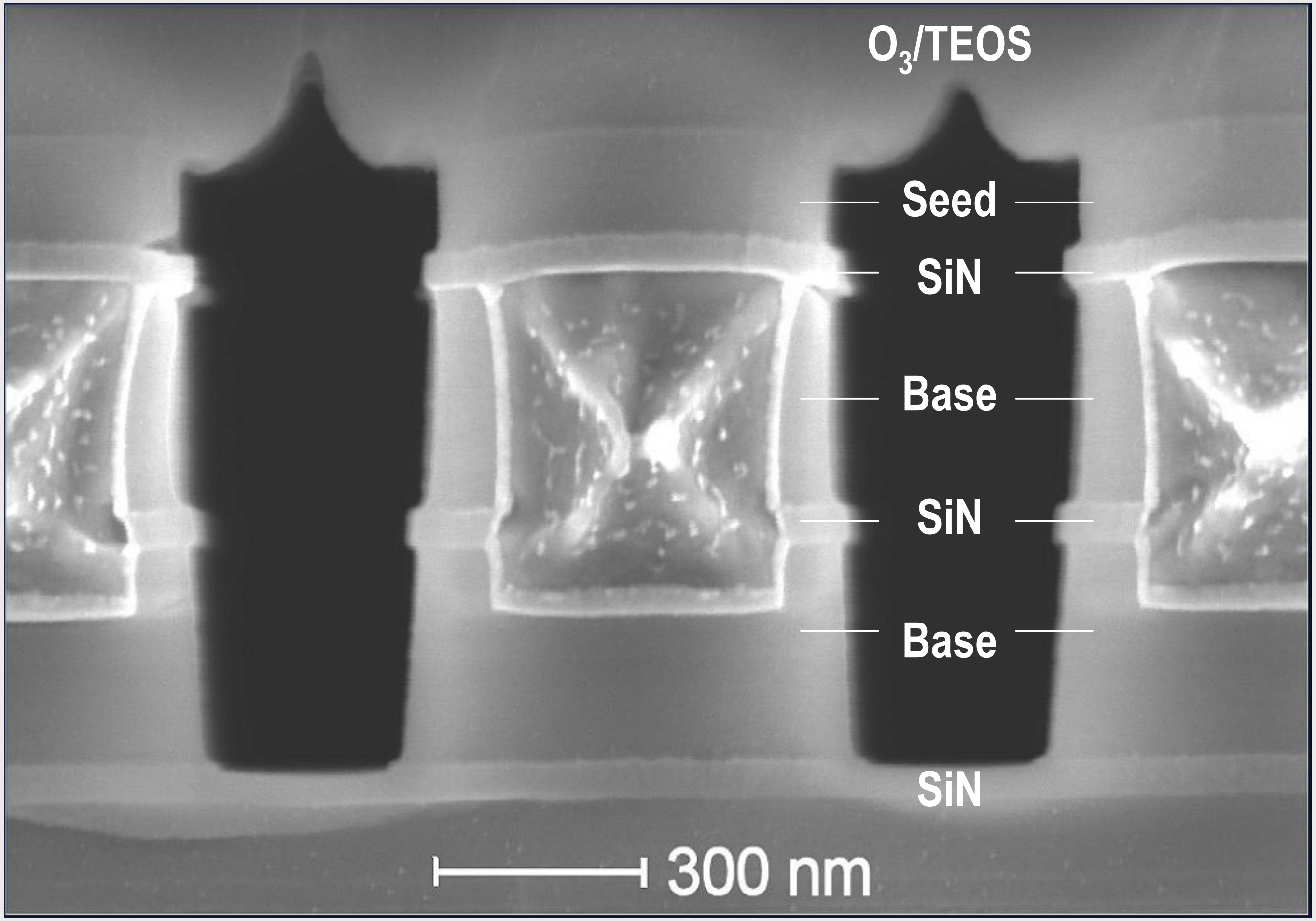
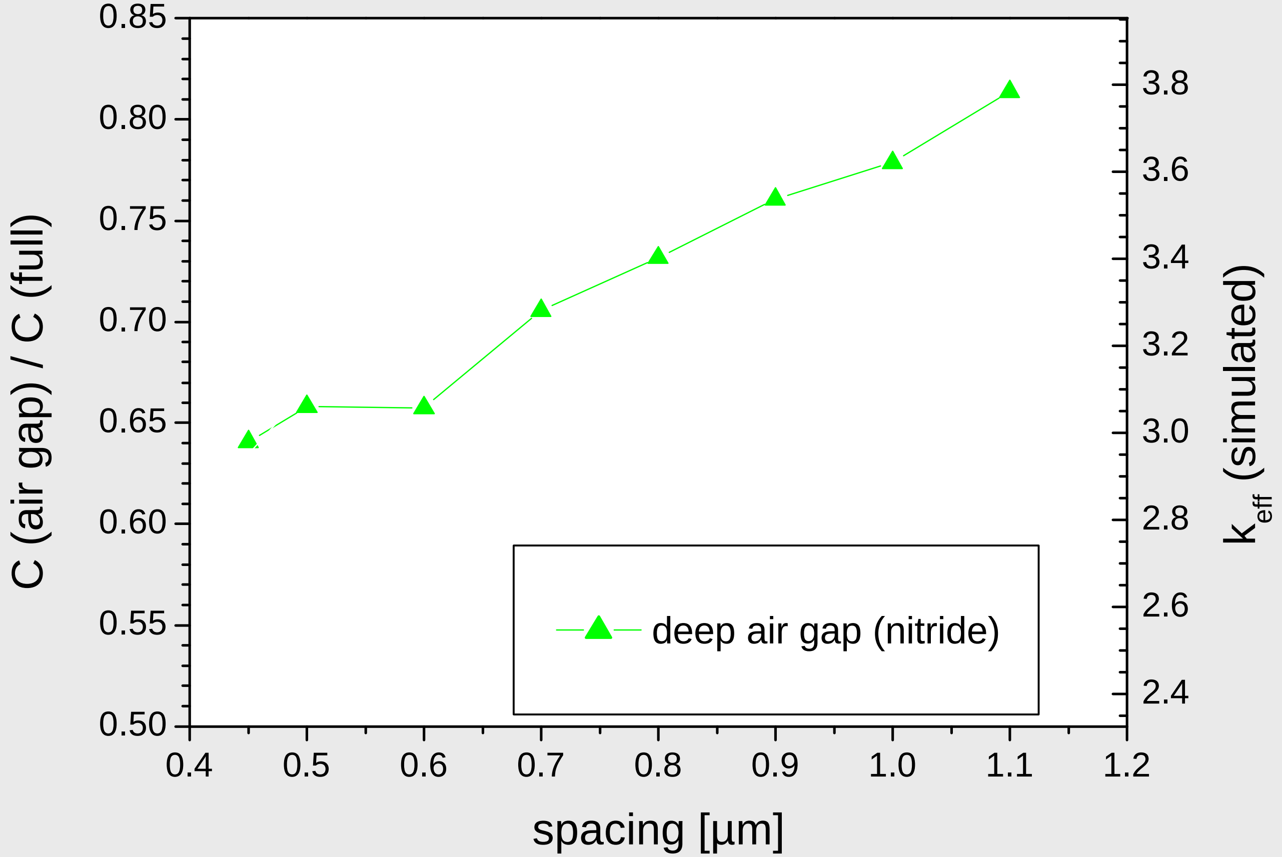
CPR's First Air Gaps

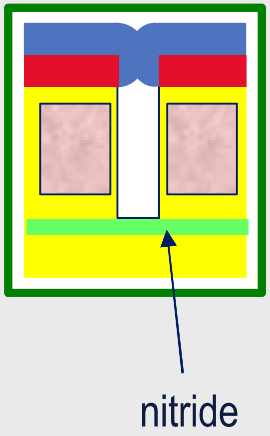


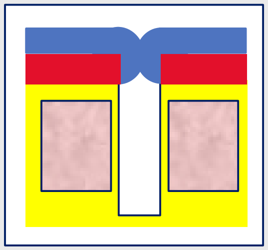
"Seed" → USG-Silane
"Base" → modified USG-TEOS

CPR‘s First Air Gaps

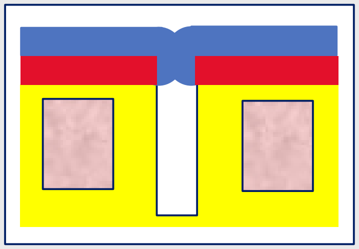
Electrical Measurements: Capacitance







air gap width: 0.38 µm
line width: 0.5 µm
spacing: 0.5 – 1.2 µm



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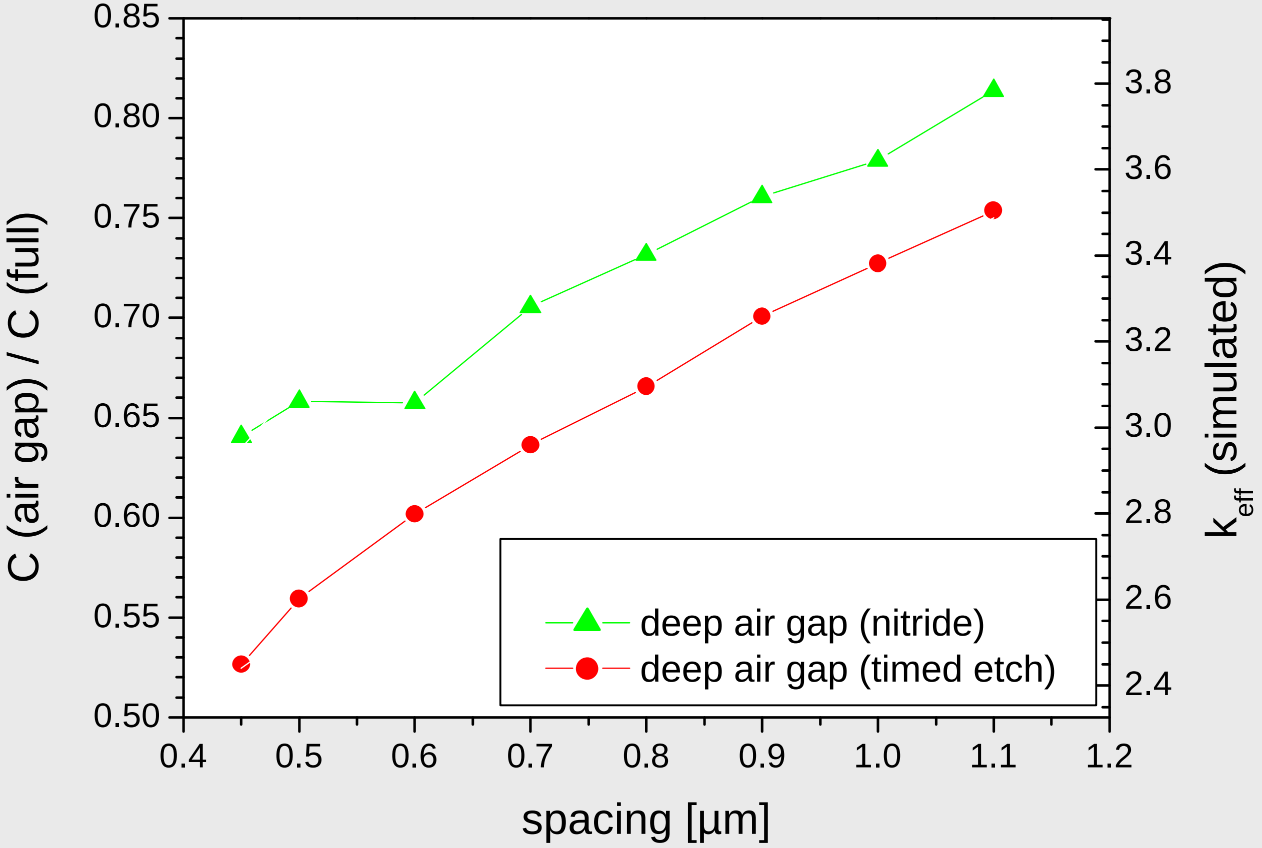

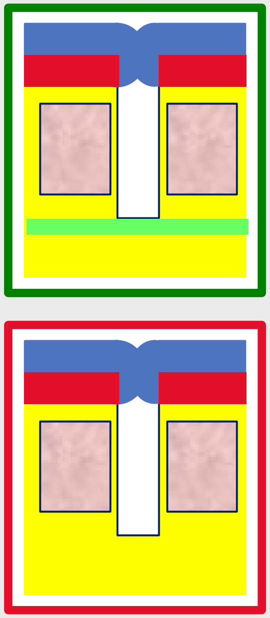

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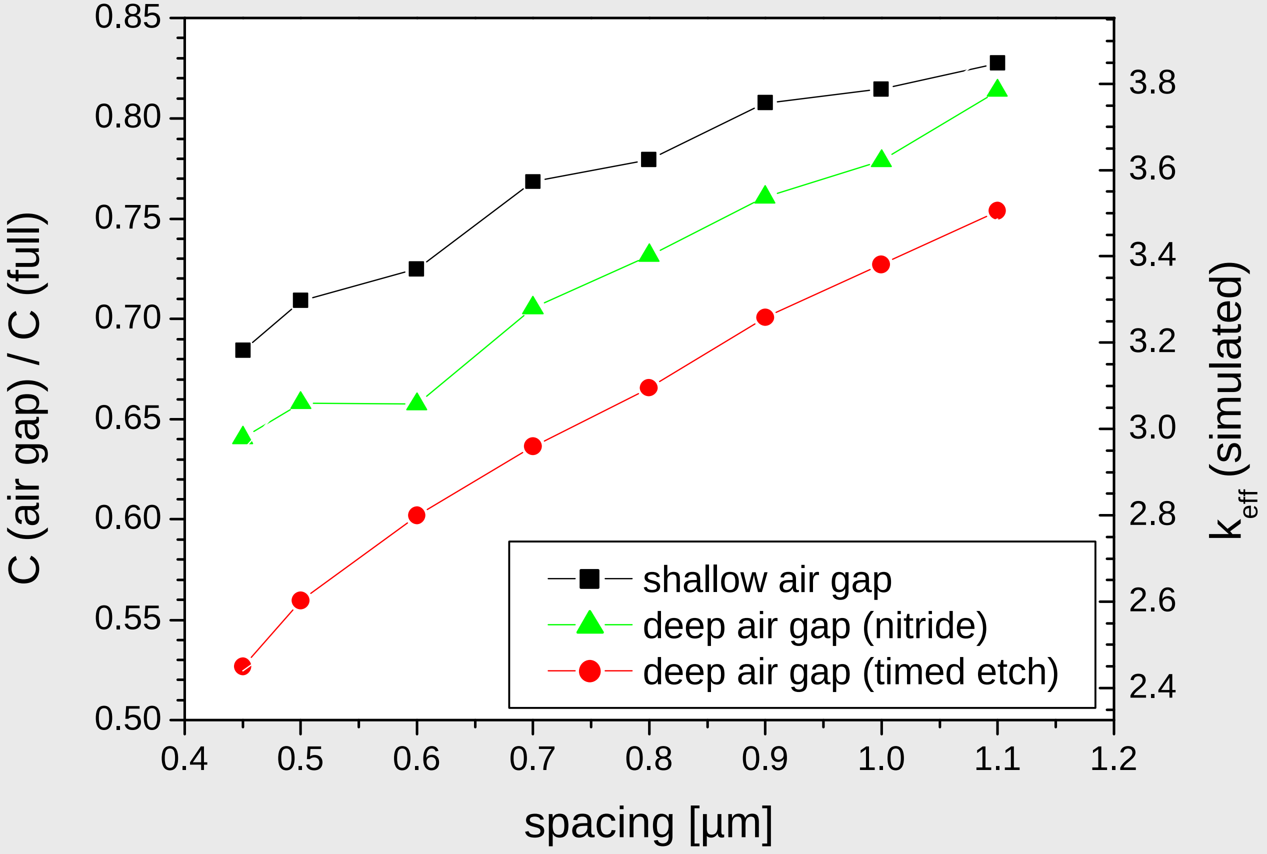

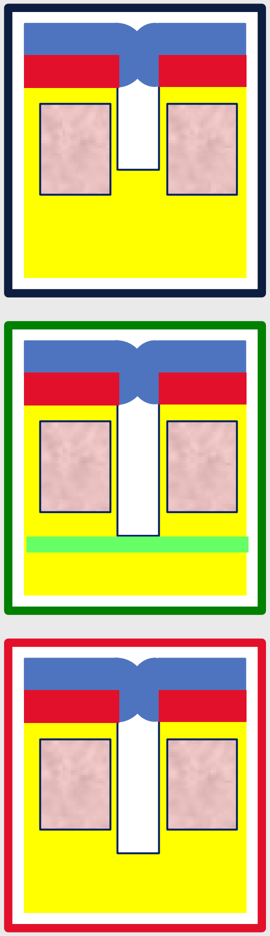

air gap width: 0.38 µm
line width: 0.5 µm
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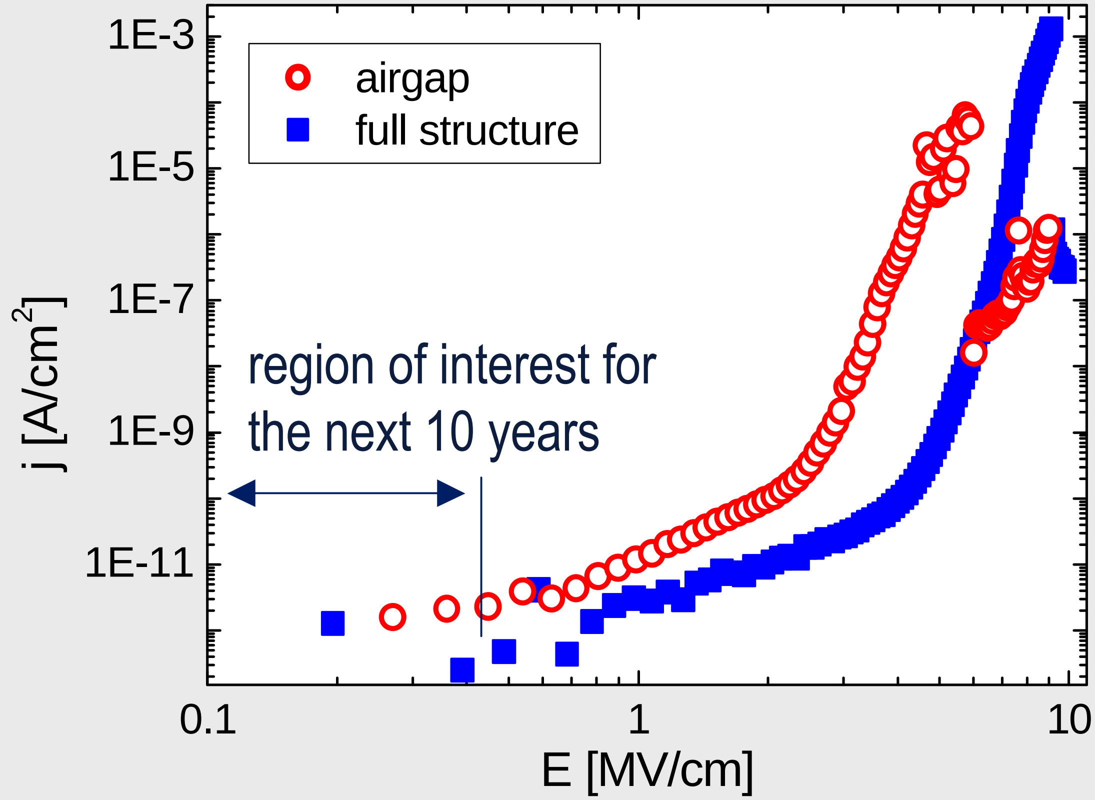
CPR‘s First Air Gaps

Electrical Measurements: Leakage Current



region of interest for the next 10 years

- Degradation of break-down field for air gap structures
- No degradation of leakage current for moderate fields as required by the ITRS roadmap for the next 10 years.

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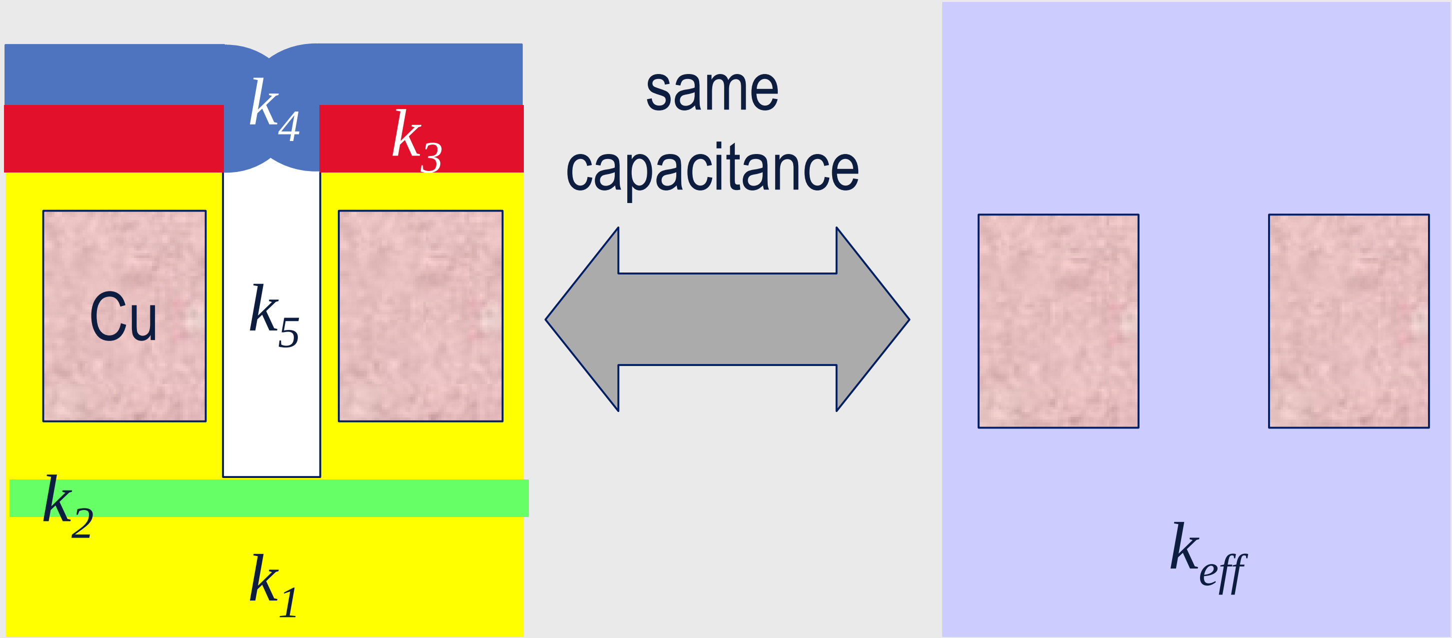
Air Gap Technology

Simulation of Line-to-line Capacitance

Effective *k* value (k_{eff})

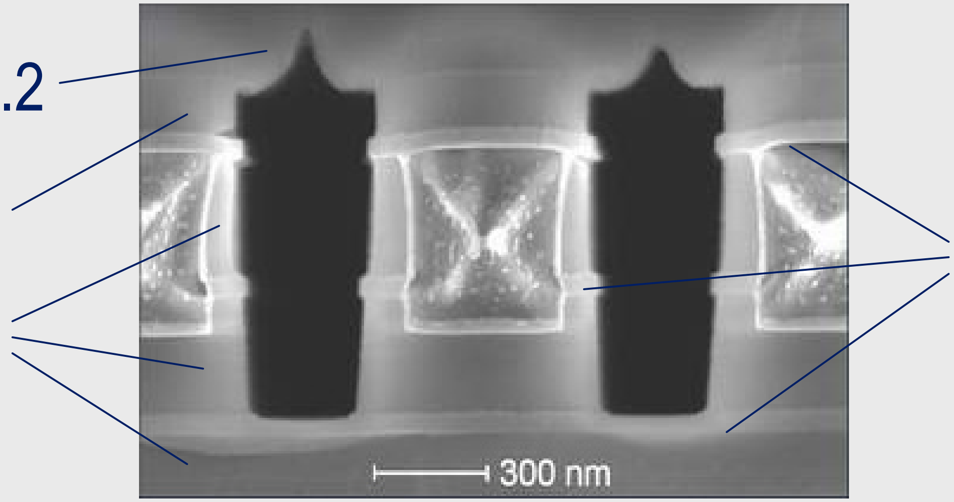
- *k* value of a fictitous uniform material where the same line-to-line capacitance would be measured as for the real, layered structure



Air Gap Technology

Simulation of Line-to-line Capacitance

- Numerical solution of Laplace equation by “Maxwell 2D“ (Ansoft Corp.)
- Input data:
  - geometrical dimensions
  - dielectric constants of used materials



$k_{\text{O3/TEOS}} = 4.2$

$k_{\text{“Seed“}} = 4.5$

$k_{\text{“Base“}} = 4.3$

$k_{\text{Nitride}} = 7.5$

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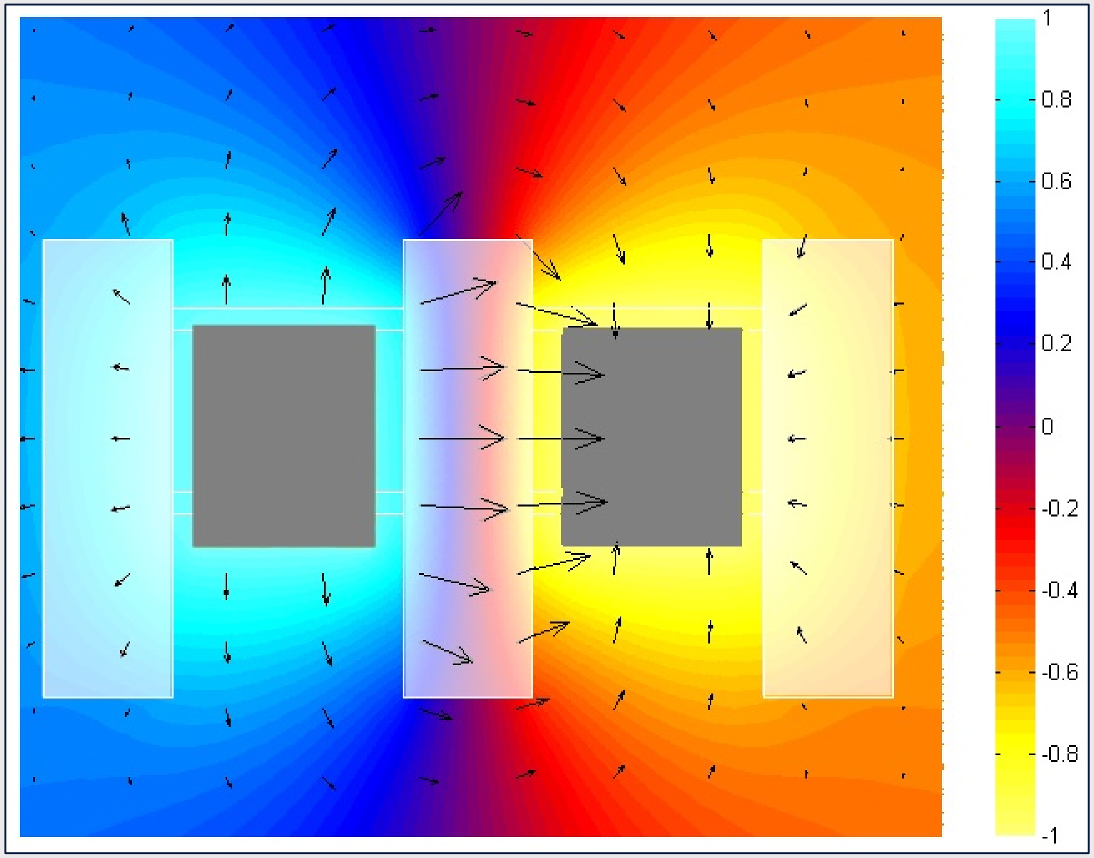
Air Gap Technology

Simulation of Line-to-line Capacitance



Simulation of
- electric field (arrows) and
- potential (color shades)
of an air gap structure.

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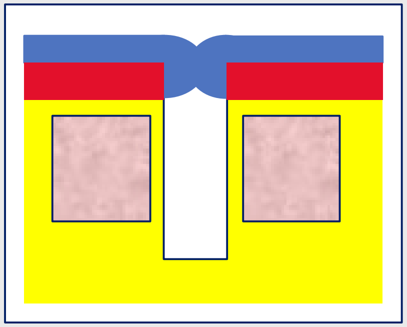
June 2003

Air Gap Technology

Simulation of Line-to-line Capacitance

Discussion of geometrical effects

Structure	Capacitance ratio	k_{eff}
0.35 µm wide air gap, centered	53.7 %	2.5



measured value:
52.5 %

Air Gap Technology

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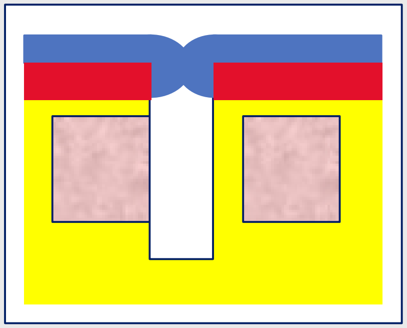
Discussion of geometrical effects

Structure	Capacitance ratio	k_{eff}
0.35 µm wide air gap, centered	53.7 %	2.5
0.35 µm wide air gap, max. misalignment	52.7 %	2.5



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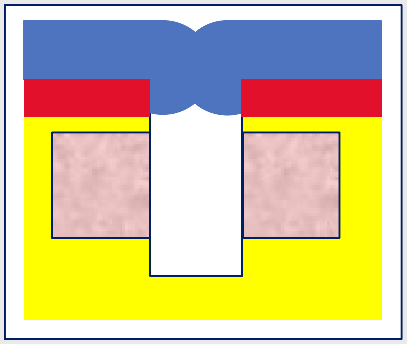
Air Gap Technology

Simulation of Line-to-line Capacitance

Discussion of geometrical effects

Structure	Capacitance ratio	k_{eff}
0.35 µm wide air gap, centered	53.7 %	2.5
0.35 µm wide air gap, max. misalignment	52.7 %	2.5
0.5 µm wide air gap (no spacers)	44.4 %	2.1



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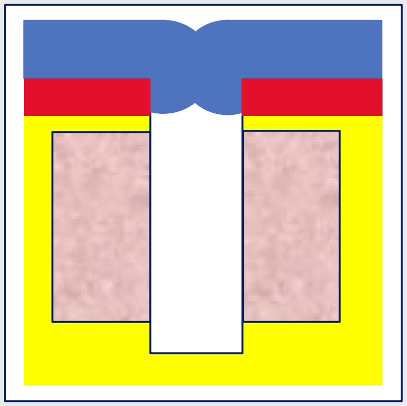
Air Gap Technology

Simulation of Line-to-line Capacitance

Discussion of geometrical effects

Structure	Capacitance ratio	*k*
0.35 µm wide air gap, centered	53.7 %	
0.35 µm wide air gap, max. misalignment	52.7 %	2.5
0.5 µm wide air gap (no spacers)	44.4 %	2.1
Like 3rd case, but: line aspect ratio = 2	37.9 %	1.7

ITRS Requirement > 2015



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IFX CPR Air Gap Technology

Outlook

- Reliability measurements
- Find a self-aligned process

Conclusions

- **Resistivity:**
  $\rho < 2.2\ \mu\Omega$ cm cannot be met even at reduced temperatures for < 40 nm conductor dimensions (“Size effect“).
- **Diffusion barriers:**
  Ta films of a few nm are sufficient.
- **Dielectric constant:**
  Air gap technology can reduce *effective* dielectric constant down to < 1.7.

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