Nano-Scale Zirconia and Hafnia Dielectrics Grown by Atomic Layer Deposition: Crystallinity, Interface Structures and Electrical Properties

Hyoungsub Kim[1,2], Paul C. McIntyre[1], and Krishna C. Saraswat[2]
[1]Materials Science and Engineering, Stanford University
[2]Electrical Engineering, Stanford University

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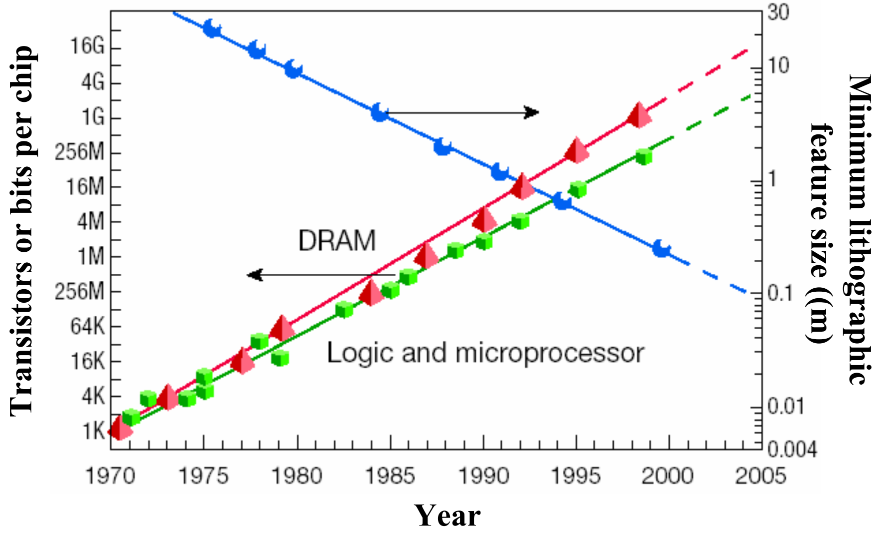
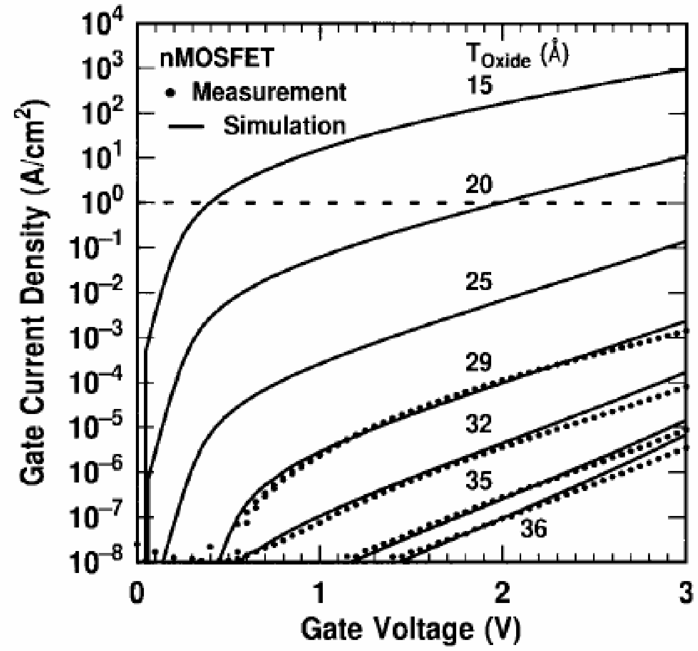
Outline

- Introduction
- Experimental
- ALD-ZrO_2 and HfO_2 on Silicon Substrates
- ALD-ZrO_2 and HfO_2 on Germanium Substrates
- Conclusions

The Need for High-*k* Gate Dielectrics



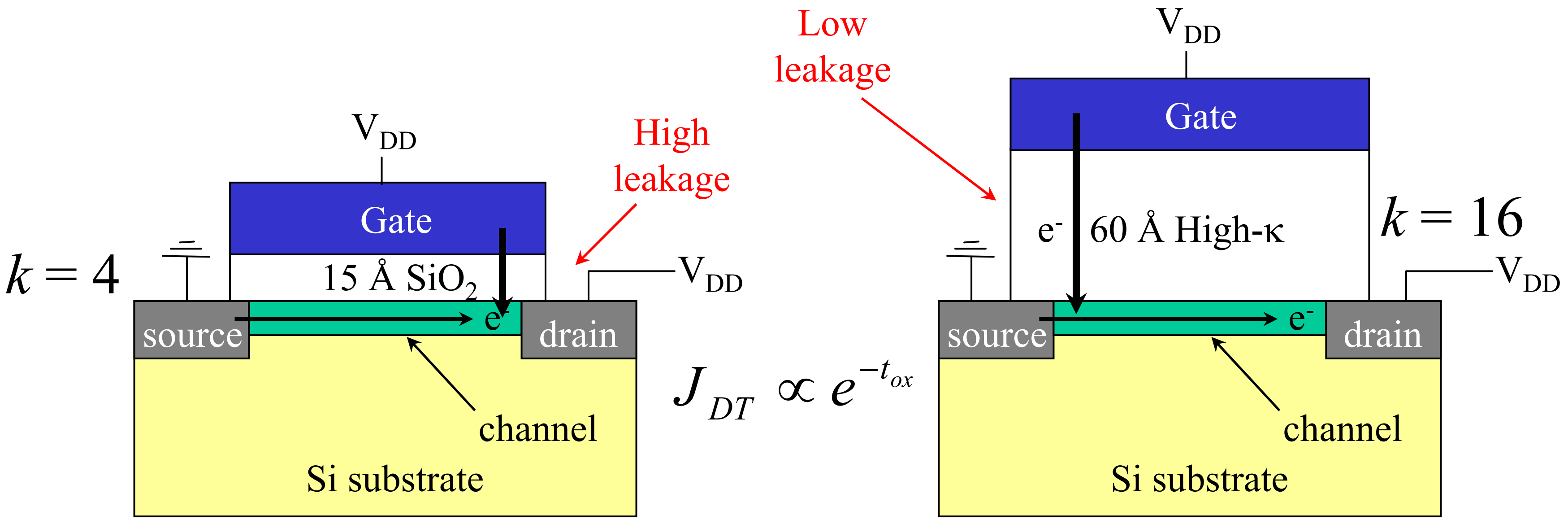
A. I. Kingon et al., Nature **406**, 1032 (2000).



S.-H. Lo et al., IEEE Electron Device Lett. **18**, 209 (1997).

- The scaling of metal-oxide-semiconductor (MOS) devices to sub-nanometer feature sizes requires **thin gate insulators**.
- **Leakage current** caused by electron tunneling increases exponentially with decreasing dielectrics thickness.
- Using high-*k* materials allows deposition of thick films with an effective thickness equivalent to thin SiO_2 films.

Benefits of High-κ Gate Dielectrics



$$J_{DT} \propto e^{-t_{ox}}$$

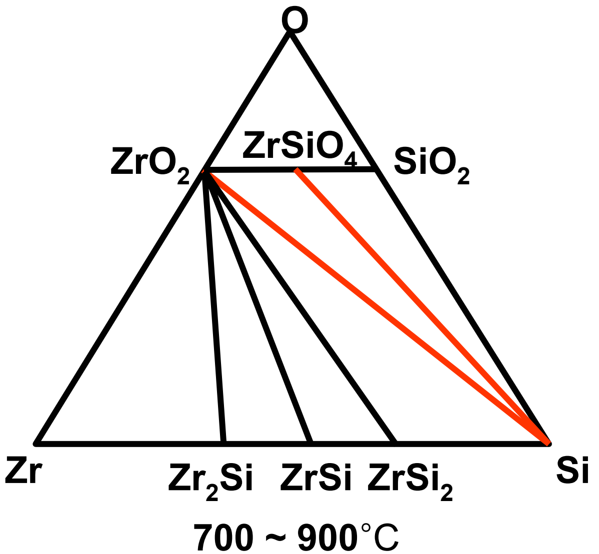
Higher-κ film ⇒ thicker gate dielectric ⇒ lower leakage and power dissipation with the same capacitance

$$C_{ox} = \frac{\kappa \varepsilon_0 A}{t_{ox}} \Rightarrow t_{high-\kappa} = \left(\frac{\kappa_{high-\kappa}}{\kappa_{SiO_2}} \right) \cdot t_{SiO_2}$$

What factors need to be included in choosing a high-*k* replacement?

Desirable High-*k* Gate Dielectric Properties

Material Properties	Electrical Properties
k> 15; uniform	Equivalent Tox < 1 nm
Thermally stable on Si (no **need** for barrier layer)	Low leakage current at the same equivalent Tox
No reaction with electrode (stop B penetration if poly-Si)	No mobility degradation (low interface trap density)

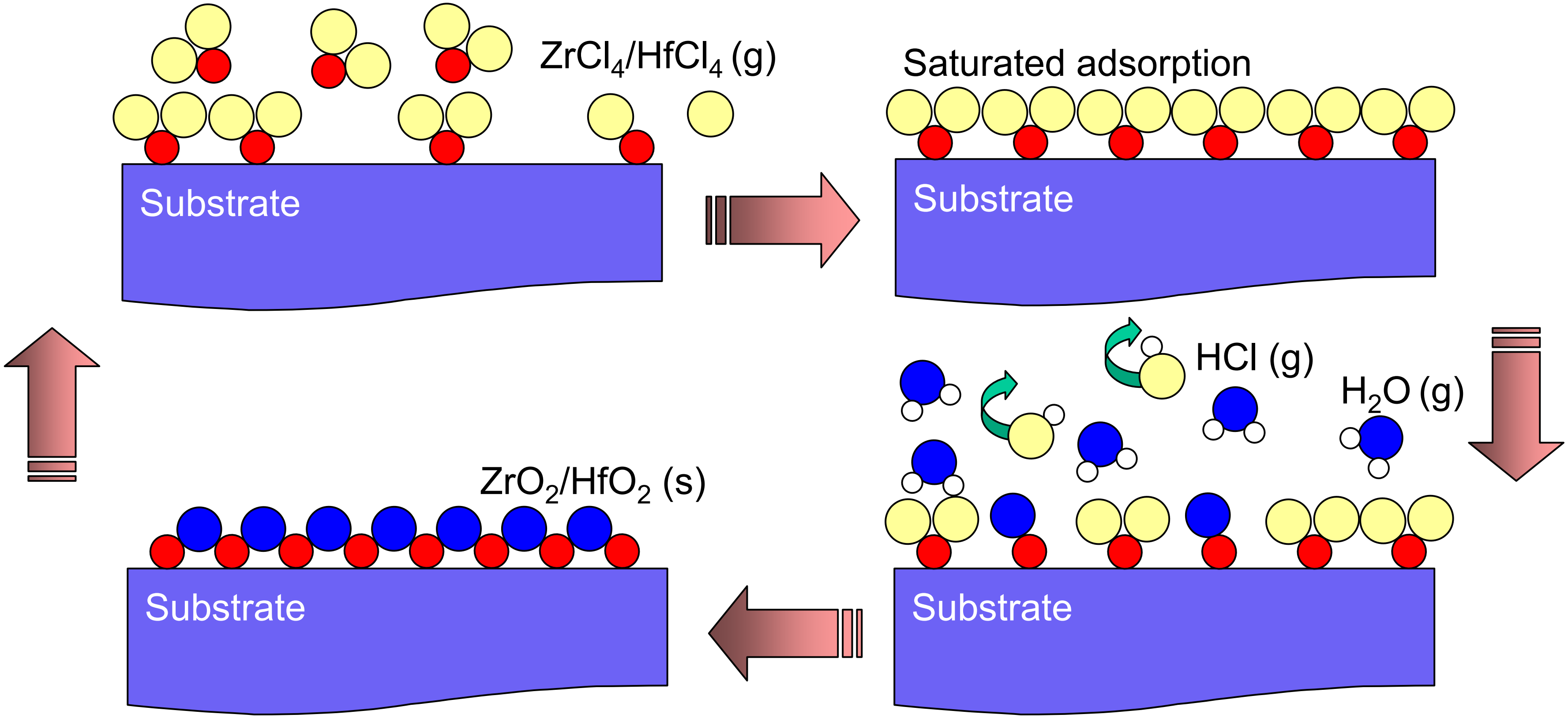


700 ~ 900°C

Ref.) Beyers et.al, J.Appl.Phys., 56, 147(1984)

Material	**SiO_2**	**ZrO_2/HfO_2**	**Silicate (Zr,Hf)**
Dielectric Constant	3.9	**~25**	15 ~ 25
Band Gap (eV)	8.9	**~5.7**	~6

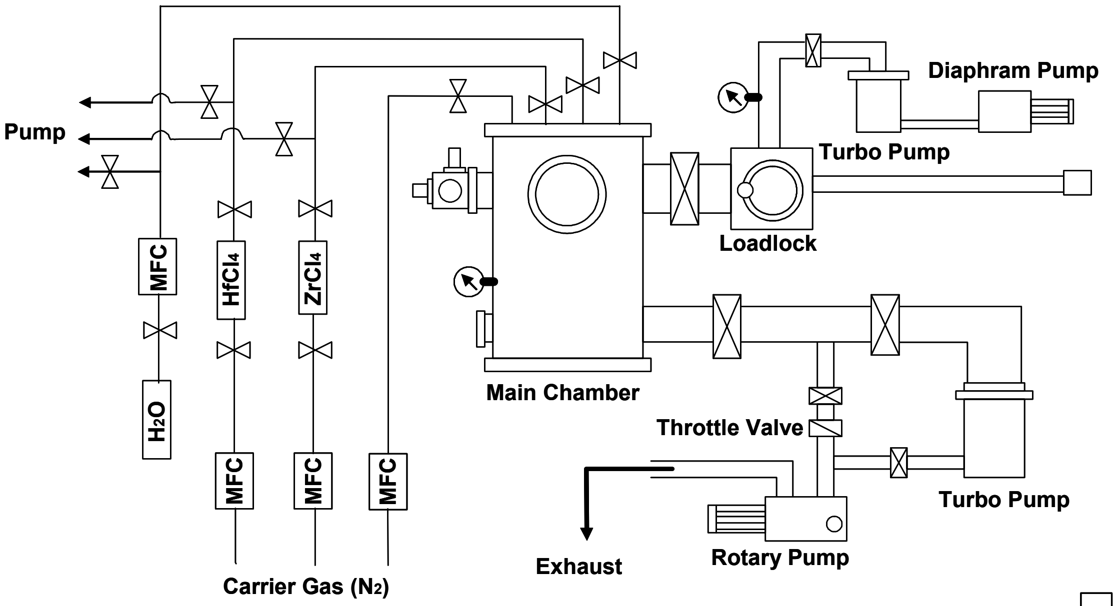
Atomic Layer Deposition



- Surface saturation controlled process
- Layer-by-layer deposition process
- Excellent film quality and step coverage

Experimental Conditions

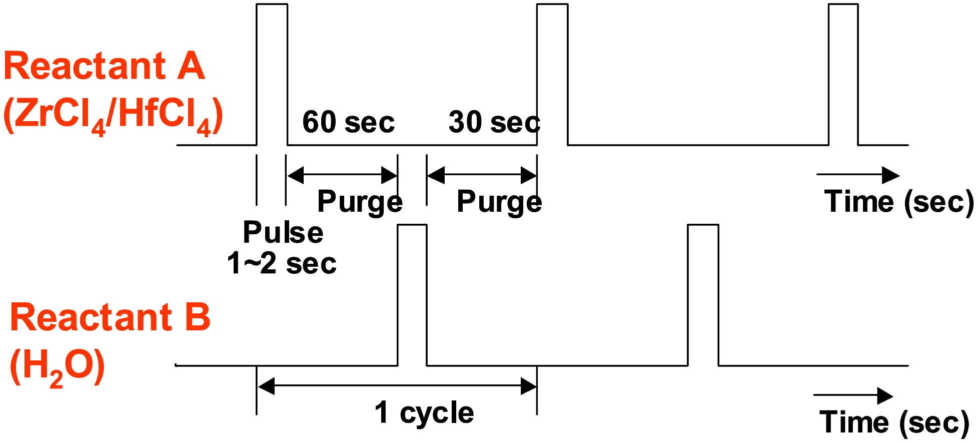
• Deposition system



- Cold wall and resistive heating type ALD system
- Load-lock and high vacuum chamber (~10^{-8} Torr)
- Solid ($ZrCl_4$/$HfCl_4$) and liquid source (H_2O) delivery system

• Deposition parameters

- Process temperature : 300°C
- Process pressure : 0.5 Torr
- Source temperature :
  - H_2O (liquid) = R.T.
  - $ZrCl_4$/$HfCl_4$ (solid) = 150°C



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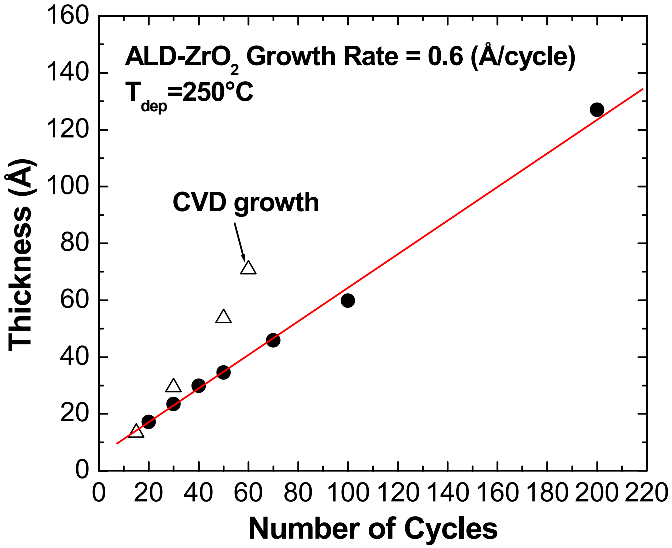
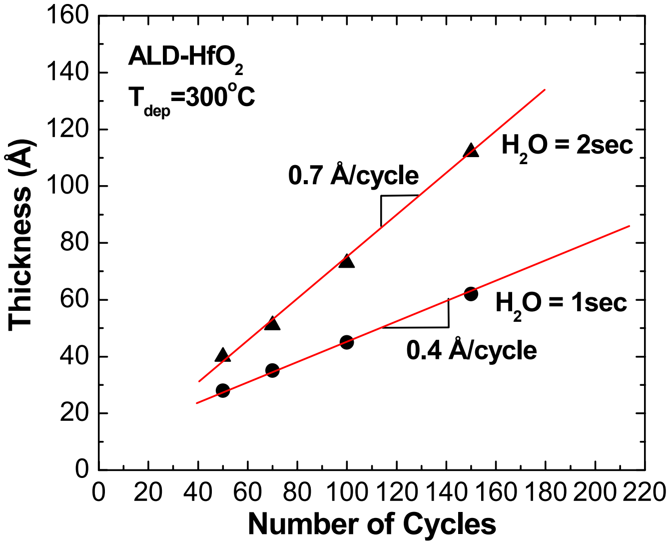
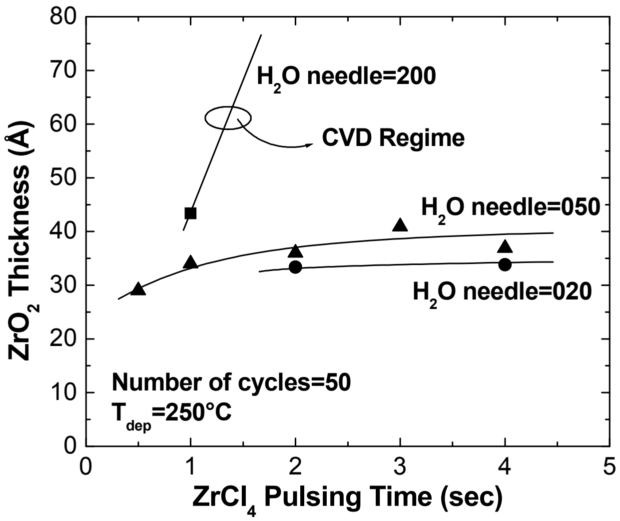
Growth Kinetics of ALD-ZrO_2 and HfO_2

- Linear growth rate (sub-monolayer growth rate)





- Independent of precursor pulsing time

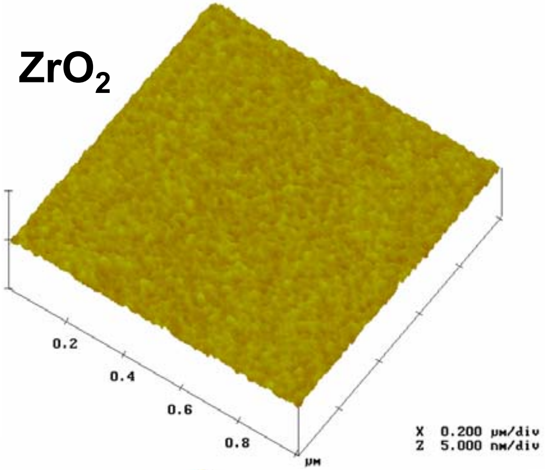


ALD of Metal Oxide Gate Dielectrics

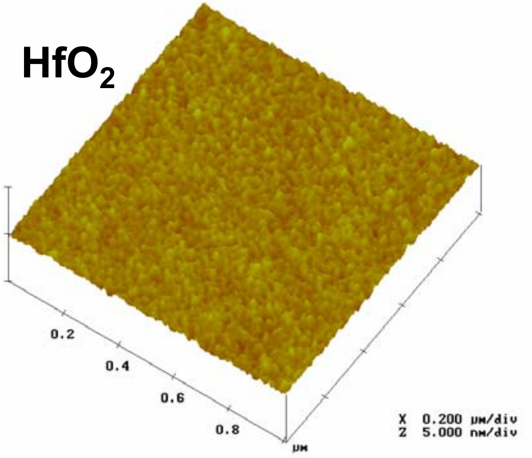
- **Excellent film quality and step coverage**

RMS roughness < 0.15nm for 3nm ZrO_2 & HfO_2

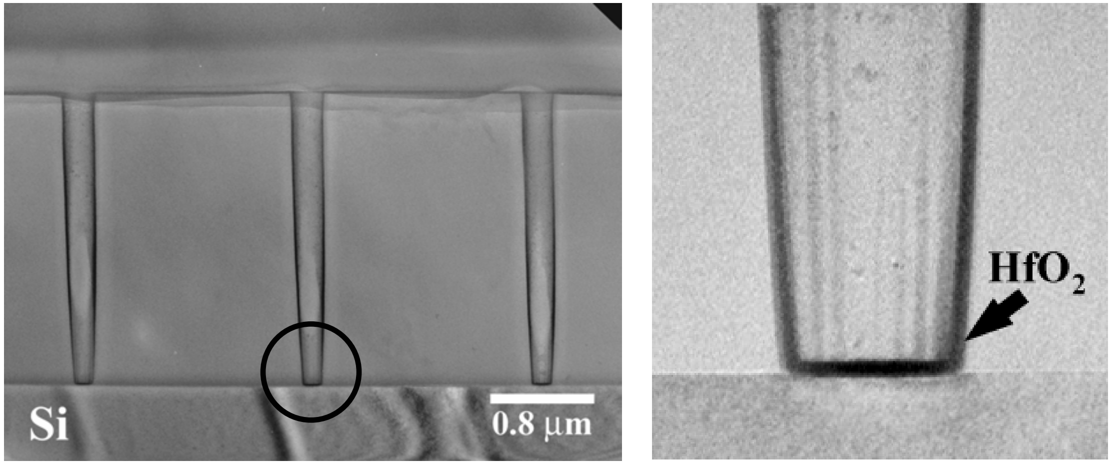
ZrO_2

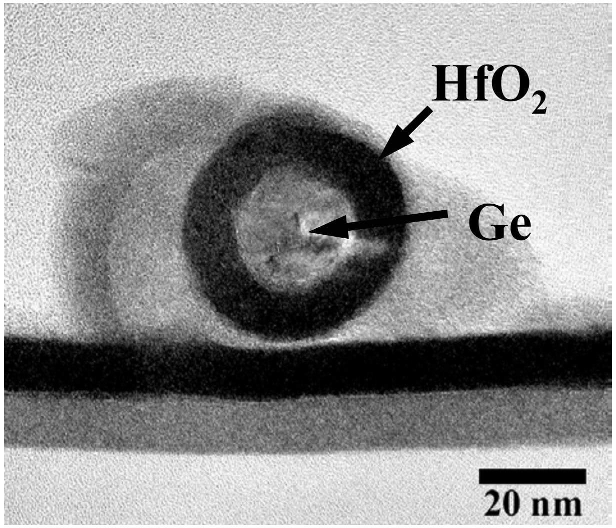


HfO_2



Excellent conformality : ~100% on A/R 10





HfO_2 (10nm)/Ge-nanowire (20 nm diameter)

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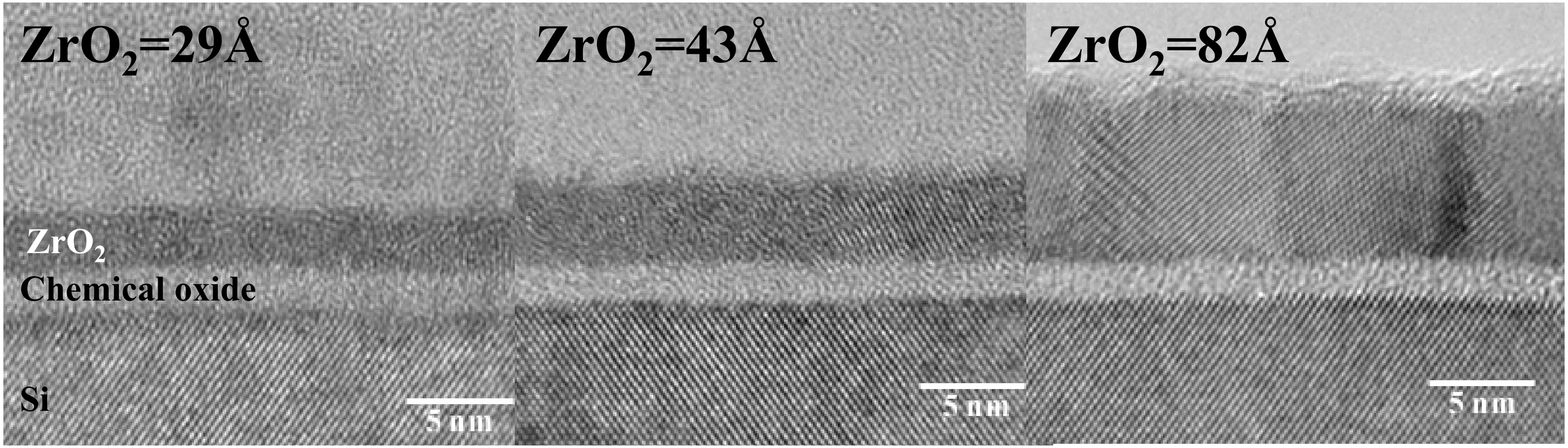
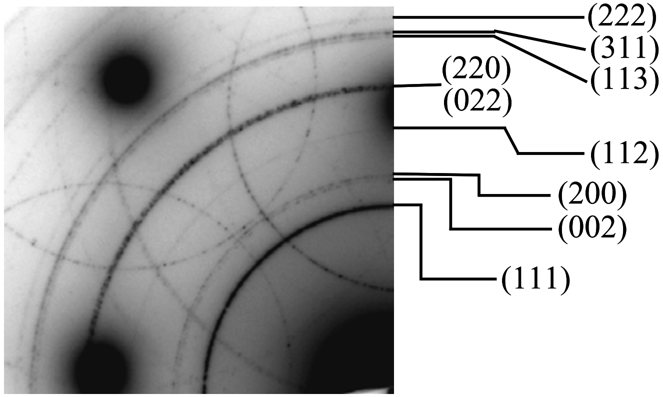
- Experimental
- ALD-ZrO_2 and HfO_2 on Silicon Substrates
  - Microstructural and electrical properties of ZrO_2 and HfO_2
  - Crystallization kinetics of ALD-HfO_2 using *in-situ* TEM
  - Effect of crystallization of ALD-HfO_2 on the electrical properties using *in-situ* and *ex-situ* annealing
  - Interface engineering using reactive metal electrodes
- ALD-ZrO_2 and HfO_2 on Germanium Substrates
- Conclusions

Microstructure of ALD-ZrO_2 on SiO_2/Si Substrate

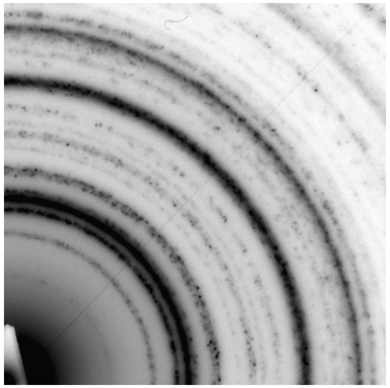


Thin ZrO_2 < 140Ă



Tetragonal

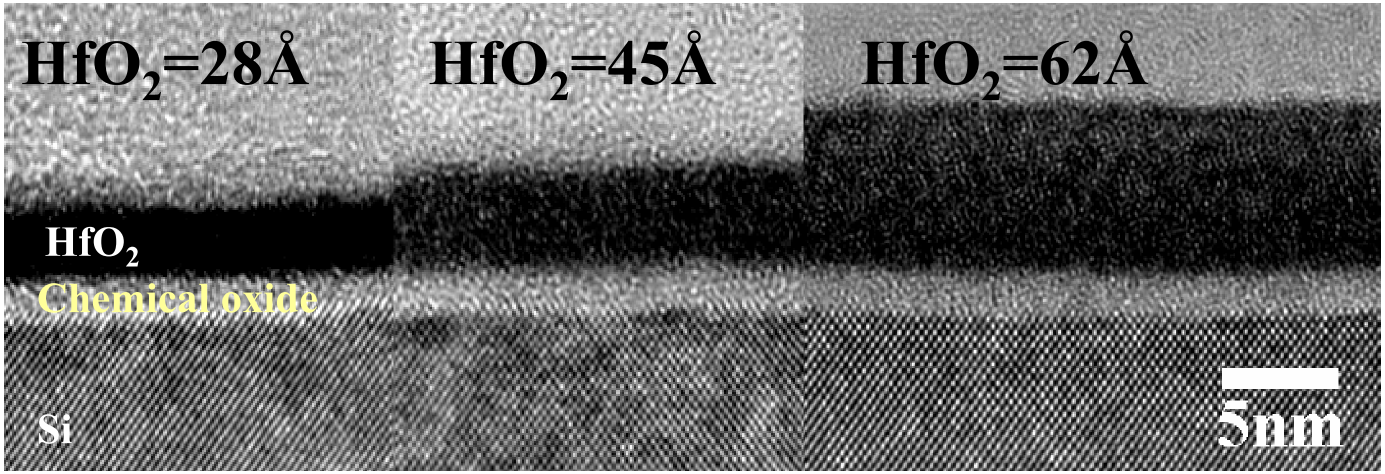
Thick ZrO_2 > 140Ă

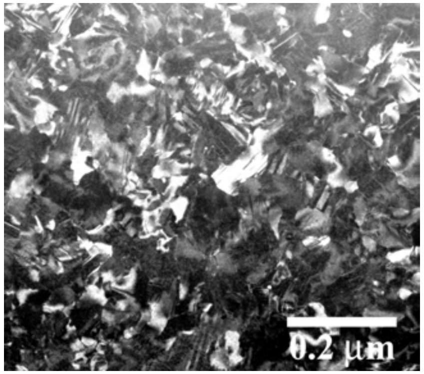


Monoclinic +Tetragonal

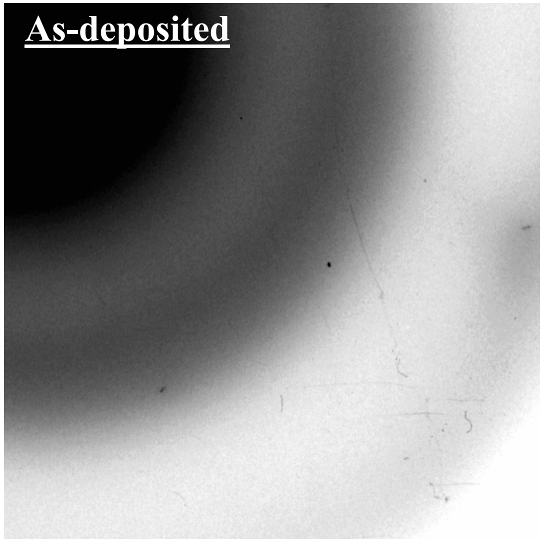
- As-deposited ALD-ZrO_2 is polycrystalline.
- Thin ZrO_2 has "tetragonal" phase; monoclinic phase present in thicker films (> 140 Å).
- ZrO_2 is composed of small nanocrystallites.

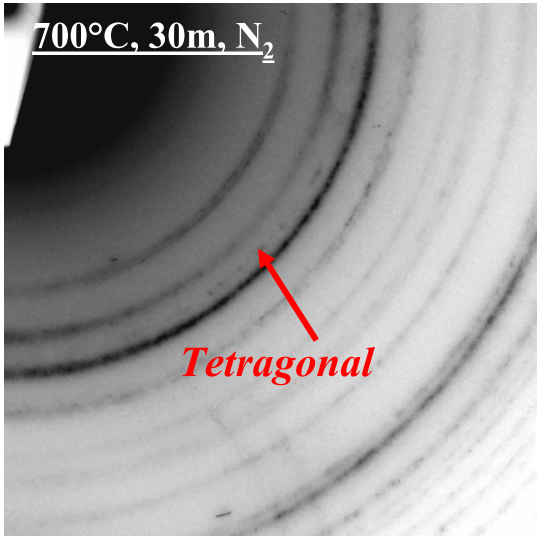
Microstructure of ALD-HfO_2 on SiO_2/Si Substrate





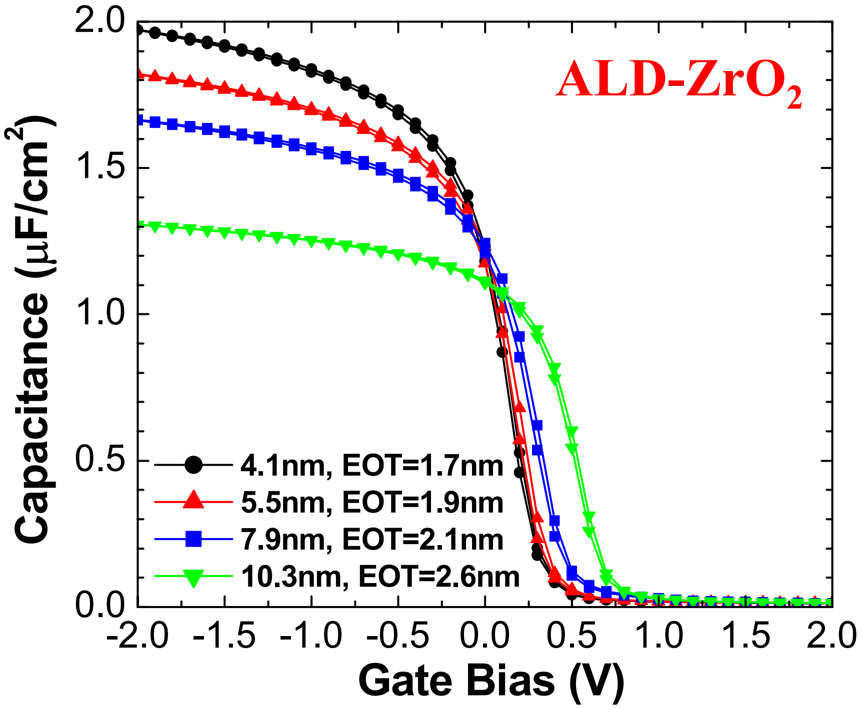
Fully crystallized HfO_2
(dark-field image)

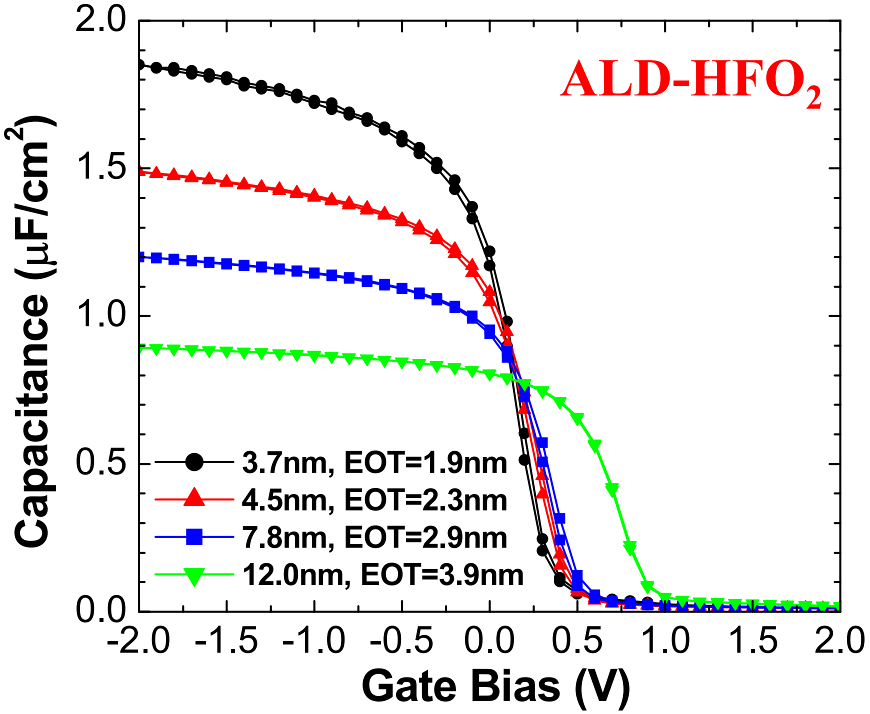




- As-deposited ALD-HfO_2 is amorphous.
- Fully crystallized HfO_2 is a mixture of monoclinic and a small amount of tetragonal phase.

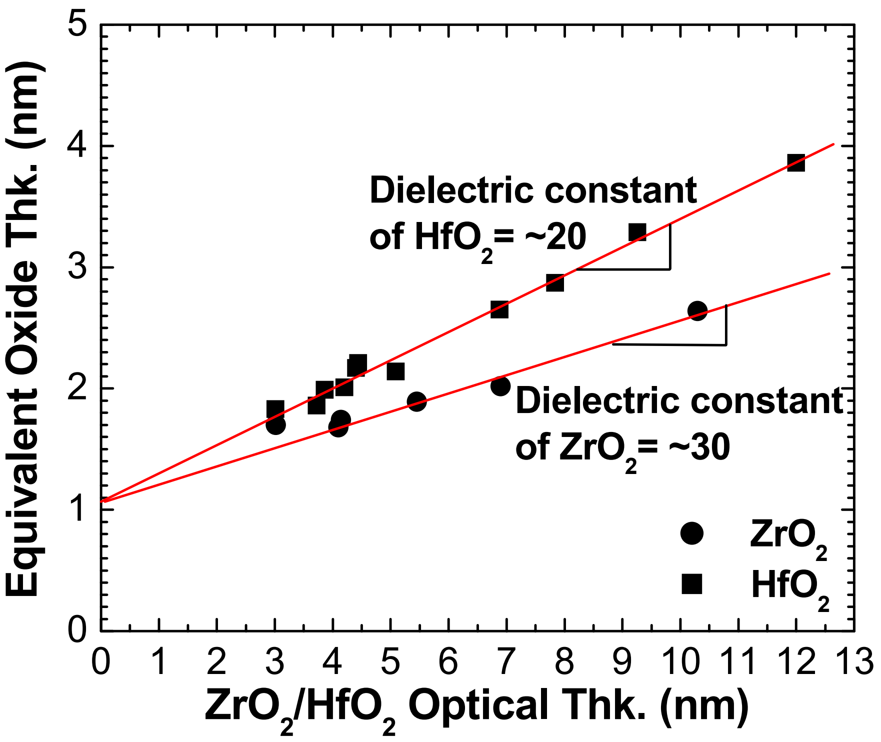
C-V Characteristics of ALD-ZrO_2 and HfO_2 on Si

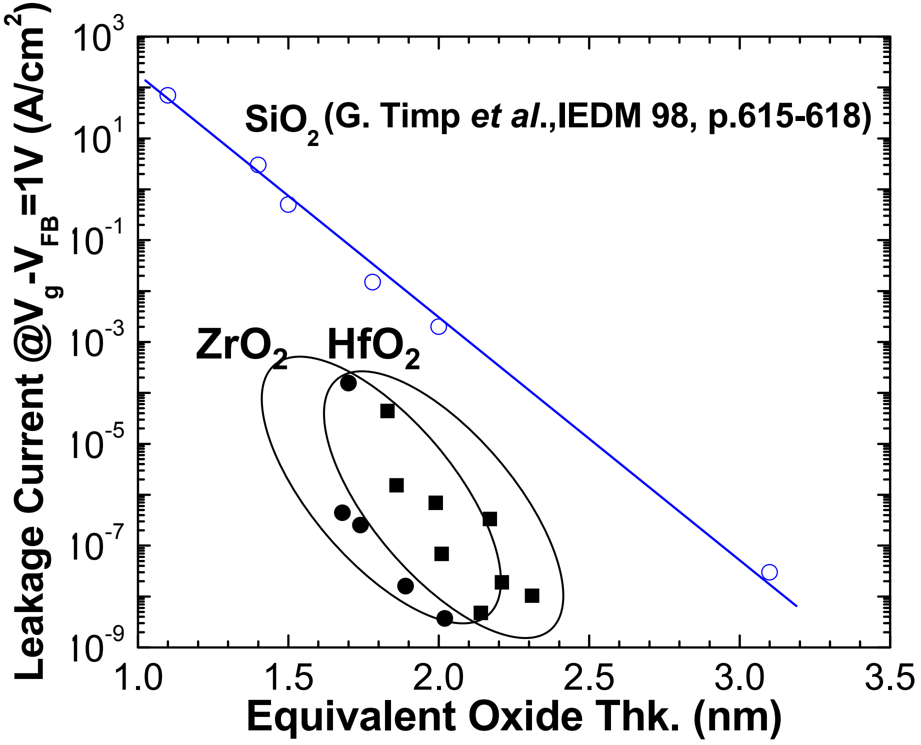




- ZrO_2 / HfO_2 film were grown at 300°C on chemical SiO_2 (~15Å).
- Series Pt electrode/ZrO_2 or HfO_2 /p-Si/Backside Al structure.
- Forming gas anneal (400°C, 30min, 4% H_2/N_2).
- Small CV hysteresis (< 30mV) for thicker films: indicates relatively low defect density of bulk traps produced by limiting Cl impurity content.

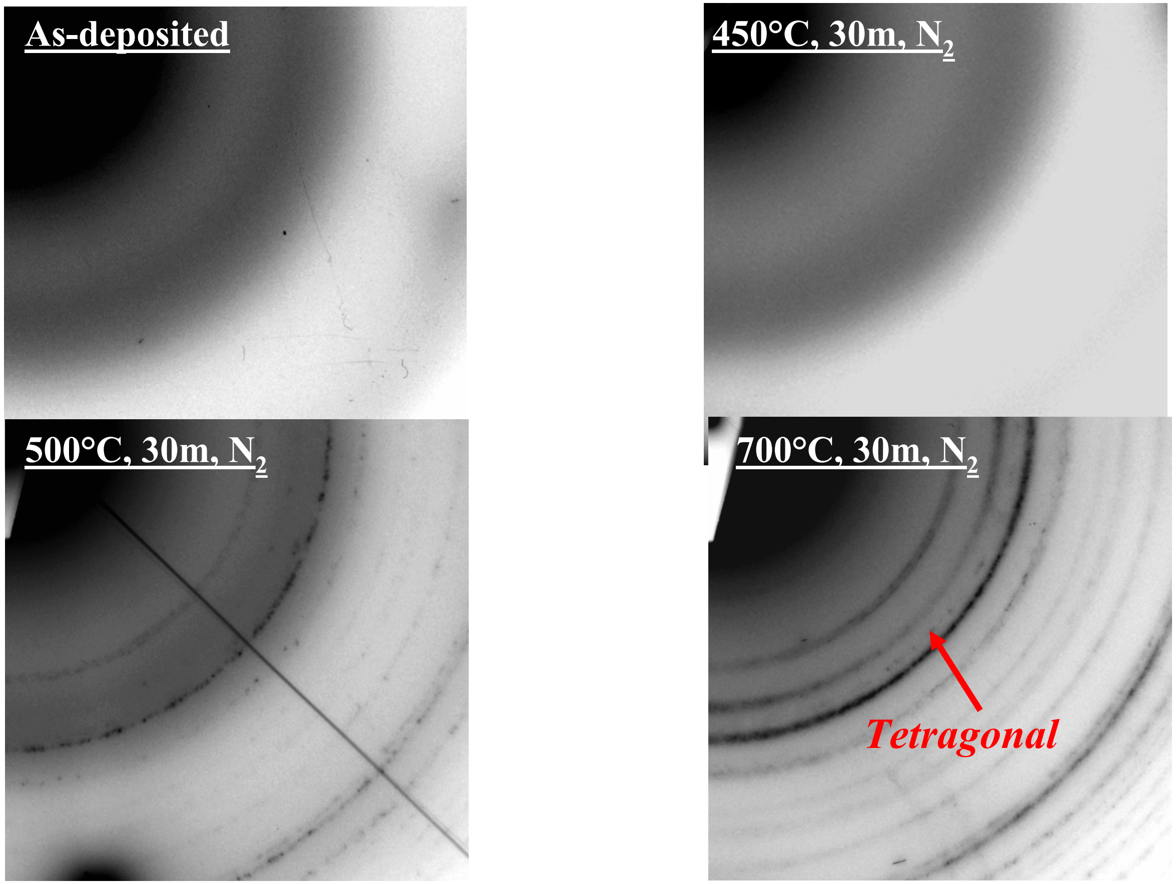
J-V Characteristics of ALD-ZrO_2 and HfO_2 on Si





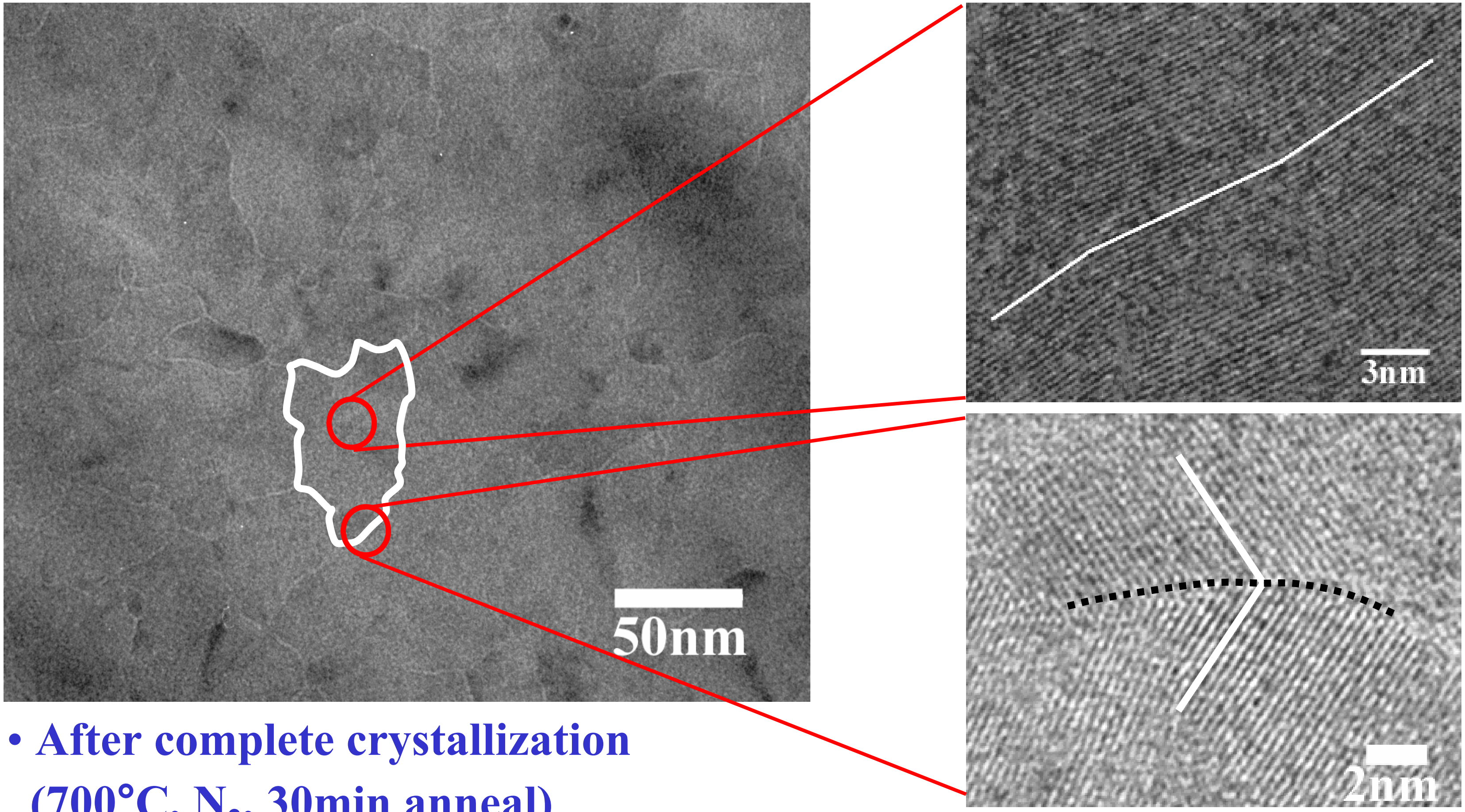
- Lower dielectric constant observed for ALD-HfO_2, possibly caused by a lower film density, as determined by x-ray reflectivity.
- Low leakage (trap assisted tunneling current) cf. SiO_2 for a similar EOT.
- No difference of leakage current mechanism between polycrystalline ZrO_2 and amorphous HfO_2 according to the leakage current density data measured as a function of temperature and applied bias .

Crystallization of ALD-HfO_2: Thermal Annealing



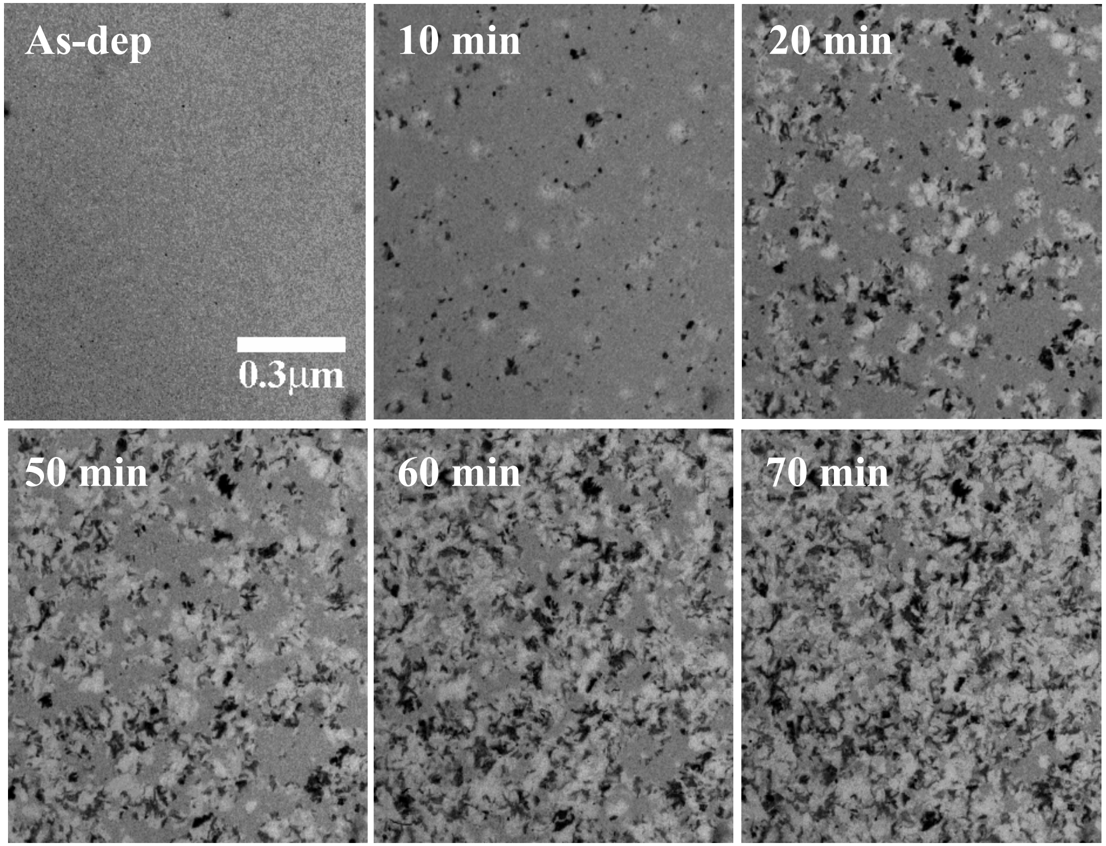
- Crystallization observed at ~ 500°C in isothermal anneals; major phase is ***monoclinic*** mixed with ***tetragonal*** (30Å HfO_2 deposited at 300°C on 25Å thermal SiO_2).

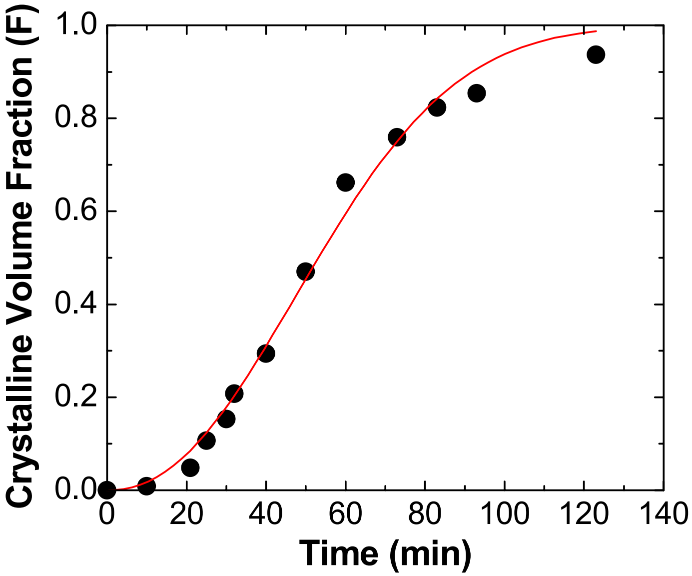
Nano-crystalline Microstructure of ALD-HfO_2 after Thermal Annealing



- **After complete crystallization (700°C, N_2, 30min anneal)**
- **Very fine subgrain structure present with numerous twin boundaries, surrounded by large-angle grain boundaries.**

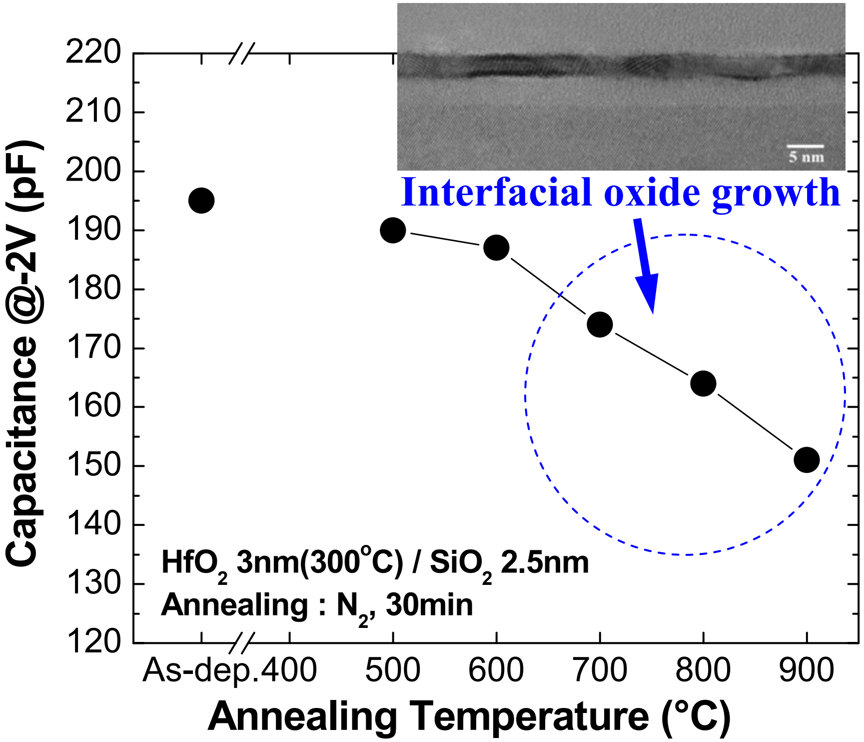
In-Situ Crystallization Kinetics of ALD-HfO_2

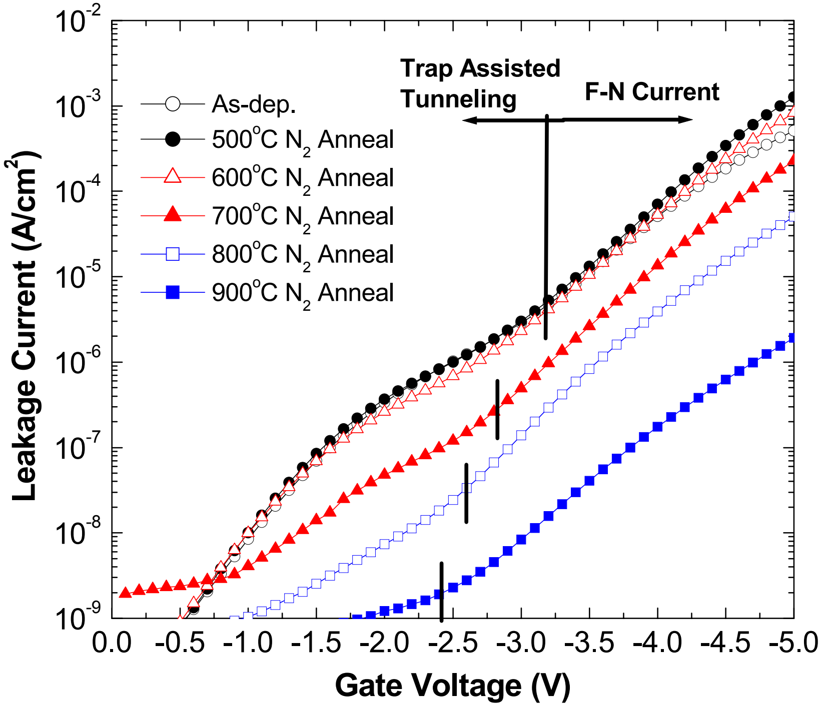




- **In-situ anneal at 520°C using 30Å HfO_2 on 25Å thermal SiO_2.**
- **Preliminary analysis shows 2-D (radial) growth with decreasing nucleation rate.**
- **Avrami isothermal transformation kinetics:** $F = 1 - \exp[-(kt)^n]$ **n~2.2**

Effects of HfO_2 Crystallization on Electrical Properties (*ex-situ* annealing)

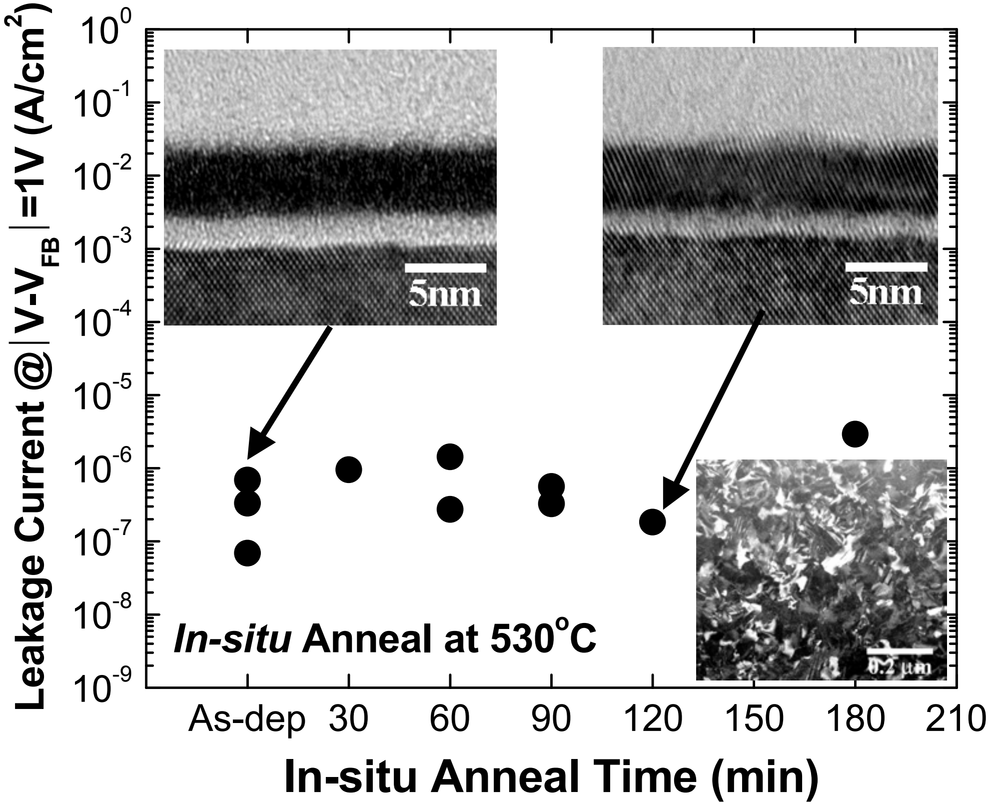




- Sample structure : 3nm HfO_2 on 2.5nm thermal SiO_2.
- After 700°C, capacitance decreases due to the interfacial oxide growth. *
- No significant increase in trap assisted tunneling leakage current resulting from crystallization.

* Reagent-grade N_2 ambient contains ~ 1 ppm O_2.

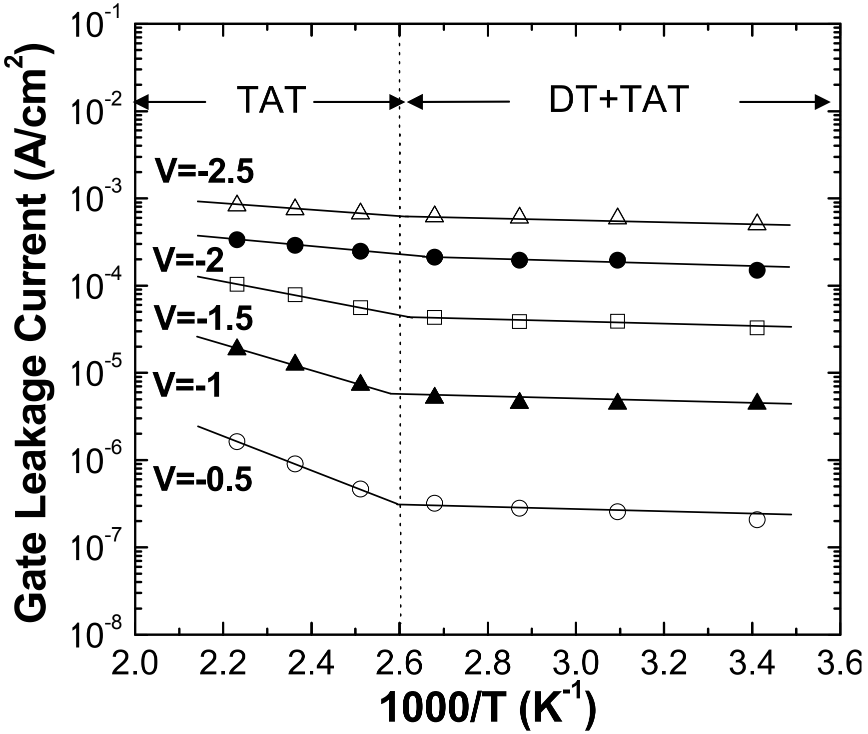
Effects of HfO_2 Crystallization on Electrical Properties (low pressure *in-situ* annealing)



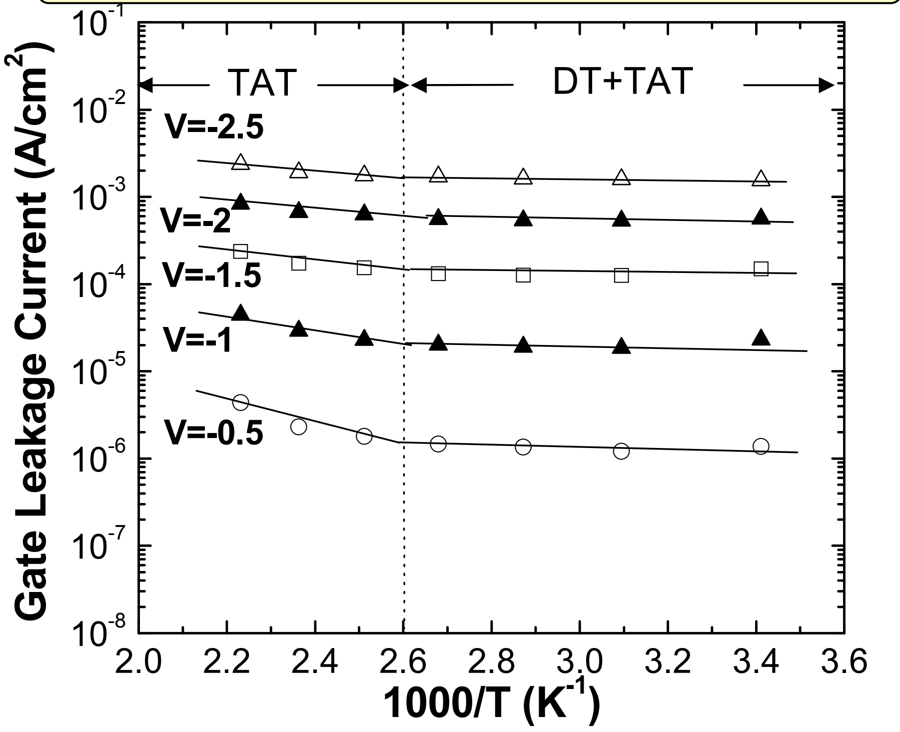
- Sample structure : ~ 4 nm HfO_2 on 1.5 nm chemical SiO_2.
- Low pressure (~1.3 Tor) *in-situ* anneal to minimize interfacial SiO_2 growth.
- No significant increase in trap assisted tunneling leakage current resulting from crystallization.

Effects of HfO_2 Crystallization on Electrical Properties (low pressure *in-situ* annealing)

As-dep. amorphous HfO_2

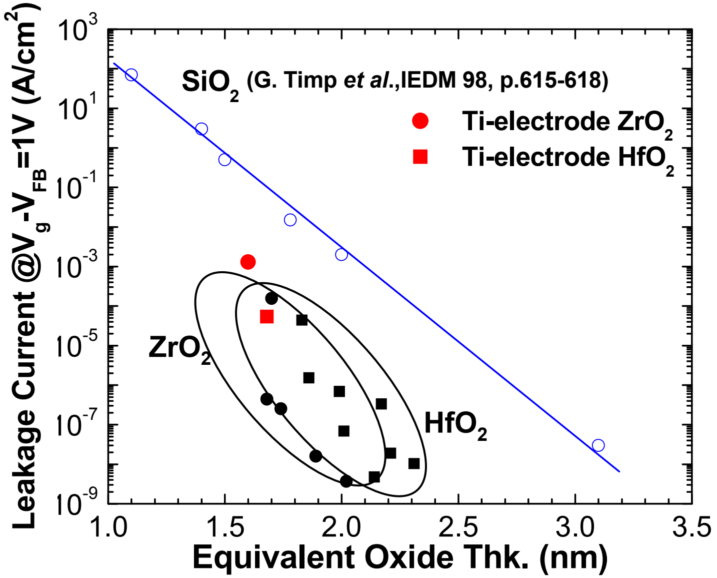


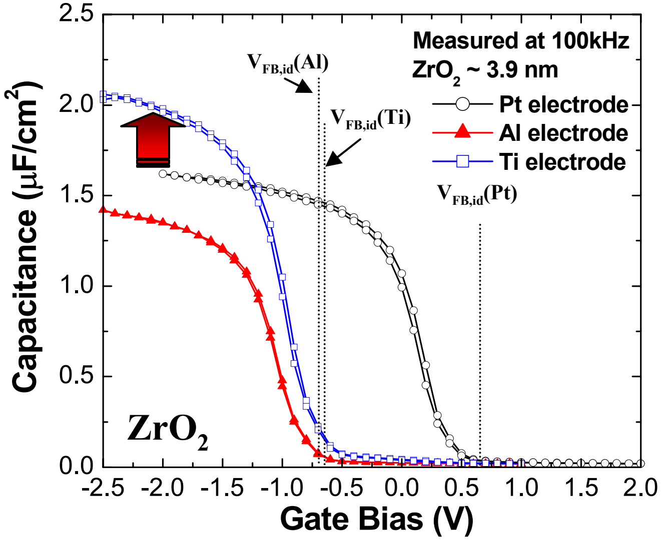
Fully crystallized HfO_2 (530°C, 120min)

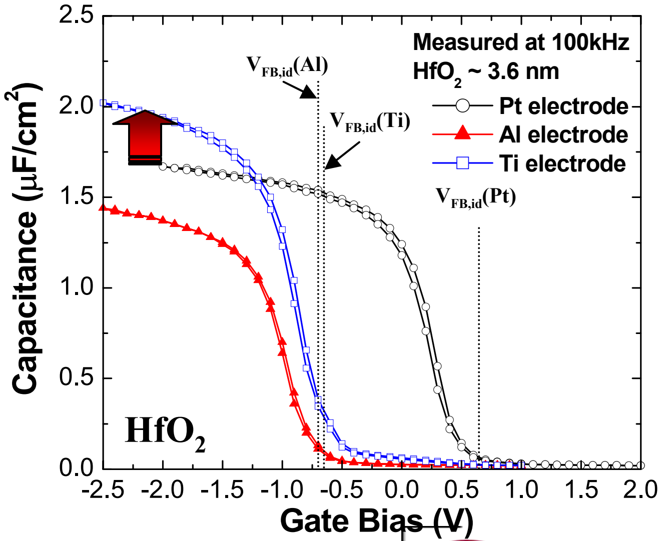


- Leakage current was measured at different measurement temperature.
- No difference of leakage current mechanism between amorphous and crystallized HfO_2.
- TAT(Trap-assisted tunneling) is the dominant leakage current mechanism.

Electrical Properties of High-*k* Dielectrics with Different Metal Electrodes



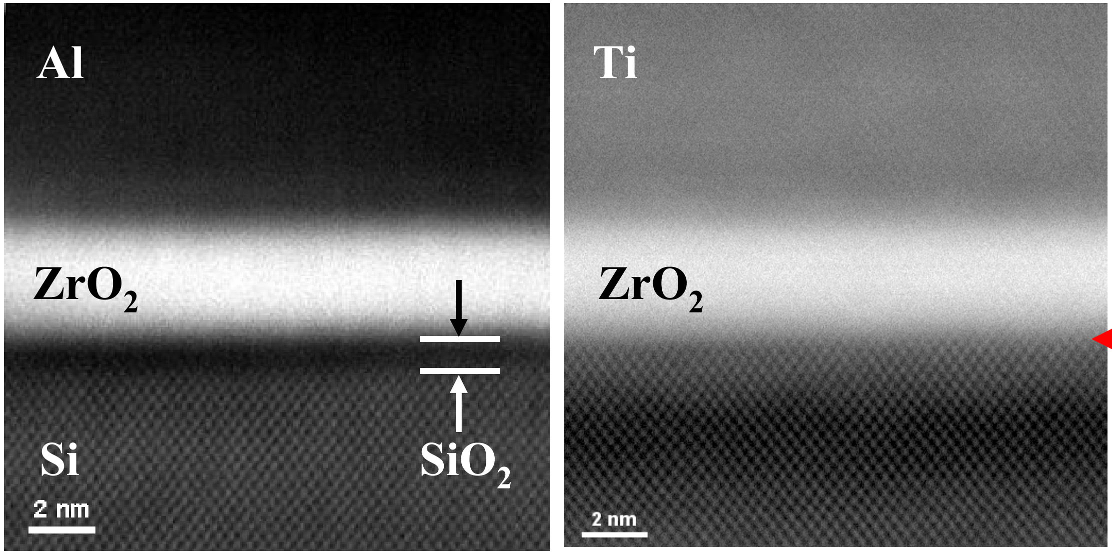




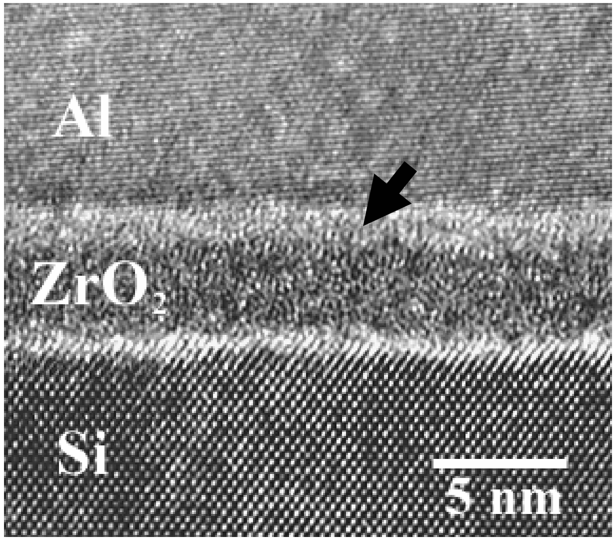
- **Metal electrodes : Pt (50 nm), Al (100 nm), Pt(50 nm)/Ti(30 nm).**
- **Ti-electroded samples show 4 ~ 5 Å smaller EOT compared to Pt-electroded samples.**
- **Al-electroded samples have higher EOT due to the interfacial reaction between Al and high-*k* gate dielectric.**
- **Reasonably low leakage current densities.**

Interface Structures: Reactive Metal Electrodes

STEM : collaboration with Prof. Susanne Stemmer (UCSB)



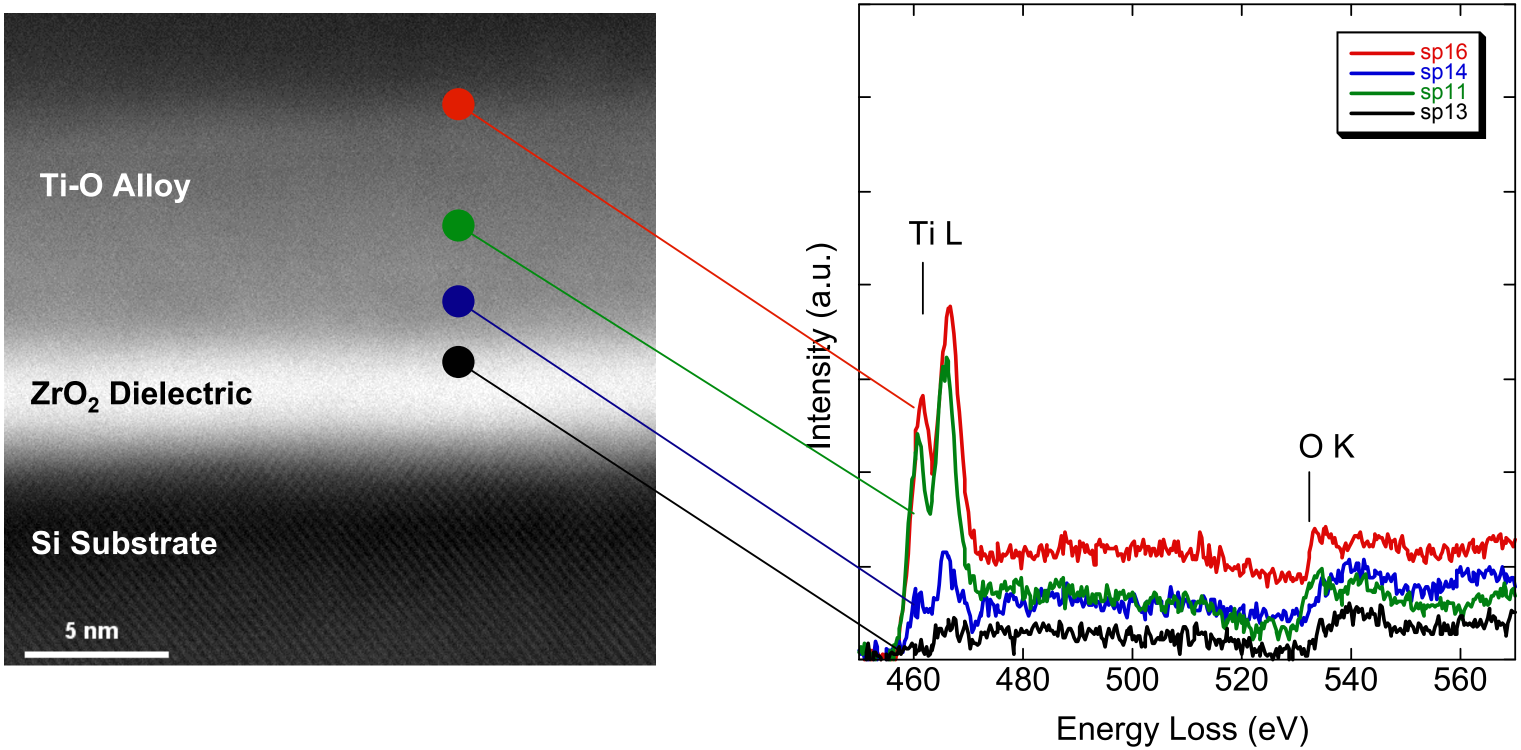
No interfacial layer



- **8 Å-thick reacted layer (Al_2O_3) between Al and high-*k* gate dielectrics.**
$|\Delta G_f(TiO_2)| < |\Delta G_f(ZrO_2)| < |\Delta Gf(Al_2O_3)|$
- **No interface oxide is observed for Ti-electroded high-*k* gate stacks.**
- **Clear interface between ZrO_2, HfO_2/Si substrate**

EELS of Ti-Electroded ZrO_2

EELS : collaboration with Prof. Susanne Stemmer (UCSB)

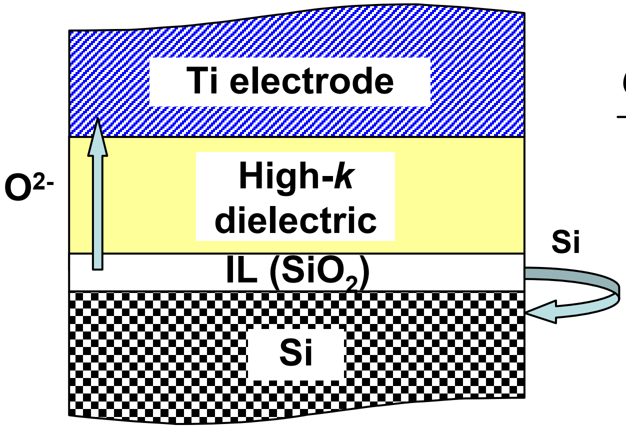


- **No detectable Ti in ZrO_2**: Ti solubility in ZrO_2 is < 4 at% @1200°C.[1]
- **Significant amount of O in Ti metal electrode**: O solid solubility in Ti is ~ 49 at% without forming a Ti-oxide.[2]

[1] R. F. Domagala, S. R. Lyon, and R. Ruh, *J. Am. Ceram. Soc.* **56**, 584 (1973).

[2] L. Murray and H. A. Wriedt, *Phase Diagrams of Binary Titanium Alloys* (ASM International, Ohio, 1987).

Thermodynamics of Ti-Electroded ZrO_2/HfO_2



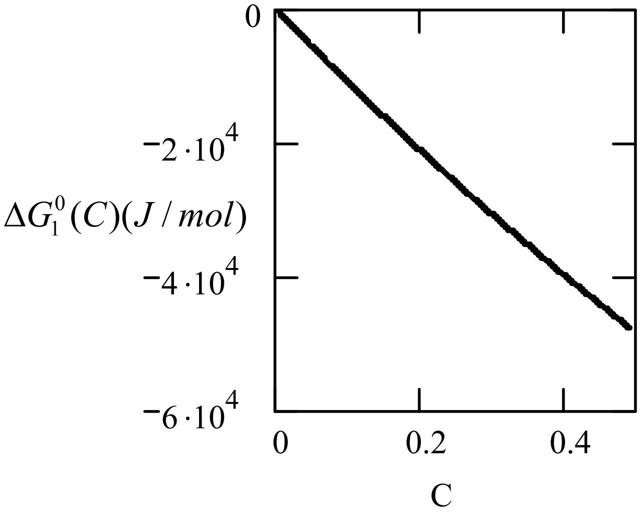
Overall Process

$$\frac{C}{2}SiO_2 + Ti \rightarrow \frac{C}{2}Si(epi.) + TiO_C \Rightarrow \Delta G_1^0(C)$$

- TiO_c is the Ti-O alloy and C is the concentration of oxygen in Ti
- According to Duhem-Margules Eq., the integral $\Delta G_f(TiO_c)$ vs. oxygen concentration in Ti

$$\Delta G^0_{f,TiO_C} = (RT/2)\int_0^C \ln P^{eq}_{O_2}\, dC^{\,1}$$

$$\ln P^{eq}_{O_2} = 21.34 + 12.45C + 2\ln[C/(1-C)] - 131{,}200/T^{\,2}$$



Strong driving force to proceed for all temperatures of interest in semiconductor processing up to solid solubility of O in Ti

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[1] O. Kubaschewski, C. B. Alcock, and P. J. Spencer, *Materials Thermochemistry* (Pergamon, Oxford, 1993), p. 35.

[2] W. E. Wang and Y. S. Kim, *J. Nucl. Mater.* **270**, 242 (1999); K. L. Komarek and M. Silver, in *Thermodynamics of Nuclear Materials* (IAEA, Vienna, 1962), p. 749.

Summary I

- Microstructural and electrical properties of ALD-ZrO_2 and HfO_2
  - as-deposited ALD-ZrO_2 (< 140 Å) is nanocrystalline in the tetragonal phase, and as-deposited ALD-HfO_2 is amorphous
  - the dielectric constant of ALD-ZrO_2 (~ 30) is higher than that of ALD-HfO_2 (~ 20)
  - the leakage current density at the same EOT is significantly lower for both oxides compared to SiO_2
- Crystallization and microstructural evolution of amorphous HfO_2
  - onset of crystallization during post-deposition anneal occurs at ~ 500°C
  - fully crystallized HfO_2 is composed of monoclinic and tetragonal phases
  - isothermal crystallization kinetics consistent with 2-D growth from initial population of HfO_2 nuclei
- Effect of HfO_2 crystallization on its electrical properties
  - *ex-situ* and *in-situ* annealing study showed negligible effect of microstructural change on the leakage current density and conduction mechanism
  - bulk or interfacial defects other than grain boundaries may control leakage

Summary I

- Interface engineering of high-*k* gate stack using a reactive metal electrode
  - Ti-electroded samples show lower EOT due to the removal of interfacial layer
  - Al-electrodes react with ZrO_2 and form an Al_2O_3 layer having a low dielectric constant at the dielectric/top electrode interface
  - Ti overlayers having a very high oxygen solubility, can effectively getter oxygen from the interface layer, thus decomposing SiO_2 and reducing the interface layer thickness in a controllable fashion
  - any reduction of ZrO_2 by Ti does not degrade MOSCAP electrical properties

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- ALD-ZrO_2 and HfO_2 on Germanium Substrates
  - Locally epitaxial growth of ZrO_2 on HF-cleaned Ge
  - ALD-ZrO_2 and HfO_2 on Ge with different surface treatments
- Conclusions

Benefits of Ge Substrates

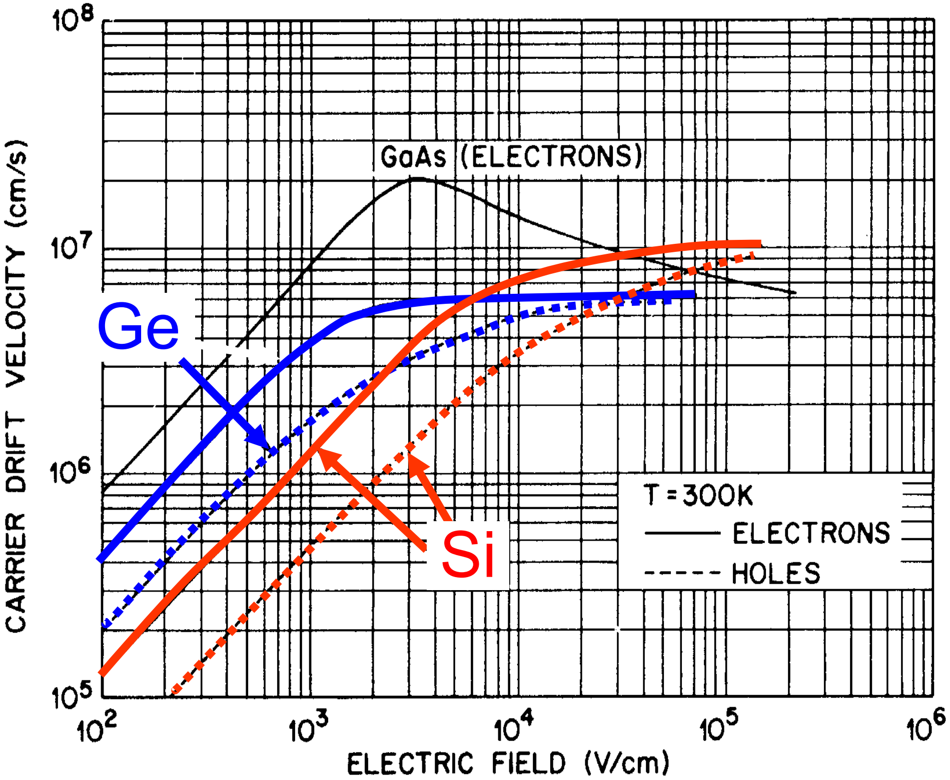
Electronic Properties:

- More symmetric and higher carrier mobilities (low-field)

=> more efficient source carrier injection due to lighter effective mass

=> decrease of CMOS gate delay:

$$\frac{C_{LOAD}V_{DD}}{I_{DS}} = \frac{L_{gate} \times V_{DD}}{(V_{DD} - V_T) \times v_{inj}}$$



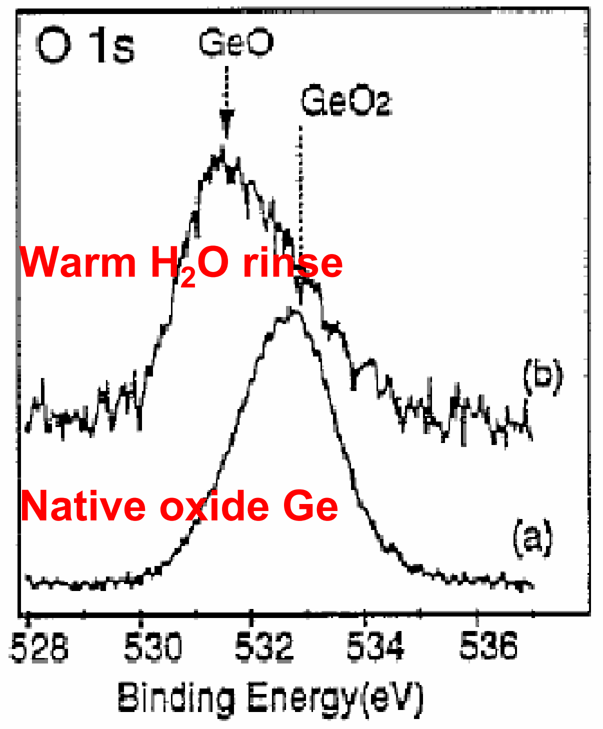
(Sze, *Phys. of Semicond. Devs. 2nd Ed.*, p.46, 1981)

Integration Problem:

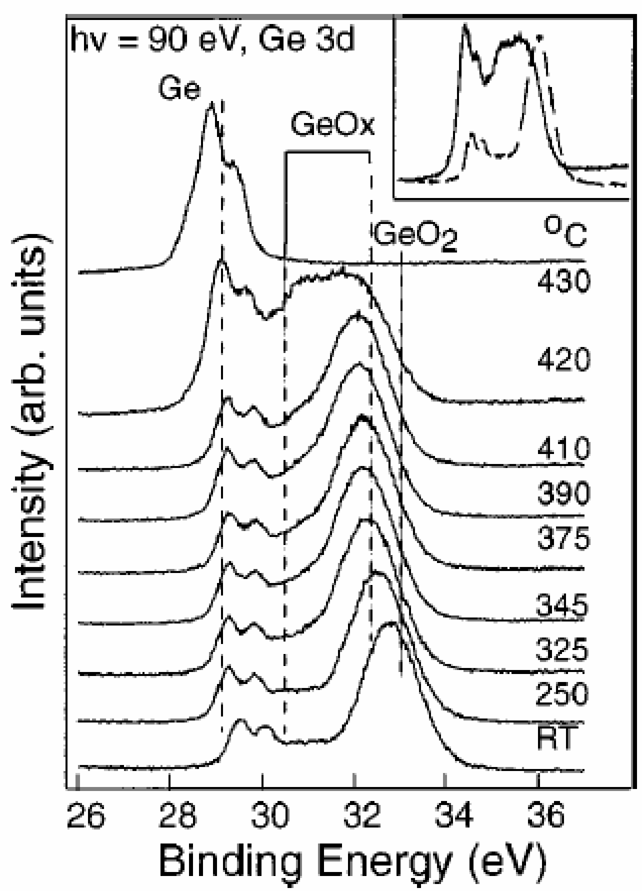
- Lack of thermally stable and high quality gate dielectric (Ge-oxide)

Possibility of better performance results by combining high-*k* gate dielectric and Ge substrate ?

Surface Cleaning and Stability of GeO_x

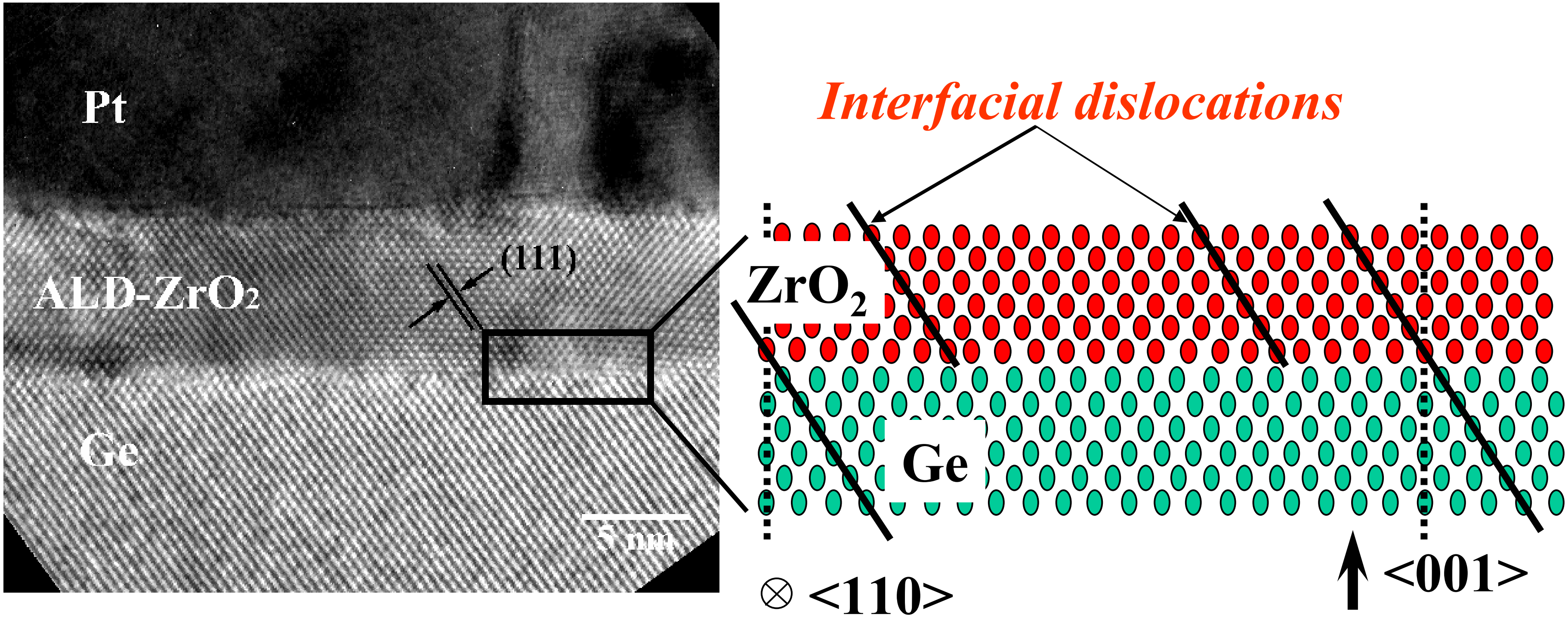


(K. Prabhakaran, *Appl. Phys. Lett*. **76**, 2244 (2000) and *Sur. Sci*. **325**, 263 (1995)



- Common hexagonal phase of GeO_2 is water soluble and volatile
- H_2O removes GeO_2 but not GeO
- GeO_x can be removed in vacuum at temperatures above 430°C

ALD-ZrO_2 on HF-last Ge Substrate

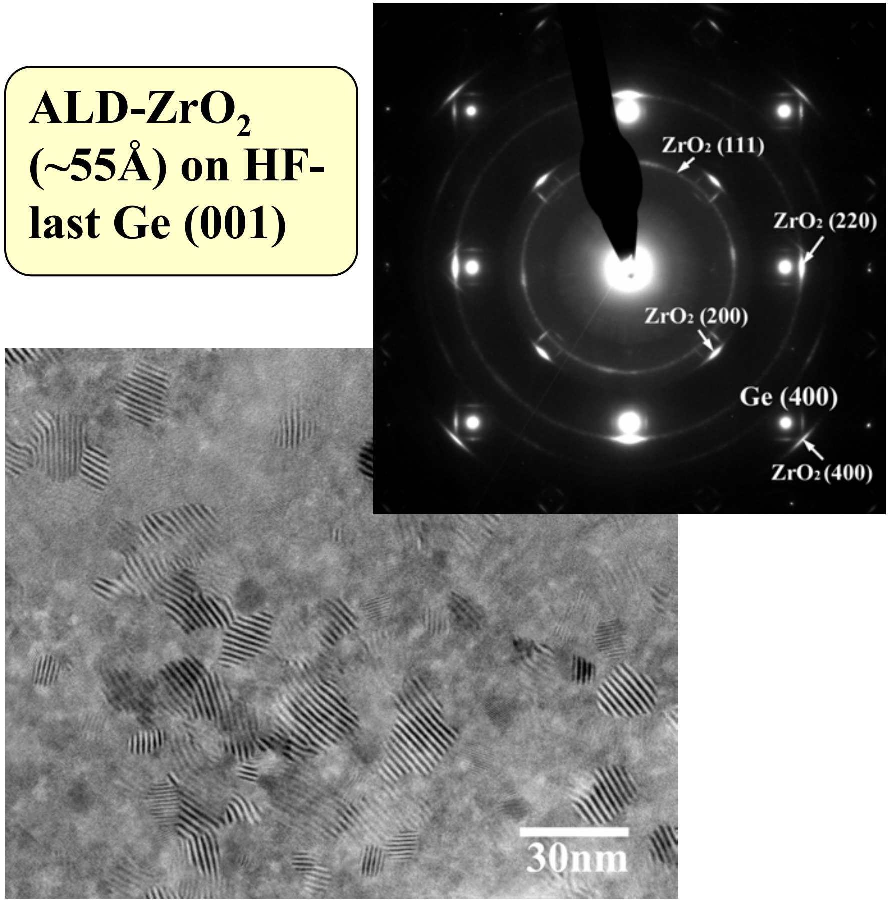


- ALD-ZrO_2 (~55Å) was grown on vapor HF cleaned Ge (100)
- No interfacial layer and local epitaxial growth were observed
- One interfacial dislocation per every 10 (111) planes: matches with lattice mismatch between ZrO_2 and Ge (~10 %).

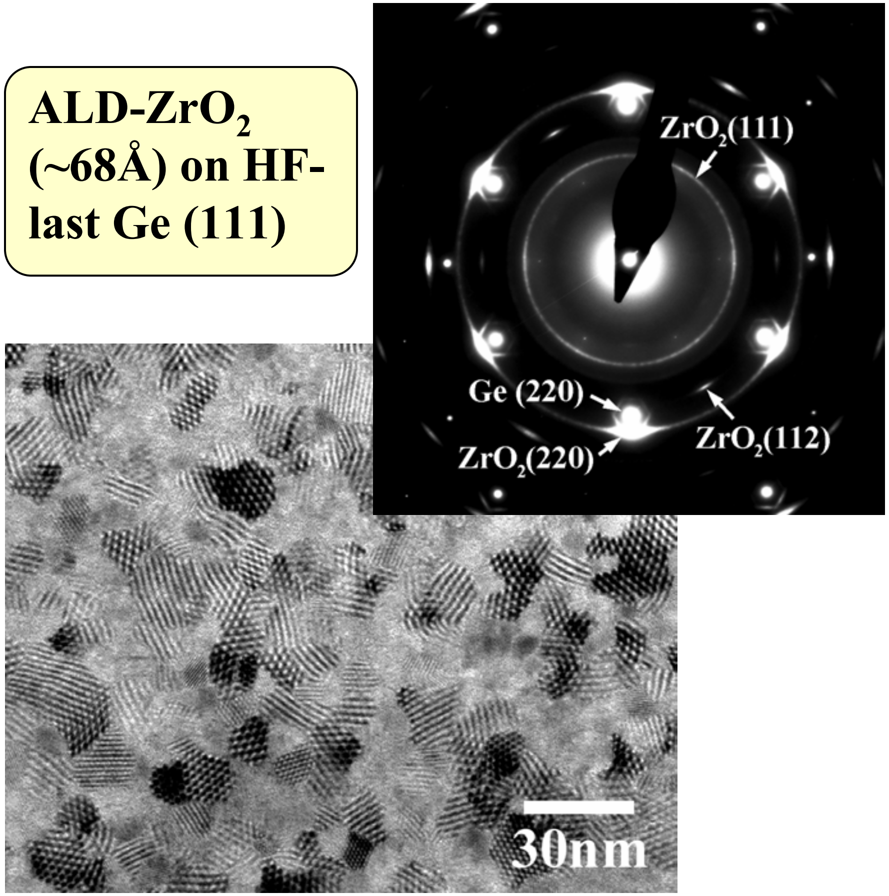
a(tet-ZrO_2)=5.07Å, a(Ge)=5.657Å

Epitaxial Relationship between ZrO_2 and Ge

ALD-ZrO_2 (~55Å) on HF-last Ge (001)



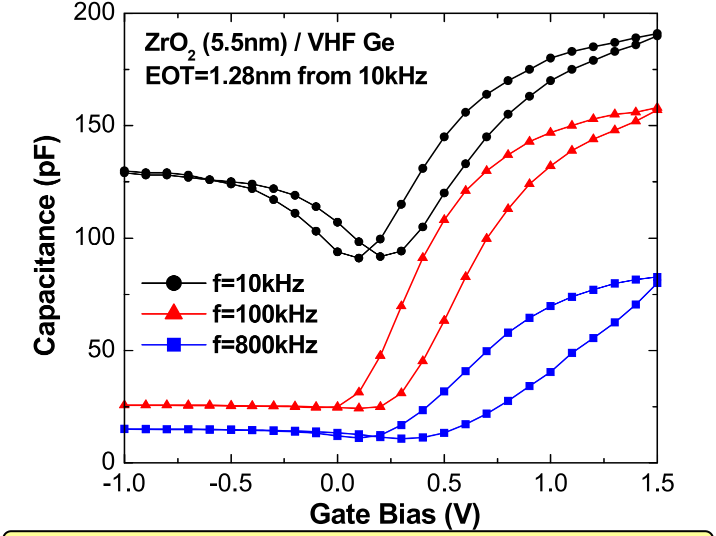
ALD-ZrO_2 (~68Å) on HF-last Ge (111)



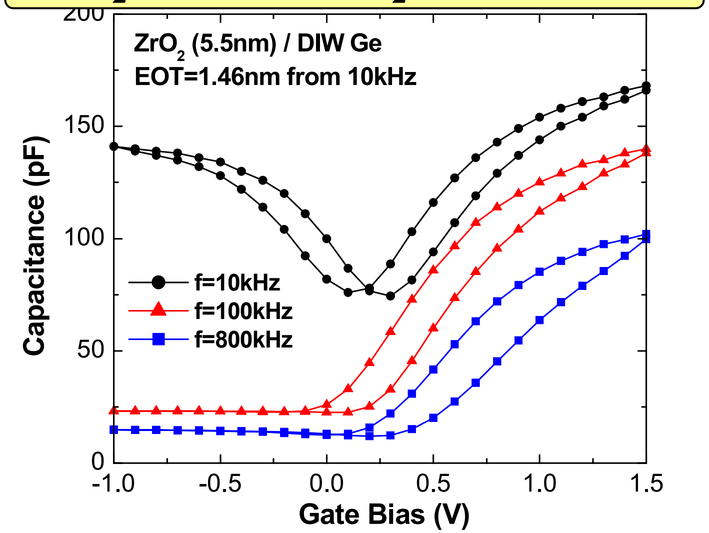
- **Majority of film has the epitaxial orientation relationship (001) [100] ZrO_2 // (001) [100] Ge, (111) [111] ZrO_2 // (111) [111] Ge ; also a polycrystalline component**
- **Tetragonal or cubic phase (ALD-ZrO_2 on Si is tetragonal)**

C-V Charactersitics of ALD-ZrO_2 on Ge

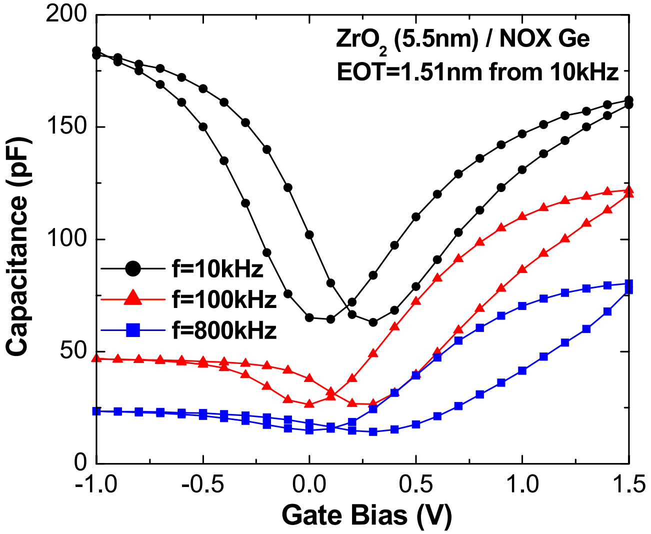
ZrO_2 (~55Å) on HF-cleaned Ge



ZrO_2 (~55Å) on H_2O-cleaned Ge

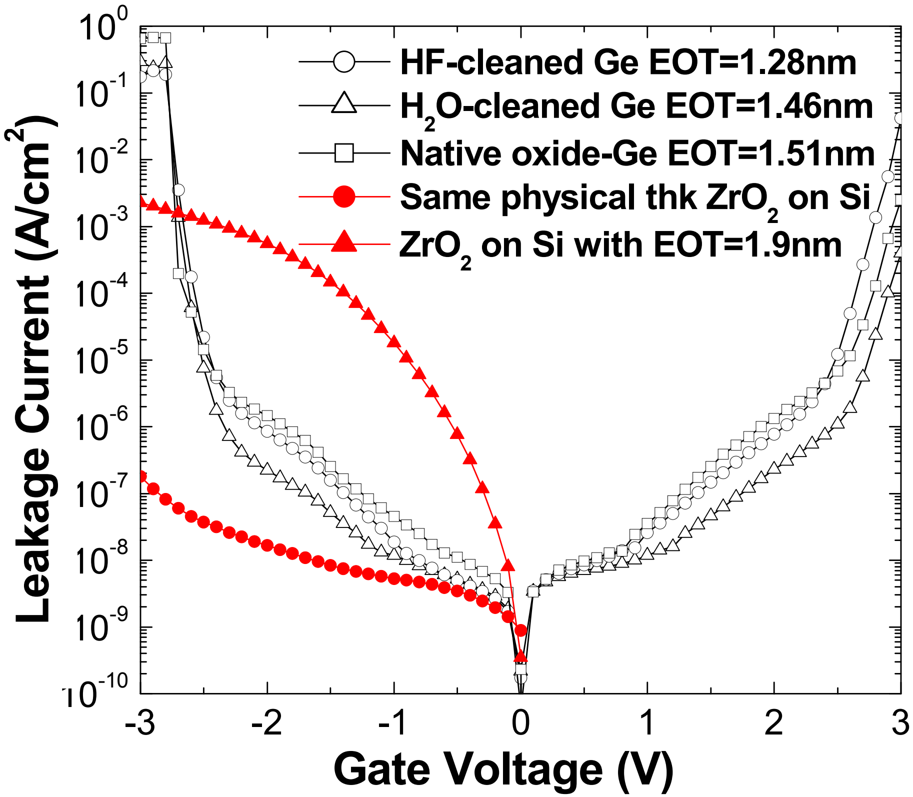


ZrO_2 (~55Å) on native oxide Ge



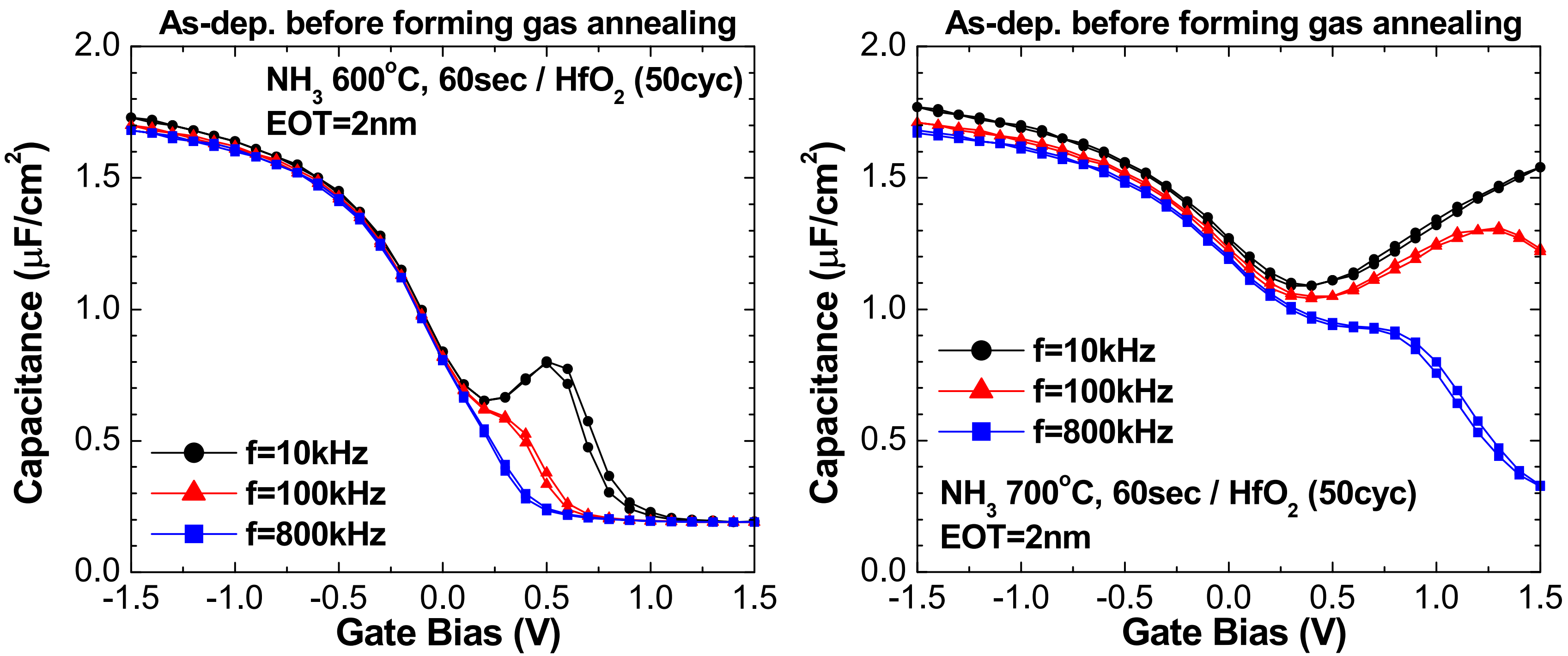
- High dissipation factor and frequency dispersion inhibit obtaining accurate EOT.
- EOT was approximated from 10kHz CV data due to the high frequency dispersion.
- Large hysteresis and frequency dispersion due to high defect density.
- Increase of inversion capacitance may result from the increase of minority carrier generation.

J-V Characteristics of ALD-ZrO_2 on Ge



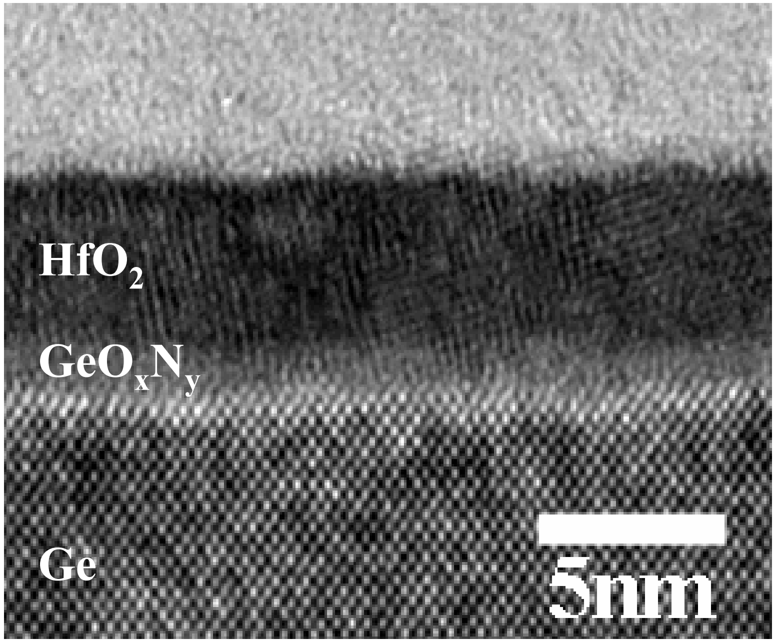
- ZrO_2 on Ge samples show a slightly higher leakage current behavior compared to same physical thickness ZrO_2 on Si.
- Significantly lower leakage current considering the reduced EOT, which results from the absence of a thick dielectric/substrate interfacial oxide layer.
- The breakdown field is quite small (< 5 MV/cm).

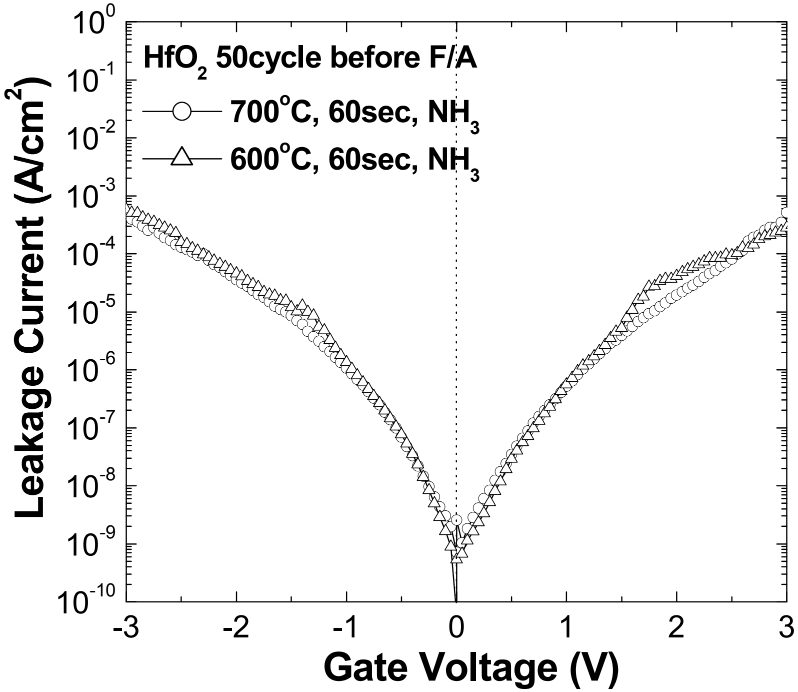
C-V Characteristics of HfO_2/Nitrided Ge



- RTP nitridation : NH_3, 60sec with different temperatures after HF stripping of Ge
- Negligible hysteresis and frequency dispersion.
- The increase of minority carrier generation is efficiently suppressed.
- Excessive nitrogen incorporation increases the density of N-related interface defect states.

J-V and Microstructure of HfO_2/Nitrided Ge



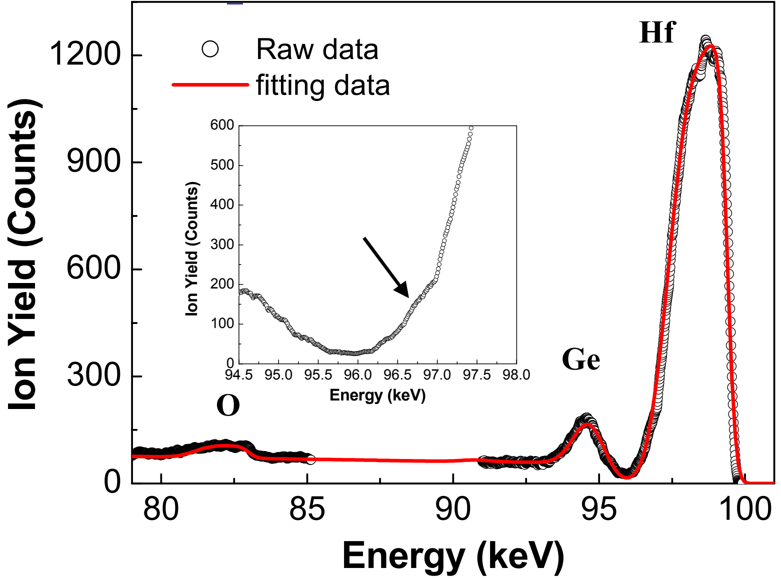


- Nitridation formed a thin (11 ~ 12 Å) interfacial oxide (GeO_xN_y).
- Smooth and uniform growth of ALD-HfO_2 on a nitrided Ge.
- Nitridation temperature does not have an effect on the leakage current.
- Leakage current density is similar with the HfO_2/Si gate stack at the same EOT.

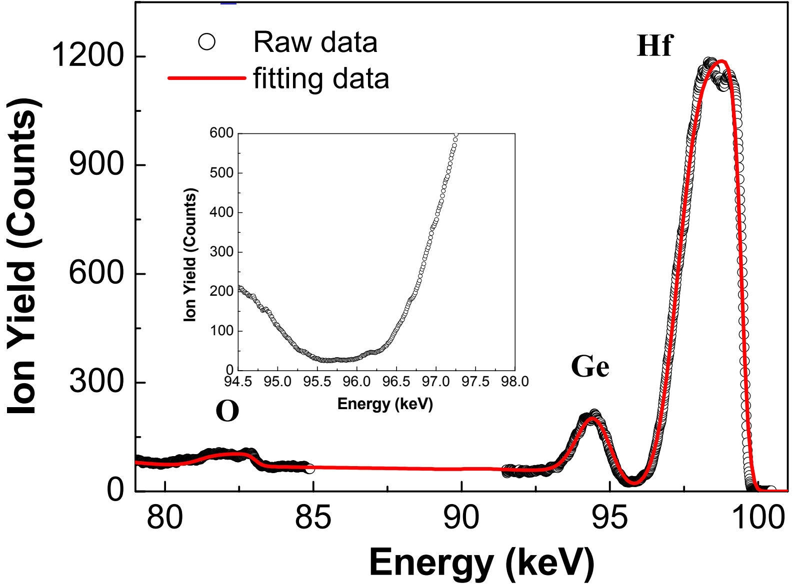
MEIS Analysis of ALD-HfO$_2$ on Nitrided Ge

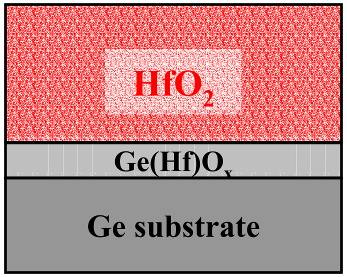
MEIS : collaboration with Dr. Mann-Ho Cho (KRISS)

HfO$_2$ (4 nm)/chemical oxide/Ge



HfO$_2$ (4 nm)/Nitrided Ge (600°C)

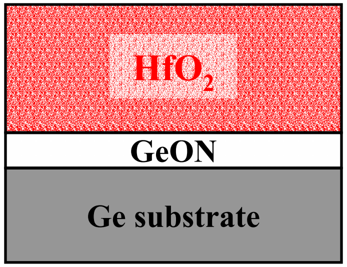




HfO$_2$

Ge(Hf)O$_x$

Ge substrate



HfO$_2$

GeON

Ge substrate

- **Distinctive diffusion of Hf atoms into the substrate interface is seen without a barrier layer (GeO$_x$N$_y$) present.**
- **Interfacial GeO$_x$N$_y$ acts as a diffusion barrier for metal impurities.**

Summary II

- ALD-ZrO_2 on HF-last Ge grows with locally-epitaxial relationship
  - gate dielectric/substrate interface appears nearly atomically-abrupt
  - (001)/<100> ZrO_2 // (001)/<100> Ge and (111)/<111> ZrO_2 // (111)/<111> Ge orientation relationship
  - no observable interfacial oxide was detected using cross-sectional TEM and XPS depth profiling

- Promising electrical properties with ALD-HfO_2 on nitrided Ge
  - HF-cleaning, H_2O-cleaning, chemical oxide consistently show large hysteresis, frequency dispersion, and inversion capacitance increase
  - negligible hysteresis and frequency dispersion are obtained through direct surface nitridation of Ge before high-*k* deposition
  - leakage current is comparable to that of high-*k*/Si
  - interfacial GeO_xN_y layer is acting as a diffusion barrier for metal impurities
  - large amount of nitrogen generates N-related defects at the interface

Conclusions

- A laboratory-scale ALD system using metal chloride and H_2O precursors was built and ZrO_2/HfO_2 deposition processes were optimized.
- Microstructural and electrical properties of ALD-ZrO_2 and HfO_2 on Si were characterized and compared.
- Crystallization kinetics of ALD-HfO_2 and the effects of crystallization on gate stack electrical properties were studied.
- A new interface engineering technique using reactive metal electrodes proved the possibility of controllable removal of dielectric/silicon interface layers.
- High-*k* dielectrics were applied to Ge substrates and improved the electrical properties when an oxynitride interface layer was present.
- Various other applications of ALD high-*k* films, such as nanolaminates, CNT transistor, Ge-nanowire transistor, and area-selective ALD were demonstrated.