CON-TACT® Planarization - The Future of Advanced Device Planarization

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OUTLINE

- The Need for Planarization
- The CON-TACT Technique
- Application Examples
- Benefits

Why CON-TACT® Planarization?

Today's Issues:

1) **Manufactured device performance and/or process window is limited** by insufficient planarization, resulting in:

- Reduced ability to build additional layers on a device
- Increased interconnect length

2) **Process Cycle Time**: CON-TACT reduces device process time over less-efficient an dirty polishing techniques

3) **Cleanliness**: Unlike polishing techniques, CON-TACT is inherently clean, introducing no new materials.

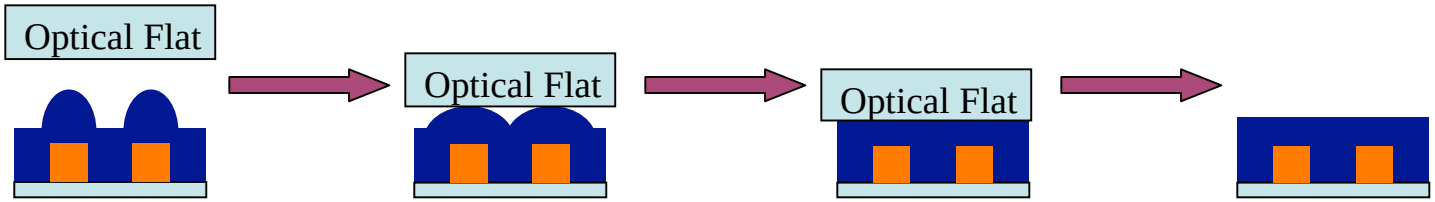
4) **Material Consumption**: CON-TACT's pressing process flows the material where it is needed, reducing "overburden"

Device Manufacturing Issue: The Iso-Dense Thickness Bias Effect

When a material is coated onto a substrate that contains areas with varying feature densities, the film thickness is greater over regions with isolated low areas (iso feature density areas on contact via patterns) than over regions with many low areas (dense feature density areas on contact via wafers). This results in the so called iso-dense thickness bias.

The CON-TACT Process

In the CON-TACT process a planarization material is pressed against an optically flat surface, forcing the material to conform to the surface of the optical flat:



The CON-TACT process can be applied to any material that is flowable at less than 300°C and has been demonstrated for:

- Photo-cured material (photoresists, epoxies)
- Thermoplastic materials (PMMA)
- Thermo-cured (thermo-set) materials (BCB, SOG, ARCs, SU-8)

Applications for CON-TACT Technology

CON-TACT planarization technology has demonstrated the ability to planarize difficult topographies for the fabrication of:

- Inter layer dielectric structures
- MEMS or Photonic structures
- STI structures
- Advanced lithographic structures (ARCs, BARCs)
- Dual Damascene structures

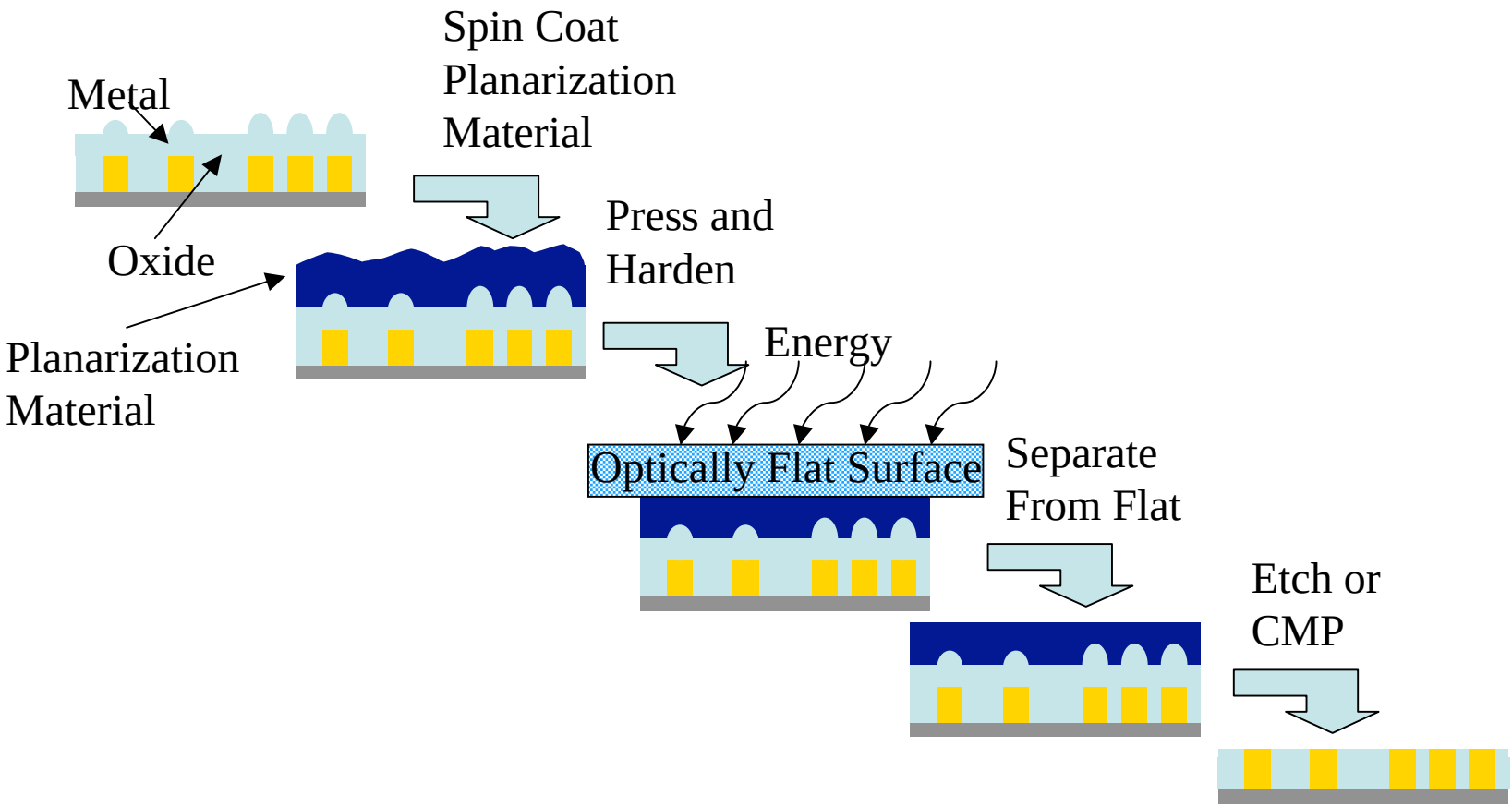
CON-TACT Planarization Options

- Sacrificial Layer
  - CMP
  - Etchback
- Leave-on Applications
  - Passivation
  - Interlayer Dielectric
  - BARC

Use of CON-TACT With a Sacrificial Planarization Material

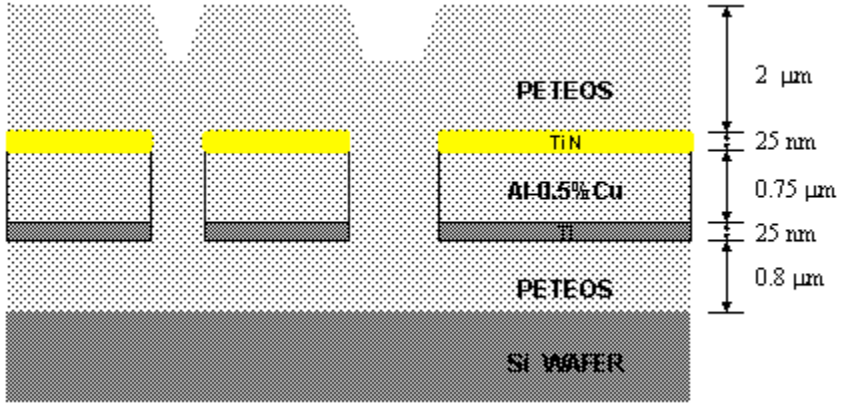
- Process flow chart
- Planarization results
  - DOP
  - WID
  - WIW

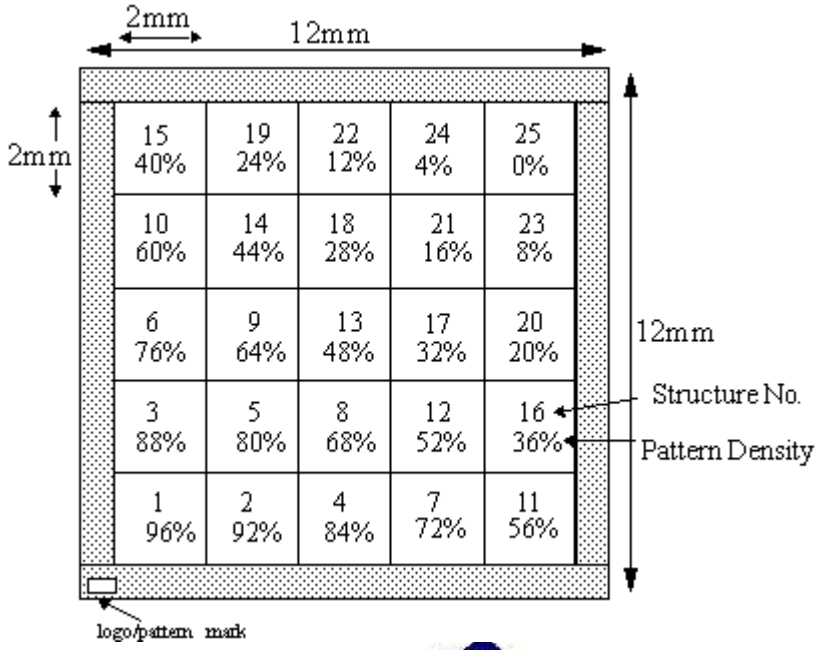
Sacrificial Layer Process Flow



Wafers for Planarization Performance Testing

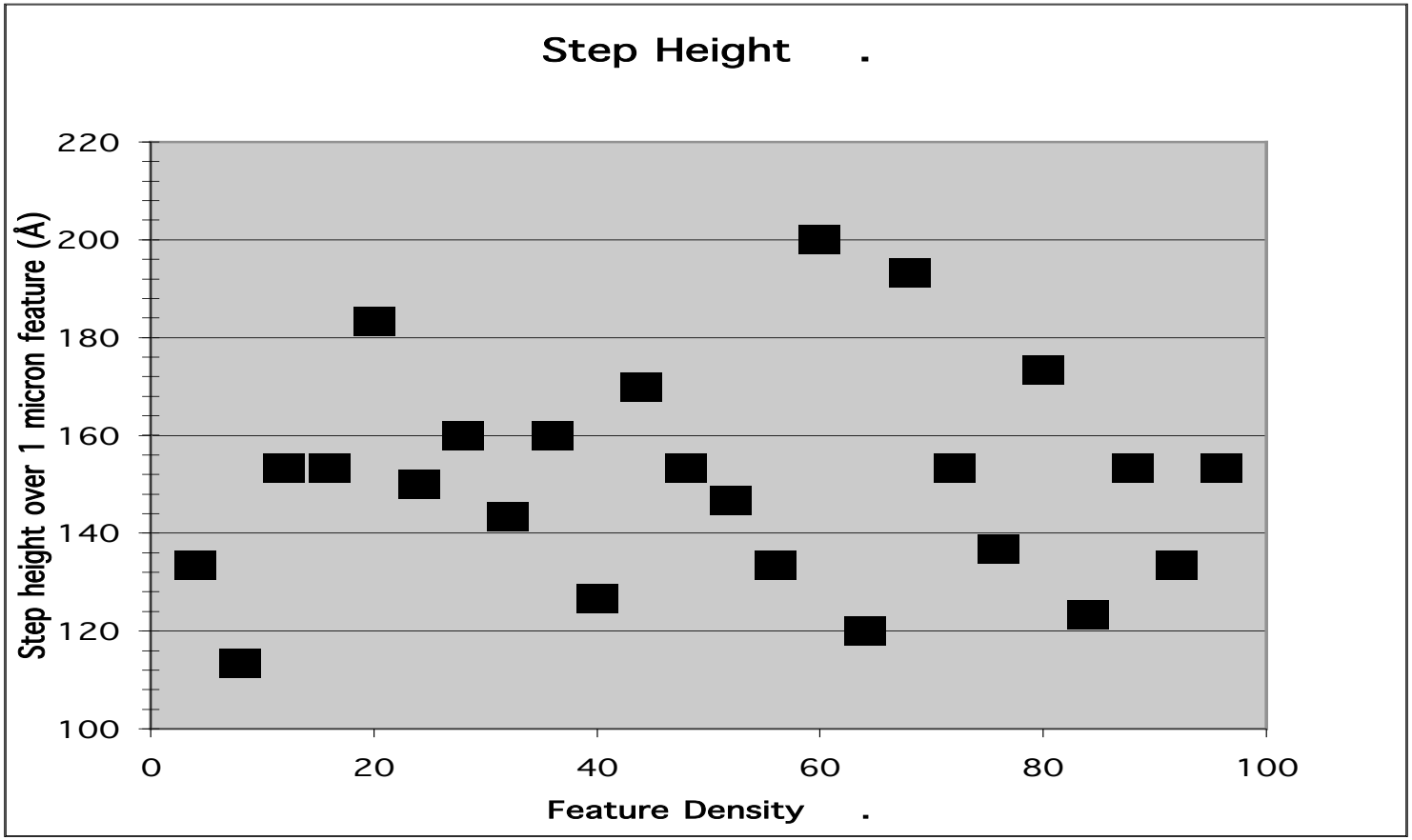
- SKW 1-1 Dielectric Oxide CMP
  - 150mm Wafers, Die size 12mm x 12mm
  - 250um pitch with line density from 0% to 96%
  - 1µm topography





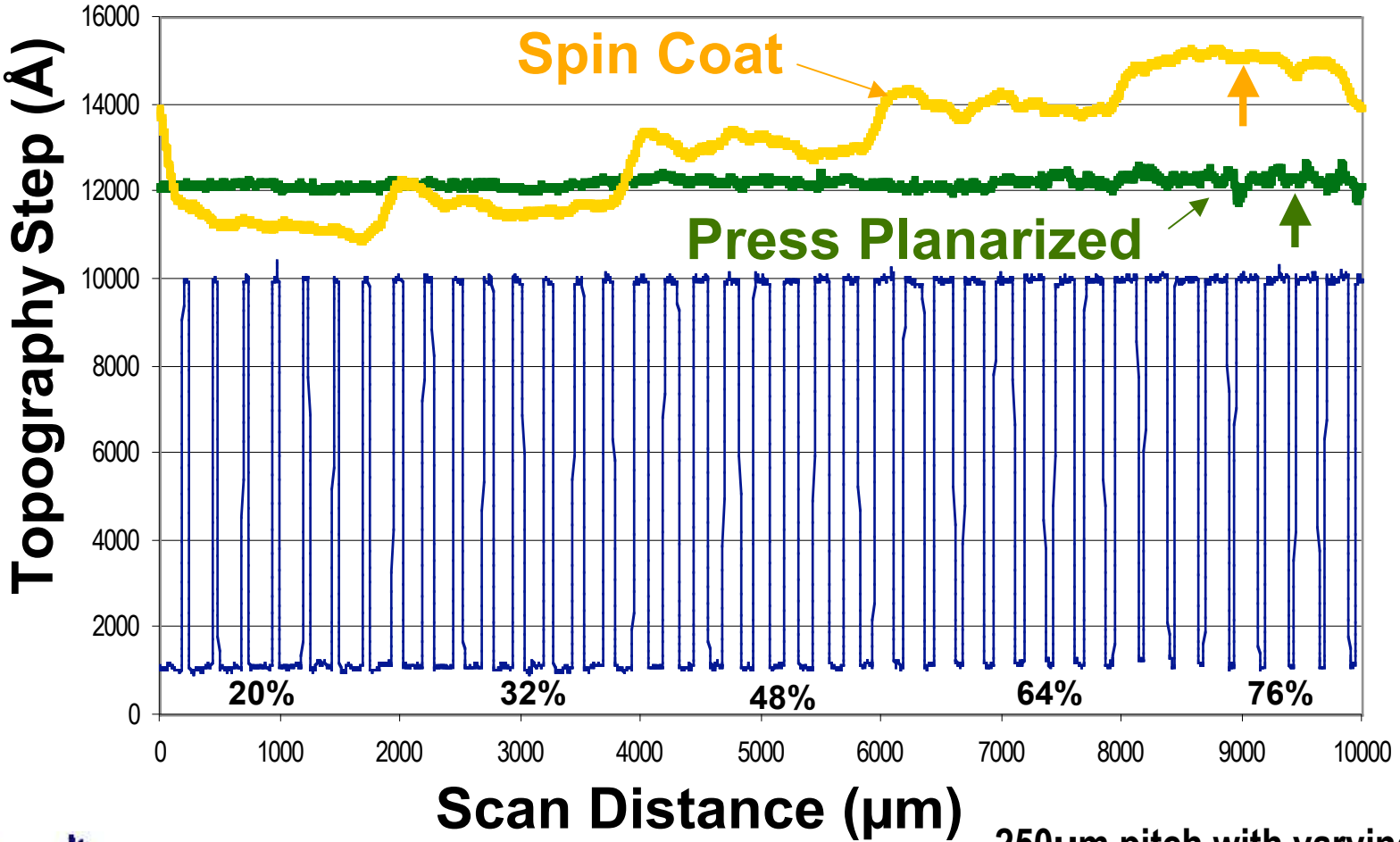
Courtesy of SKW Assoc. www.testwafer.com

Surface Planarity (DOP) of CP



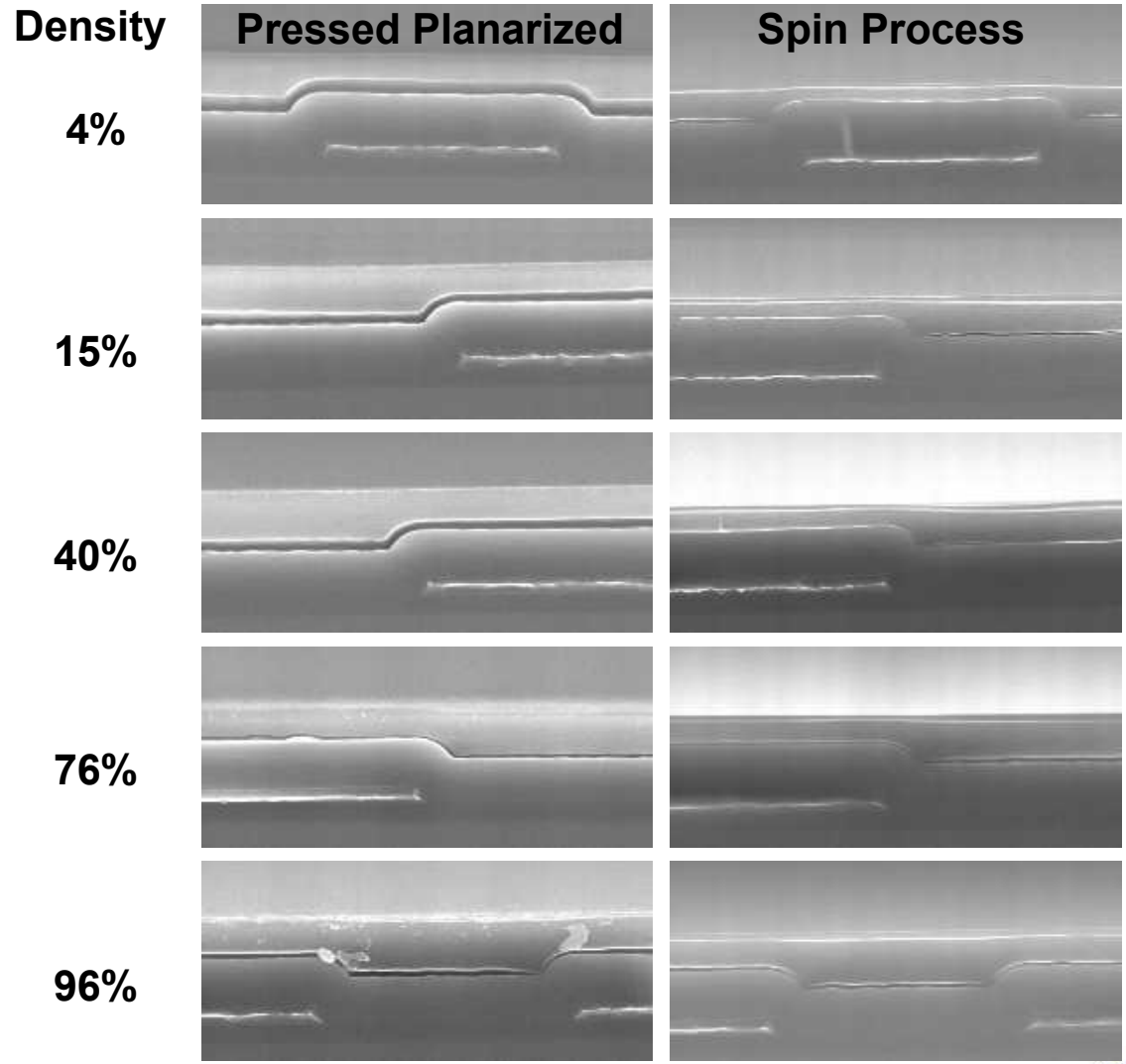
DOP = >98%

Planarization Performance



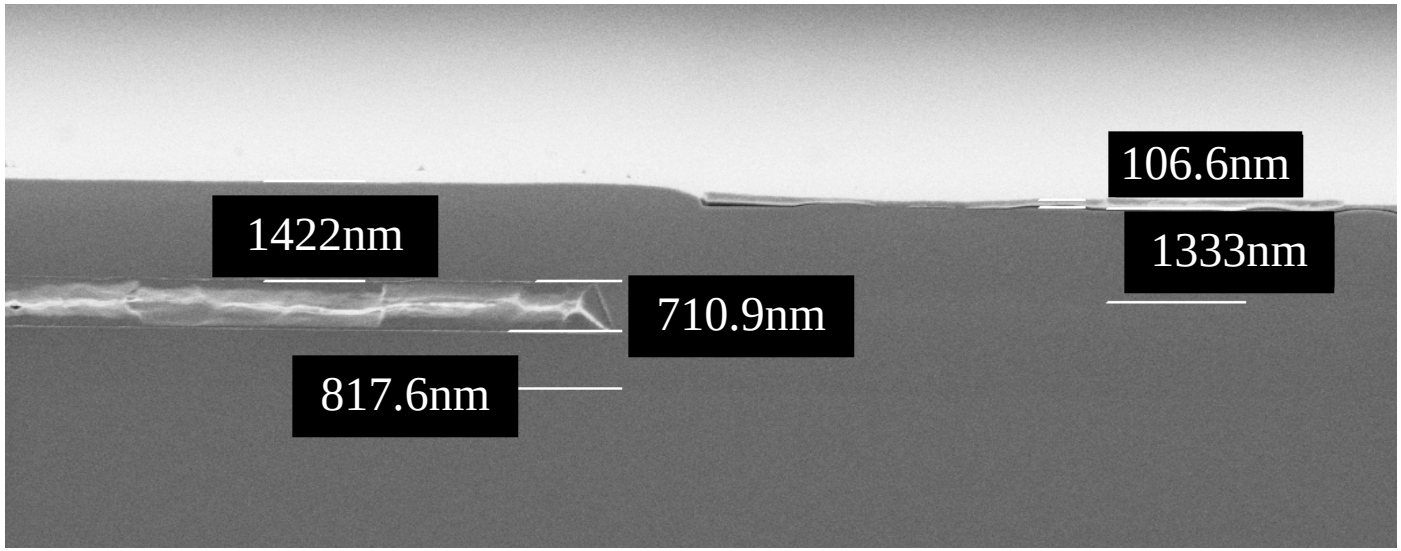
250µm pitch with varying density

Planarization Performance



Post Sacrificial Material Etch

A 1000nm Step Height is reduced to 17.6nm resulting in a post-etch DOP of 98%



Oxide thickness above a feature + metal thickness + Oxide below the metal = 2950.5 nm

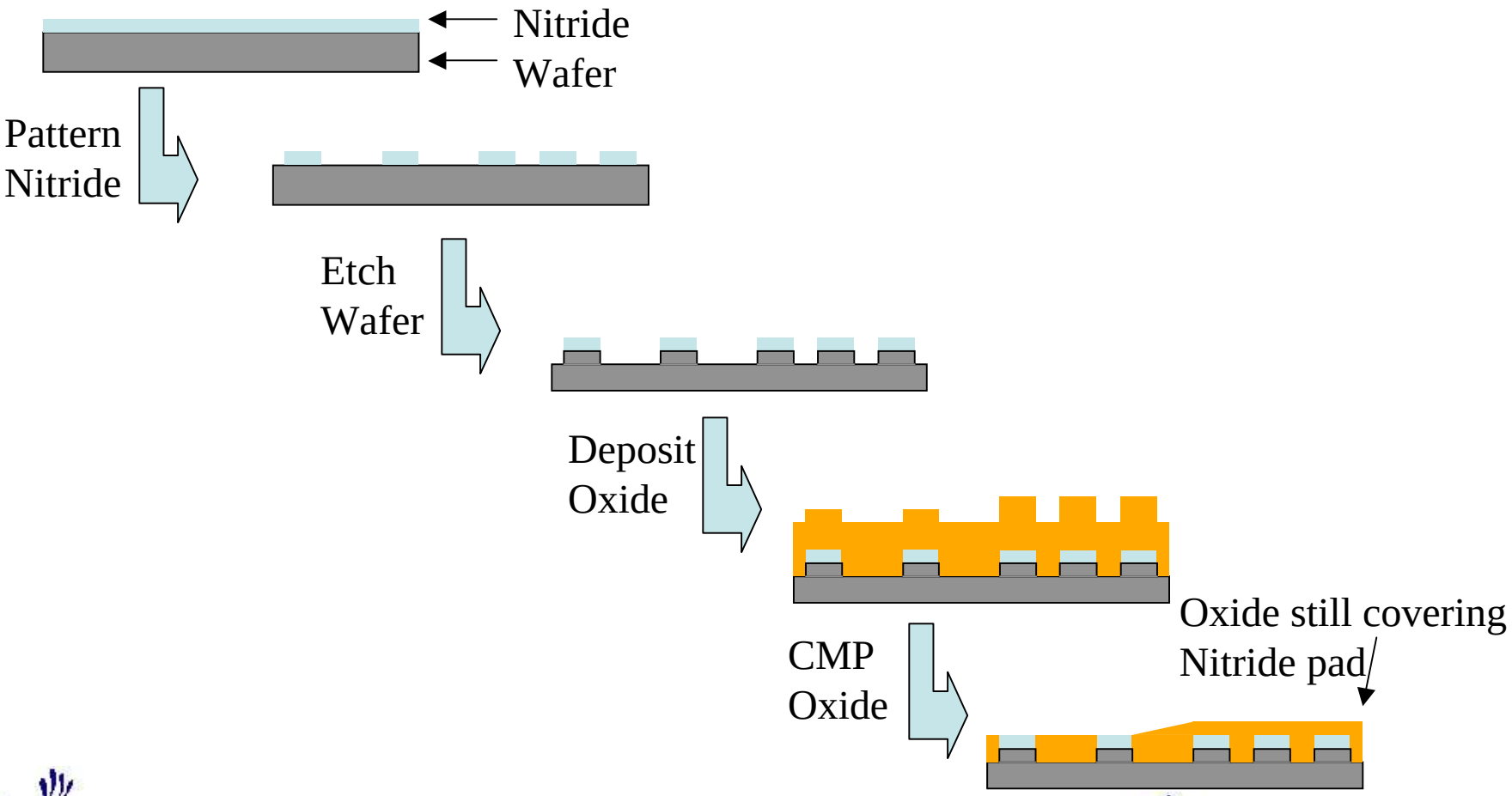
Oxide thickness in trench + Remaining sacrificial oxide = 2968.1 nm

Remaining oxide step height = 17.6nm

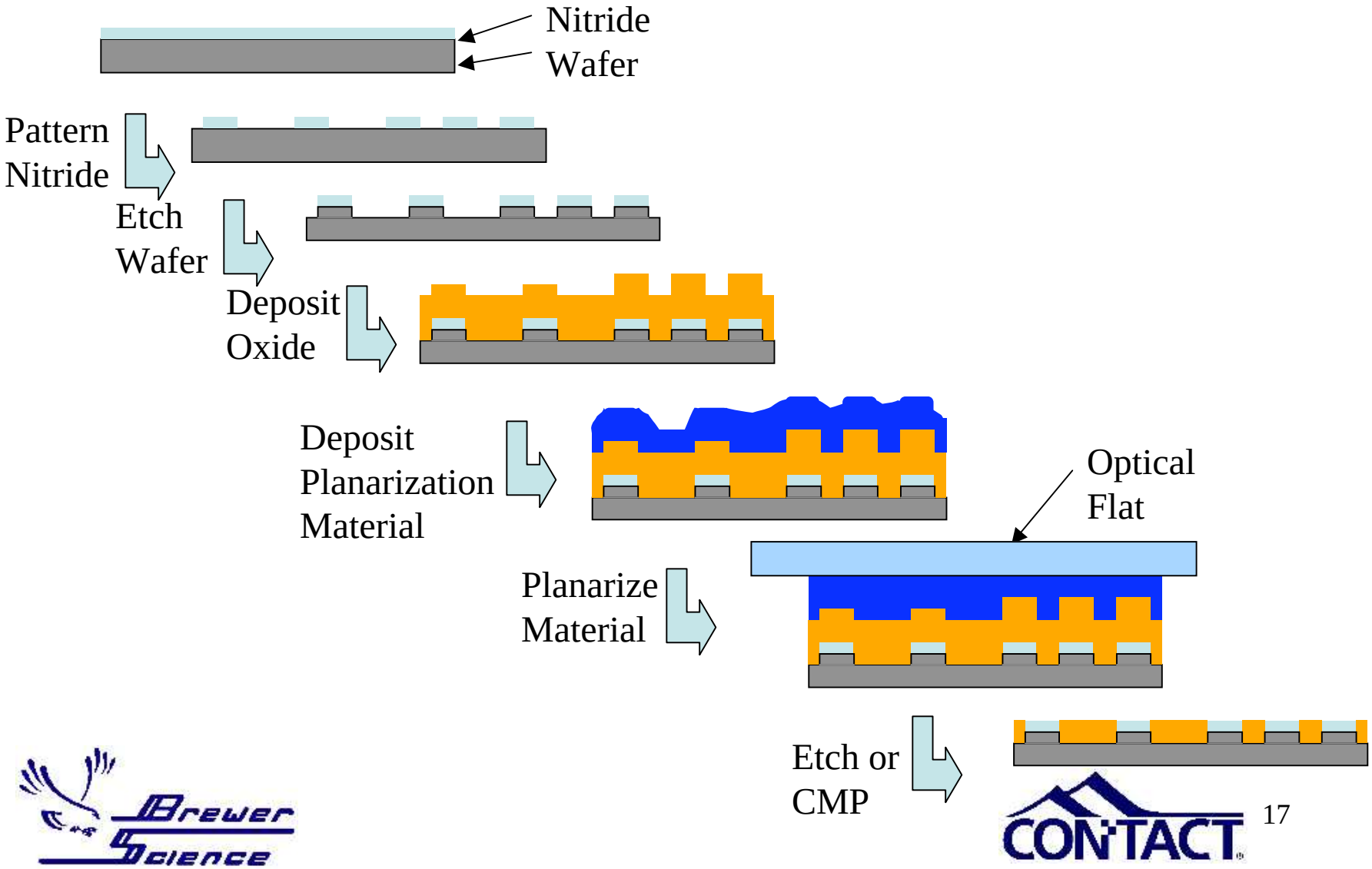
STI Applications for Sacrificial CON-TACT

- Process flow chart
  - Sacrificial Application
  - Conventional vs. Sacrificial CON-TACT
- Planarization results
  - Step height reduction

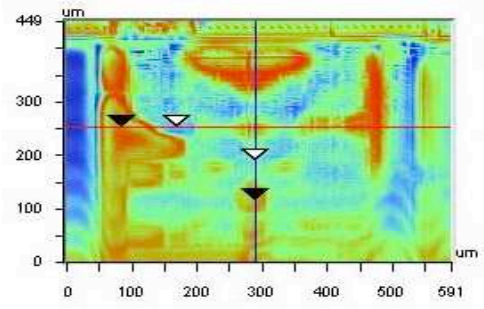
CMP Process Flow for STI Applications



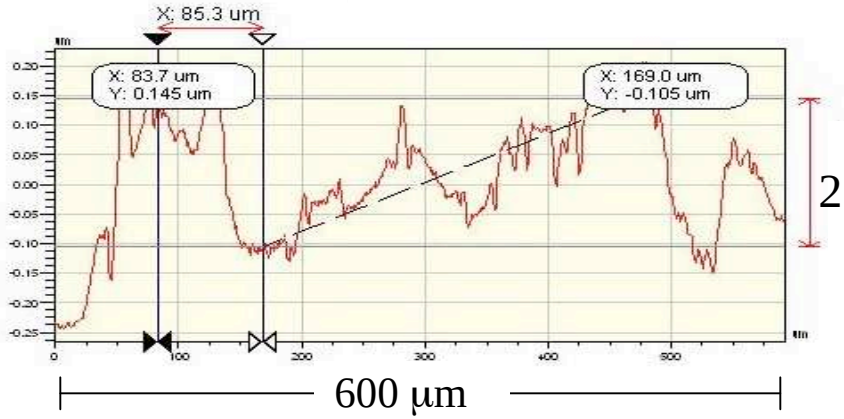
CON-TACT Process Flow for STI Applications



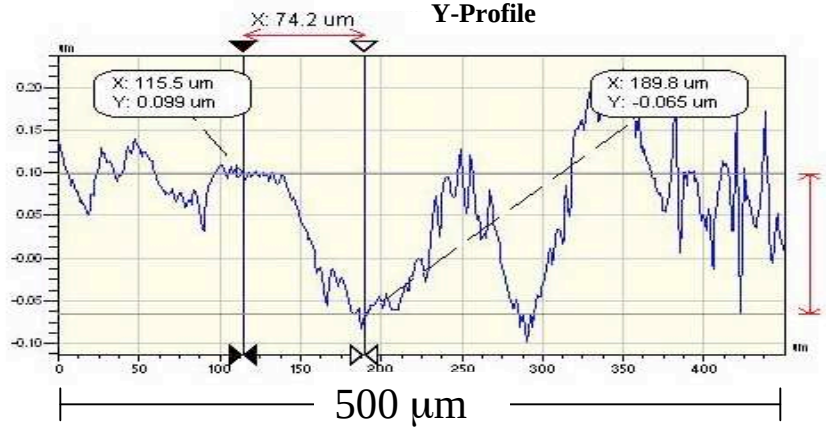
STI DRAM Planarization Performance - Spin Coat



X-Profile



Y-Profile



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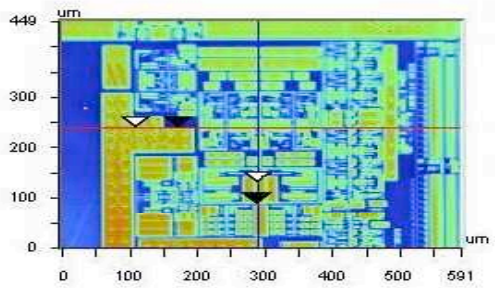
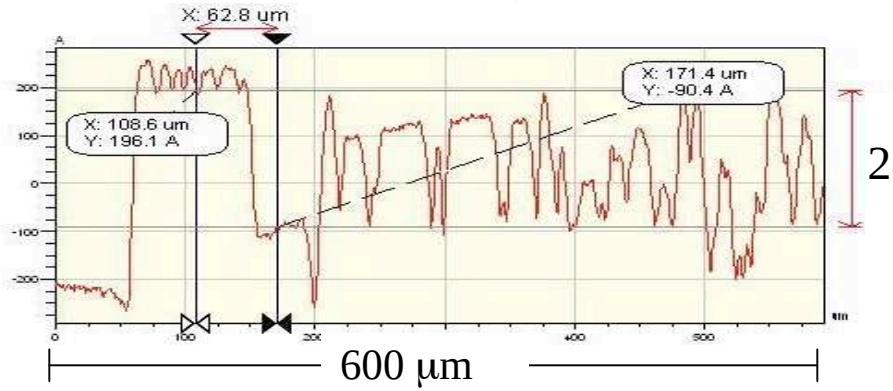
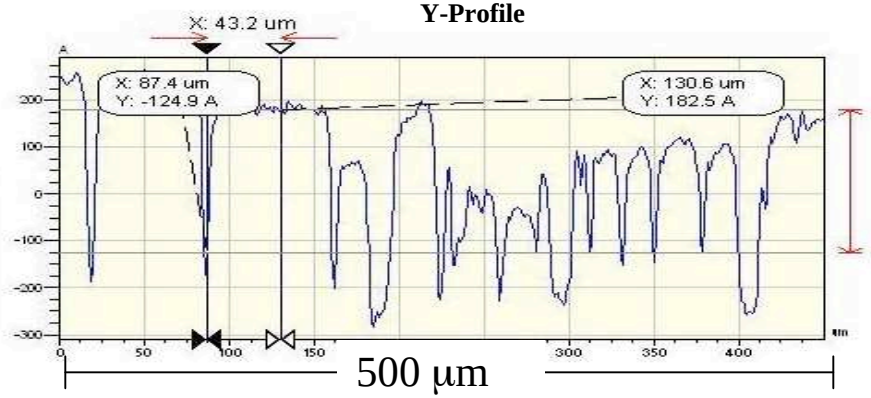
STI DRAM Planarization Performance - Pressed



X-Profile



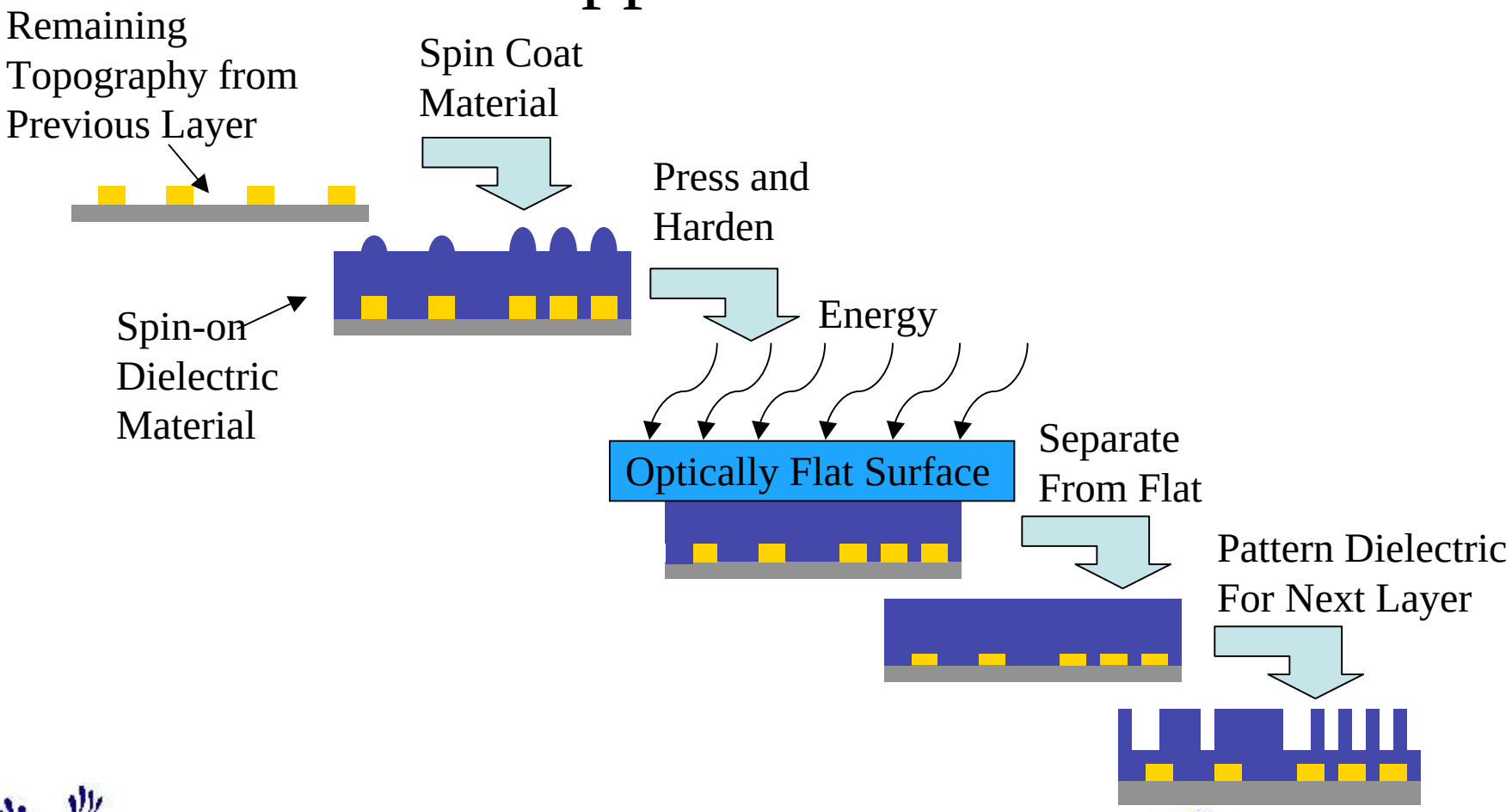
Y-Profile



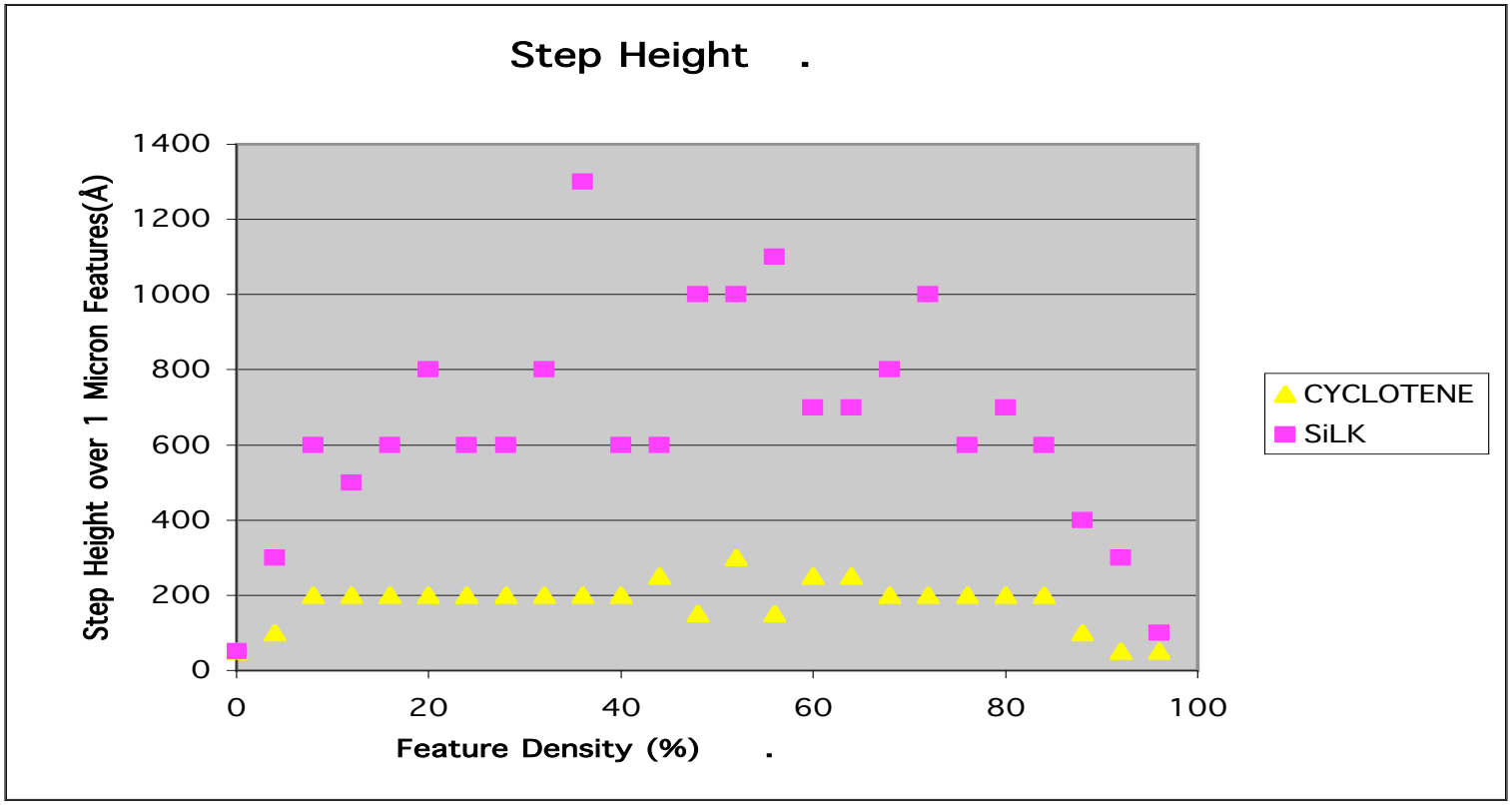
Use of CON-TACT Planarization in Leave on Applications

- Process flow chart
- Planarization results
  - DOP
  - Reduction of feature density dependency

CON-TACT Process Flow for Leave-On Applications



Surface Planarity (DOP) of CP

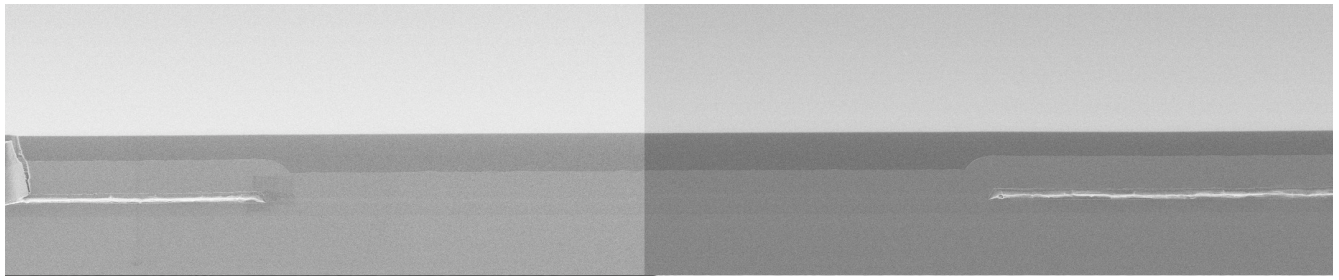


DOP CYCLOTENE® Resin = >98%

DOP SiLK ® Resin = >93%

Film Thickness Uniformity

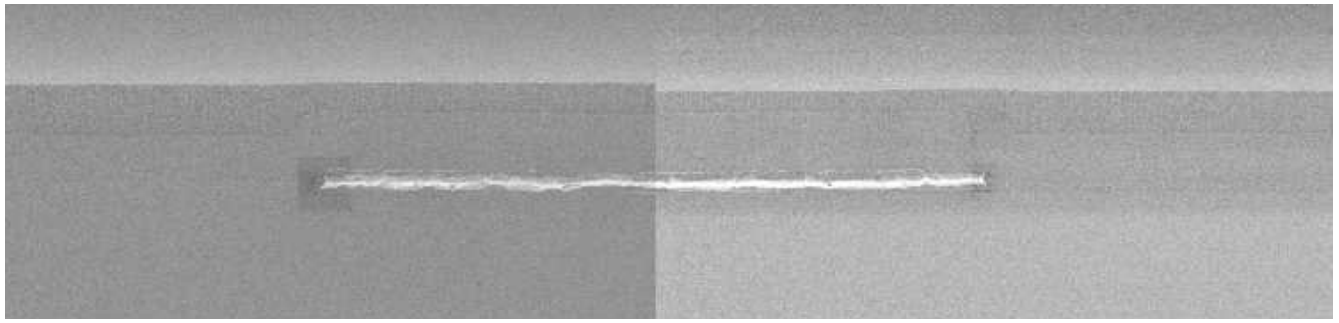
High Density Area



Low Density Area

Pressed CYCLOTENE Resin on SKW-CMP Wafer

High Density Area



Low Density Area

Unpressed CYCLOTENE Resin on SKW-CMP Wafer

* High and low feature density areas represent a difference of 48% feature density

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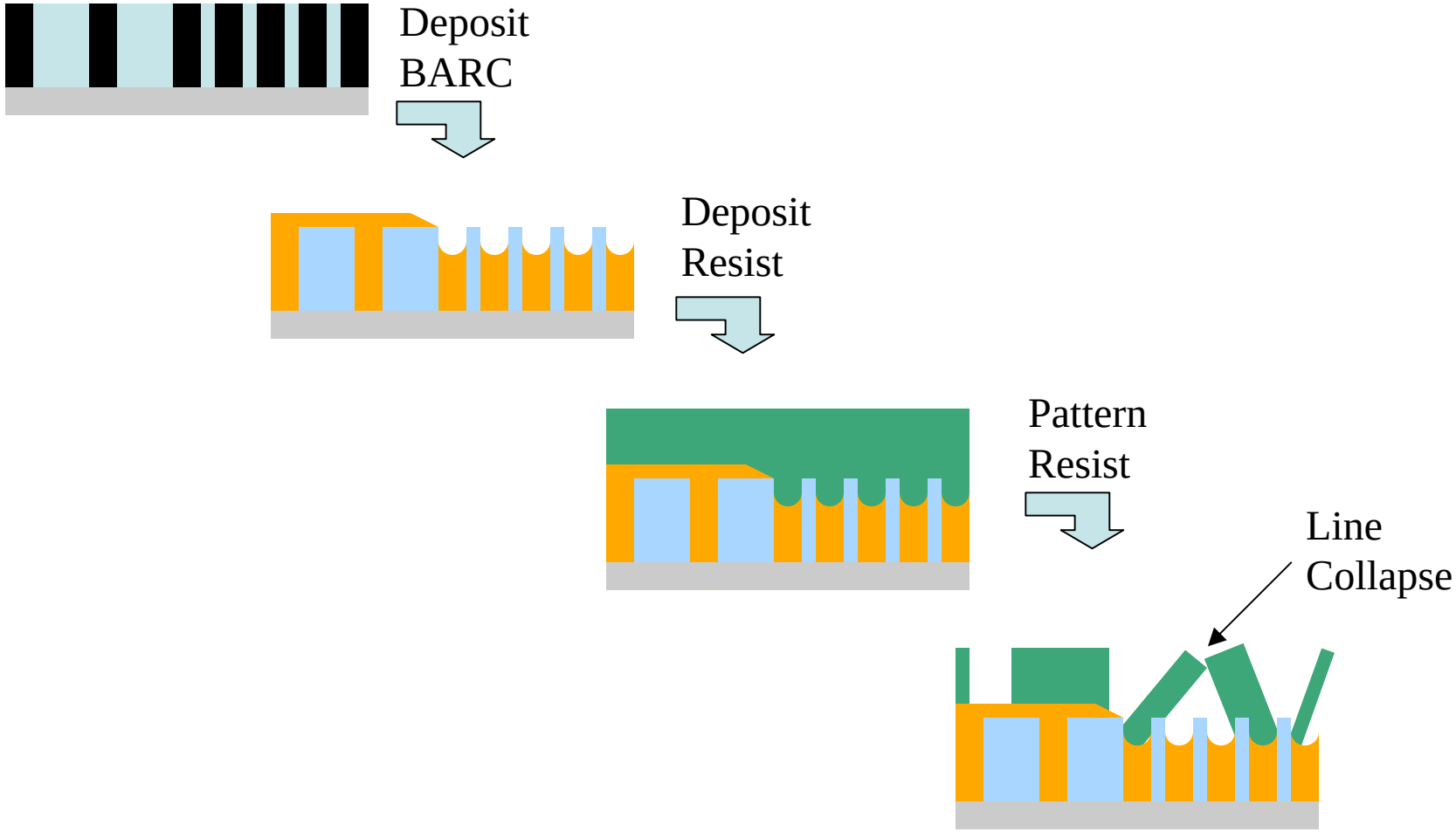
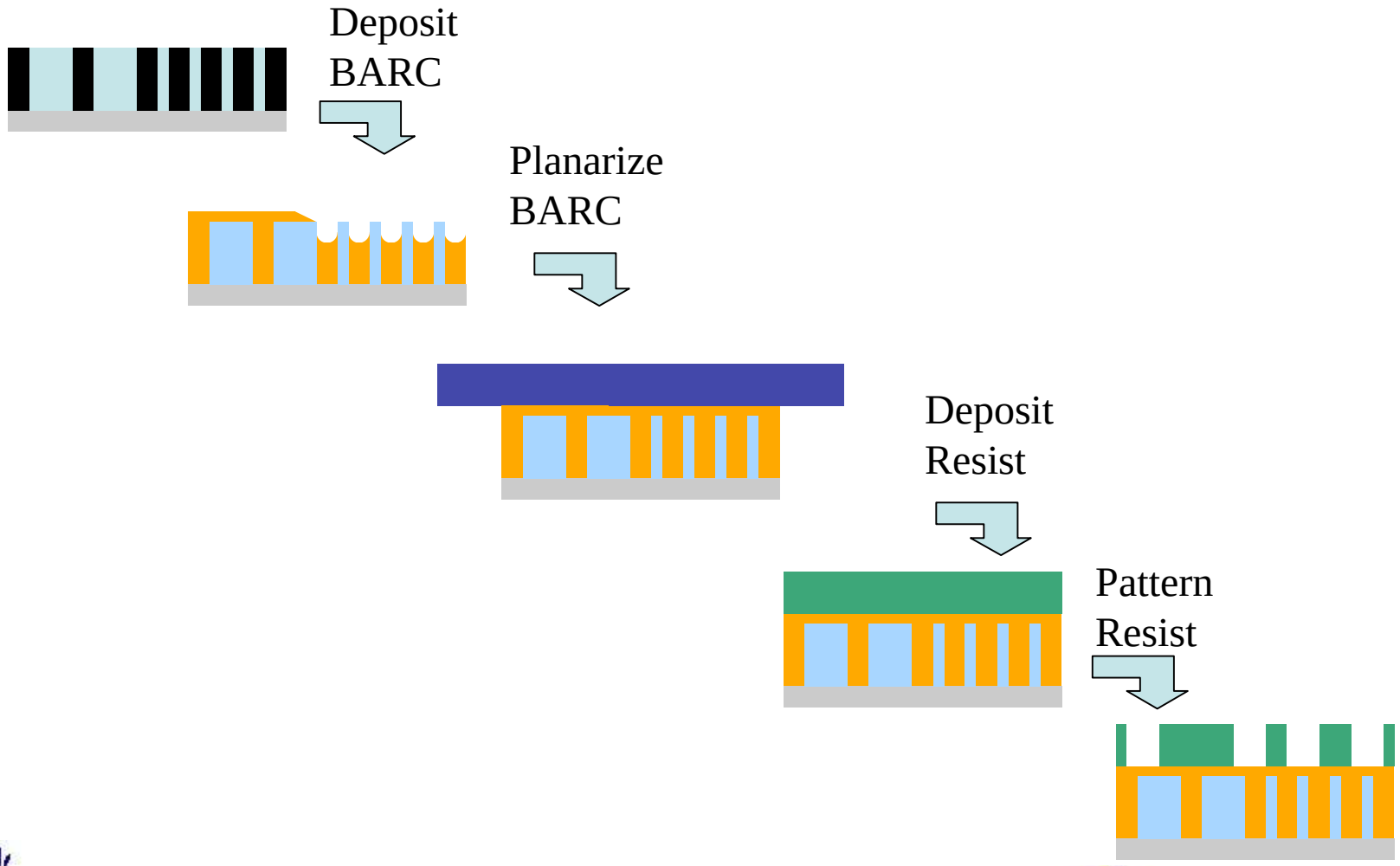
CON-TACT for Advanced Lithography Applications

- Process flow chart
  - Leave-on Planarization
  - Conventional vs. CON-TACT
- Planarization results
  - Removal of iso-dense bias
  - Photolithography results
- Benefit of removing iso-dense bias

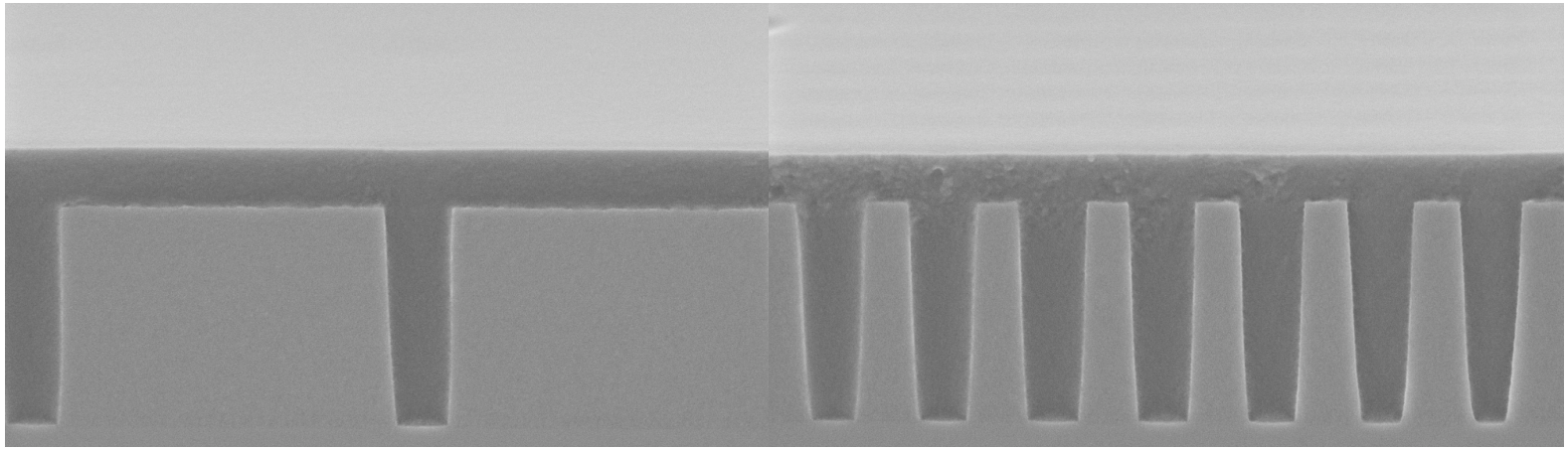
Current Photolithography Process



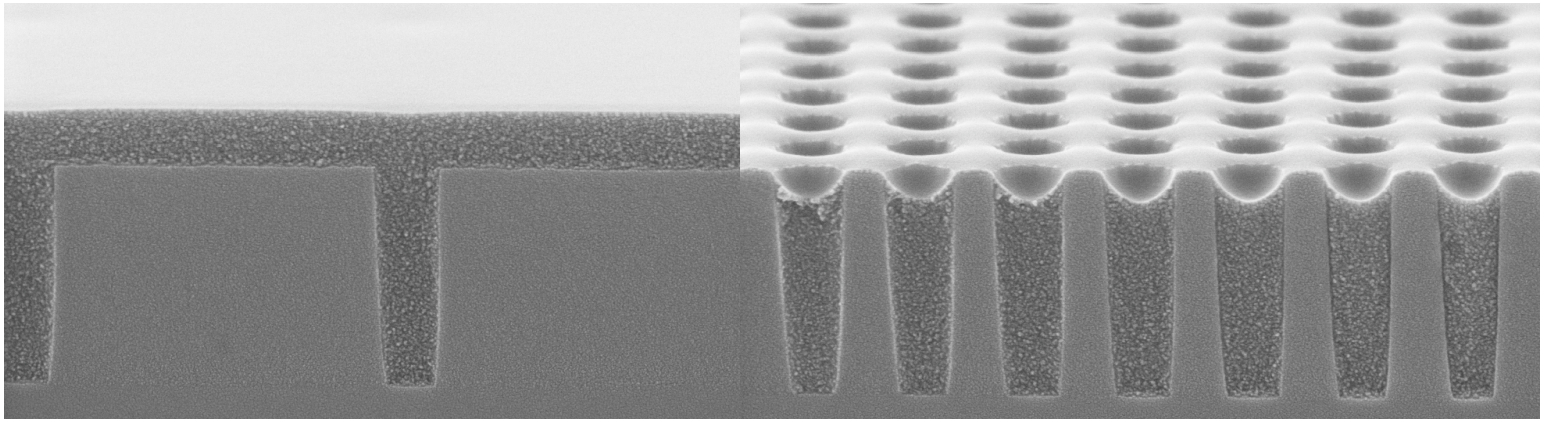
CP Improved Photolithography Process



Removal of Iso-Dense Bias

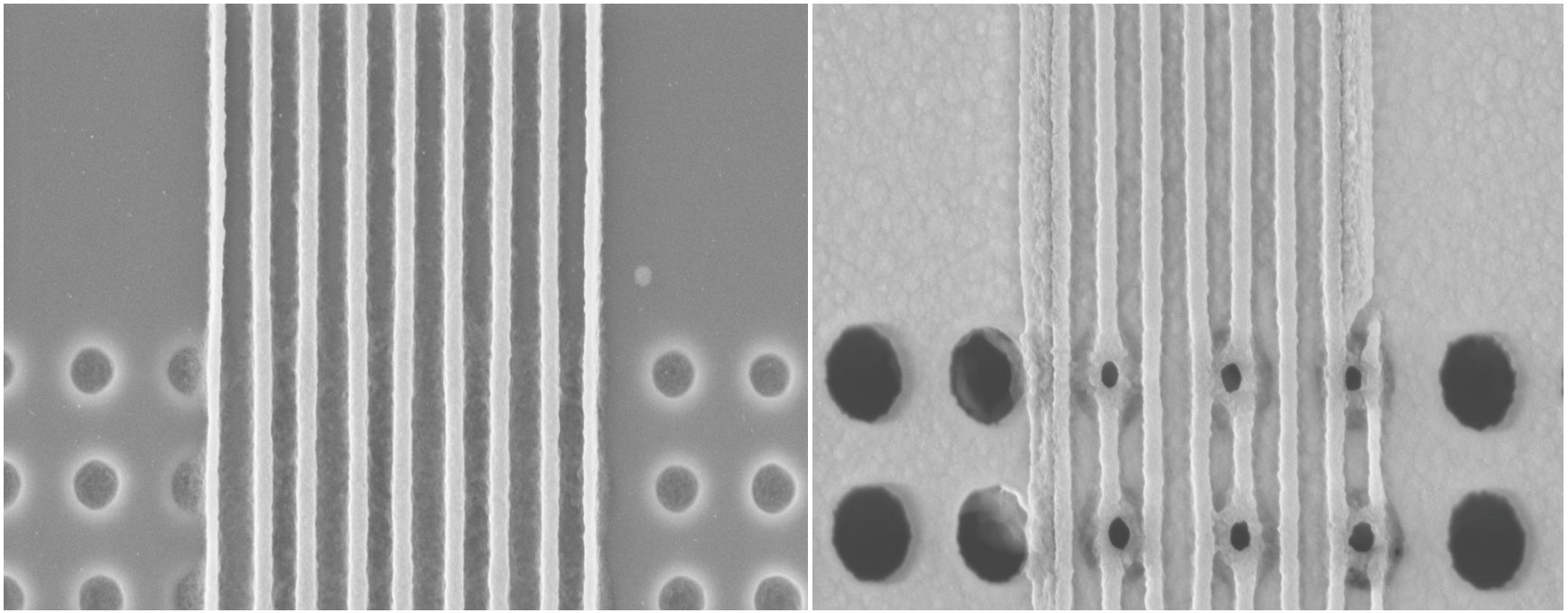


Pressed Iso-Dense Bias of BARC Material on Contact Vias



Un-Pressed Iso-Dense Bias of BARC Material on Contact Vias

CP Improvements in Photolithography



A) B)

Lines printed over vias filled with A) pressed BARC and B) Unpressed BARC

Benefit of Removing Iso-Dense Bias

- Improved local and global planarization performance
- Improved Depth of Focus (DOF) for additional photolithography processes
- Reduced film thickness requirements for BARC layers.
- Enable advanced processing techniques

CON-TACT Successes

- Planarized CYCLOTENE and SiLK resins to 98% DOP and 93% DOP respectively while greatly reducing the feature density dependency
- Planarized a sacrificial material to 98% DOP while achieving less than 3% for both WIWNU and WIDNU
- Transferred the high degree of planarity of the sacrificial material to the dielectric layer via etch

CON-TACT Successes

- Reduced the step height of a sacrificial planarization material coated over STI-DRAM structures by a factor of 10, to approximately 200Å
- Reduced the Iso-Dense Bias effect of BARC coated over contact via wafers making advanced lithography steps possible
- Reduced expected CoO by as much as 58% over CMP technology

The Machine

QUESTIONS?

Contact Julie Snook

Applications Engineer

Brewer Science, Rolla, Missouri

(573) 364-0300

jamsnook@brewerscience.com