Methodology for environmental impact evaluation - 2D vs 3D case study

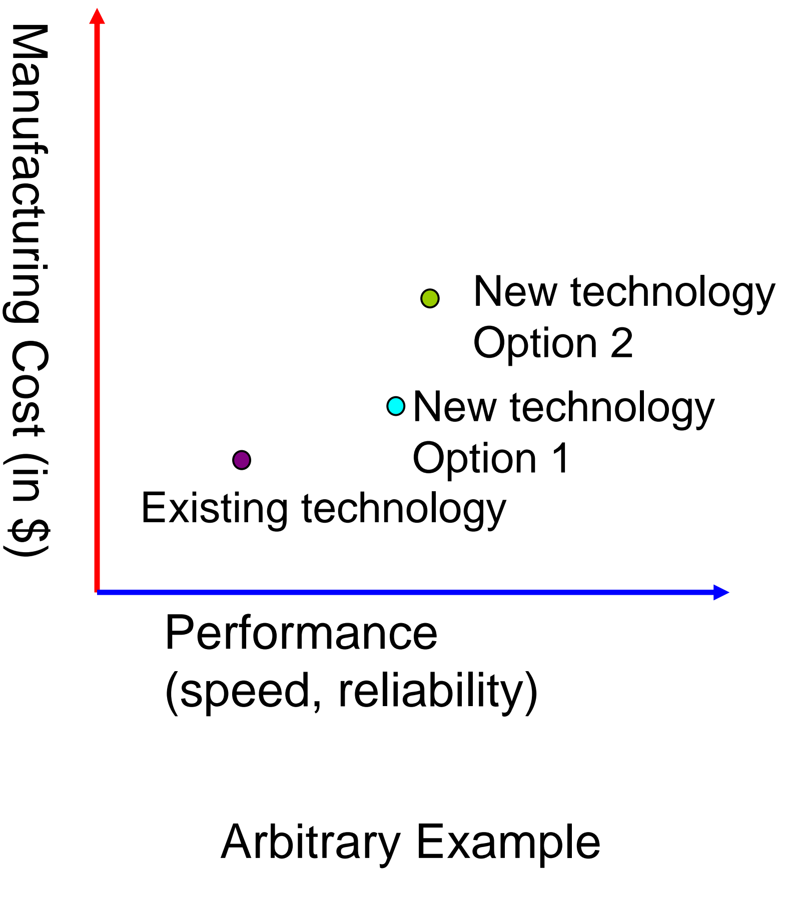
ERC Teleseminar
12/01/2005

Ajay Somani, Duane Boning and Rafael Reif
Microsystems Technology Laboratories, MIT

Outline

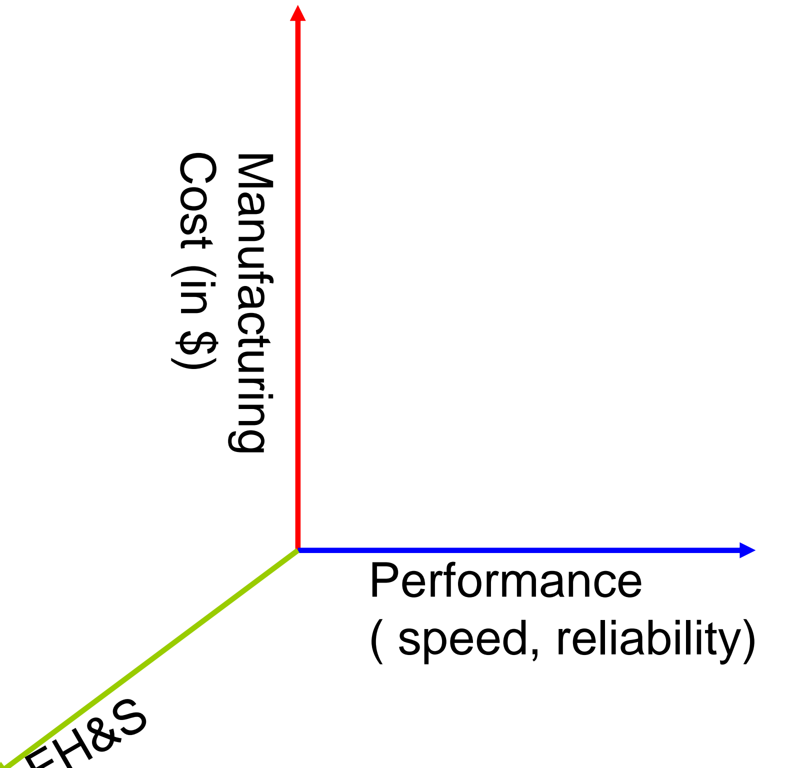
- **Motivation for Methodology and Model**
- Defining objectives of project
- Our Approach/Methodology
  - Brief description
  - Generating environmental footprint for standard CMOS logic device
- Case Study 2D v. 3D
  - Why 3D? (Benefits)
  - Describing different options
  - MIT 3D's process flow
  - Comparison and preliminary conclusions
  - Designing Handle Wafer
- Conclusion and Future Work

Motivation for Methodology



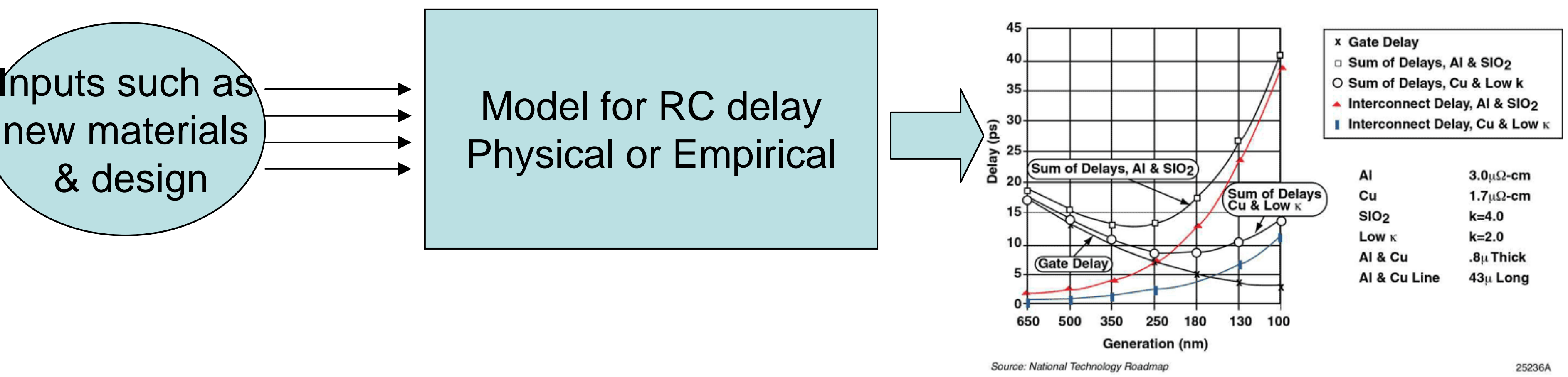
- Each semiconductor technology can be mapped on manufacturing cost and performance axis
- In reality, performance is not single axis but has multi-parameters such as speed, power, reliability etc.
- All these parameters can be measured and modeled depending upon specific applications
- Performance parameters can also be easily correlated to revenue ($$) depending on market size
- Having models which can model performance like speed, reliability helps in deciding the future course of technology

Motivation for Methodology



- Need for EH&S as 3rd axis, so technology can be mapped on space rather than plane, help in decision making
- EH&S like performance has multi-variables
- Health and Safety are hard to quantify
- So for now, Environmental Impact will be used as 3rd axis
- Even environmental is multi-parameter like energy, water and materials consumption and emissions
- These parameters can be related to cost ($$) through CoO models.
- To put Environment as 3rd axis, we need to have method or approach to quantify

Why Models?



- Models make us understand complex relationships b/w input and desired output (tradeoffs)
- Eventually helps in providing direction for future technologies – shaping future
- Also helps in resource allocation
- For models – needs to know what is desired output
- And also needs to have either physical understanding or huge data available in public domain

Outline

- Motivation for Methodology and Model
- **Defining objectives of project**
- Our Approach/Methodology
  - Brief description
  - Generating environmental footprint for standard CMOS logic device
- Case Study 2D v. 3D
  - Why 3D? (Benefits)
  - Describing different options
  - MIT 3D's process flow
  - Comparison and preliminary conclusions
  - Designing Handle Wafer
- Conclusion and Future Work

Objectives of Project

- Developing a methodology to analyze environmental impact evaluation for new process technology
  - Generate environmental footprint for standard IC technology so new process technology can be compared
  - Look for new technologies such as 3D IC and perform environmental impact evaluation
- In the process, develop good database which is more transparent relative to previous LCA studies
- Find out critical unit processes which can be designed not only from environmental but also from cost and performance standpoint
  - Preferably new unit processes which are in research phase and various options are under study

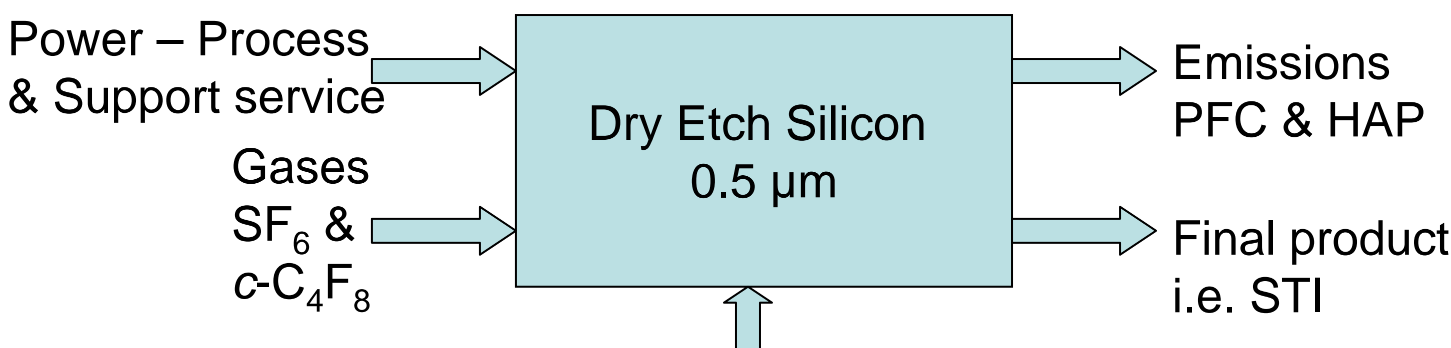
Environmental Footprint Standard IC

STI module (~6) → Front end Module (~70) → Back end Module (~90) → Packaging Module (~?)

Standard CMOS device with basic modules

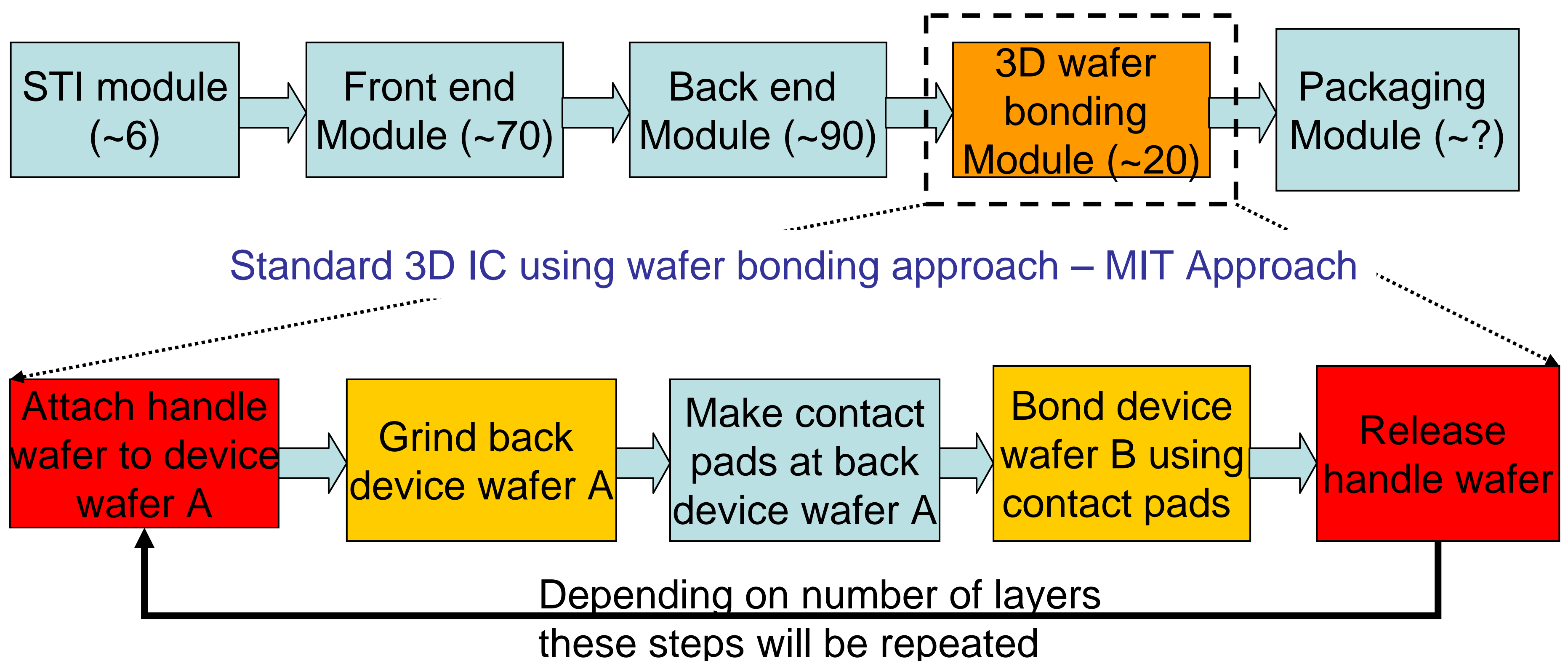
Nitridation 80 nm → Lithography → Wet etch nitride → Dry etch Si 0.5 µm → Ashing → DCVD SiO_2 1 µm → Oxide CMP

STI module in detail of discrete unit processes



Water and other support gases - recycled

Environmental Footprint 3D IC



Describing 3D wafer bonding module in terms of process flow

- New processes but did not seem to be environmentally alarming – still in research
- New process and seems to be environmentally non-friendly – still in research

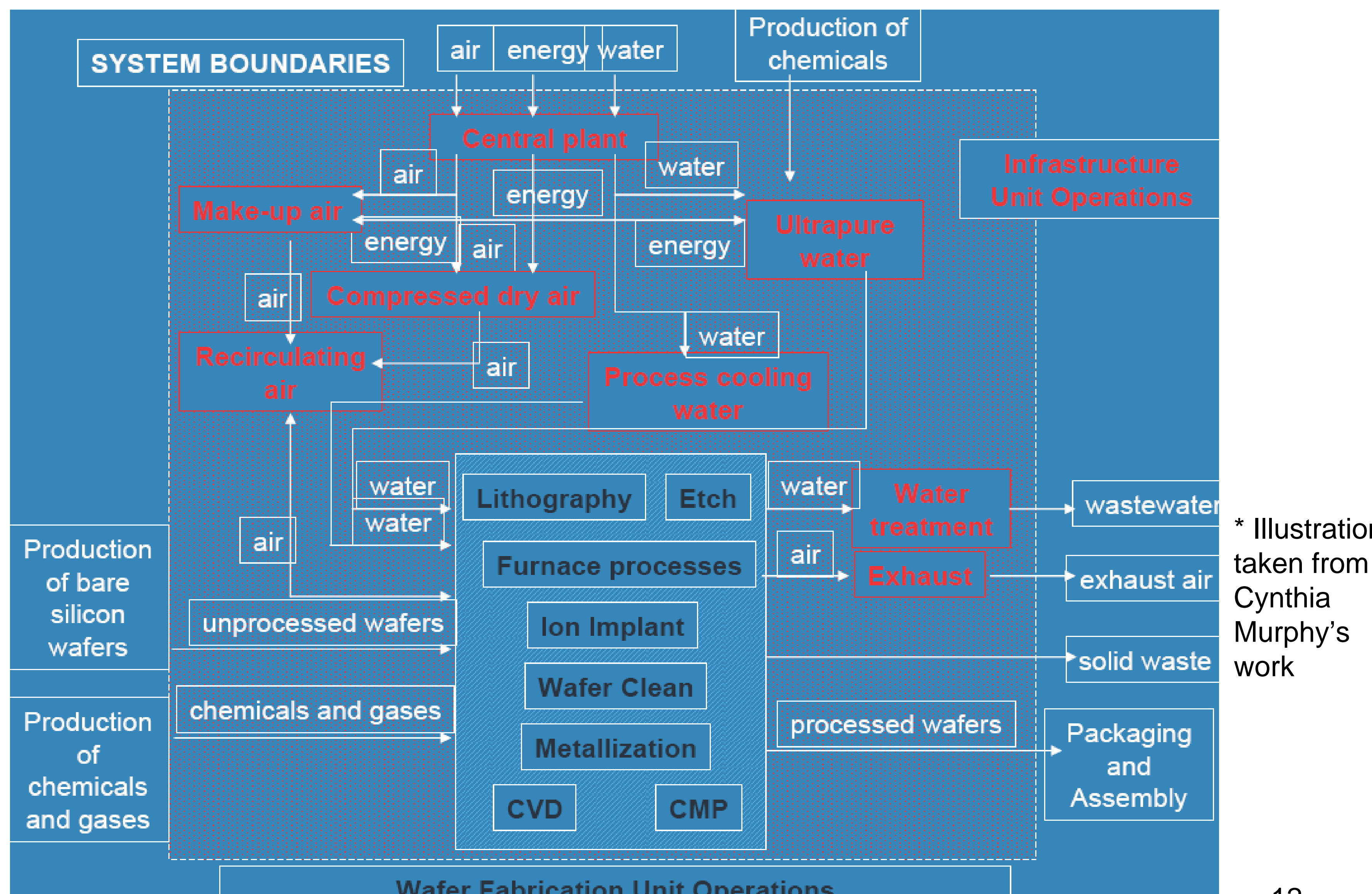
Outline

- Motivation for Methodology and Model
- Defining objectives of project
- **Our Approach/Methodology**
  - Brief description
  - Generating environmental footprint for standard CMOS logic device
- Case Study 2D v. 3D
  - Why 3D? (Benefits)
  - Describing different options
  - MIT 3D's process flow
  - Comparison and preliminary conclusions
  - Designing Handle Wafer
- Conclusion and Future Work

Description of Approach / Methodology

- Identify boundaries for analysis (as LCA – cradle to grave but want to do more like hybrid LCA which is LCI approach - proposed wafer fabrication as boundary)
- Identified six environmental issues, which will be addressed in this approach – energy, water, emissions (PFC), HAP's, VOC's and chemical wastage
- Define functional unit for comparison
- Compare alternative technologies in totality (consider full process technology as overall optimization is required and it is much complex function)
- Generate environmental footprint for standard IC technology process
- Eventually, new/additional processes environmental footprint is compared with existing technology in order to understand the relative change
- Identify new processes which are not proto-typed or still have performance –cost issues and design them for environment

System Boundaries



* Illustration taken from Cynthia Murphy's work

Example- Strained SiGe technology

- No change in Back end
- Assumption – no change in design besides changing the relative area
- For functional unit
  - Can be compared per unit Si area
  - Both performance and environmental impact should be normalized
- Few additional/new steps in Front end
  - New step like depositing epitaxial Ge along with Si, is very much like epitaxial deposition of Si (except need to evaluate GeH_4) and also additional annealing steps to relax Si-Ge layers
  - No high temperature annealing/ oxidation but low temperature for longer times (because of diffusion)
- Eventually, need to compare additional new steps with environmental footprint of existing standard technology by estimating new/ additional steps

Energy Estimation for standard CMOS

Unit Operation	No. of times each operation	Wafers/run	Wafers/hr	Power (KW)
Implant	9	25	20	27
CVD	11	10	15	16
Clean/ Wet etch	31/14 (45 total)	50	150	8
Furnace	2	150	30	21
RTP	5	1	10	48
Oxidation	4	150	30	21
Etch	17	1	30	135
Ashing	25	1	20	1/ 50 ?
CMP (Cu and ox)	14	1	25	29
Photo (coater)	25	1	60	90
Stepper	25	1	60	115
Electrodeposition	6	1	20	120
Sputtering	8	1	25	150

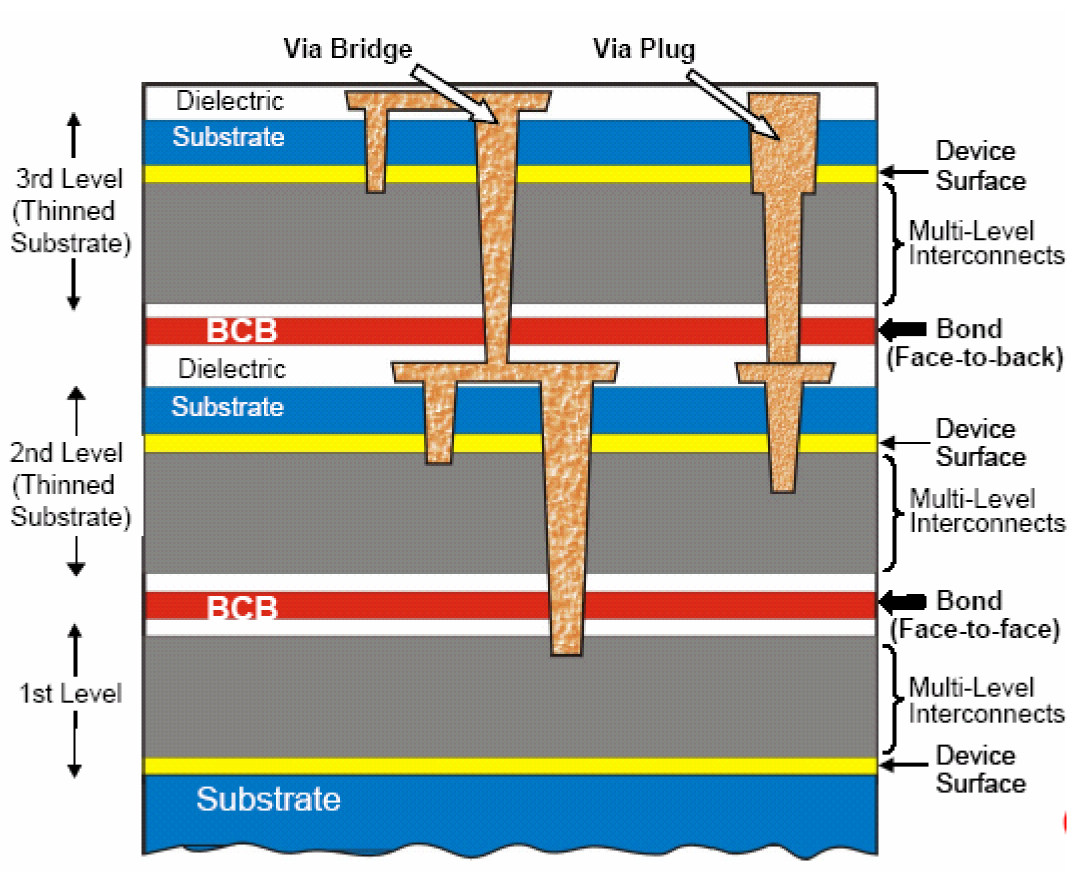
Available LCI Data and Sources

- Peter Dahlgren's Sematech Study (LCI)
  - Implanter, PECVD, Wet Spin etcher
- Cynthia Murphy's work
  - Furnace processes such as oxidation and annealing
  - Energy consumption for most of the unit processes for 0.13μm technology acquired with the help from Sematech and some other member companies
- Guess estimates

Outline

- Motivation for Methodology and Model
- Defining objectives of project
- Our Approach/Methodology
  - Brief description
  - Generating environmental footprint for standard logic device
- **Case Study 2D v. 3D**
  - Why 3D? (Benefits)
  - Describing different options for 3D
  - MIT 3D's process flow
  - Comparison and preliminary conclusions
  - Designing handle wafer
- Conclusions and Future Work

3-D Integrated Circuit and benefits



Courtesy: Prof. R. J. Gutmann, RPI

3D IC

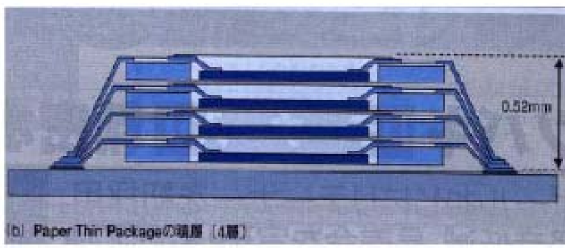
- Having more than one device layer
- Can have different functions

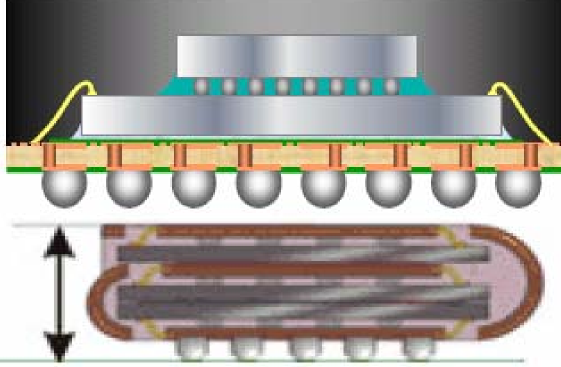
Benefits

- Increased packing density
- Reduced wire delay
- Lower power for similar feature size
- Reduced noise
- More functionality

3-D Integration Approaches

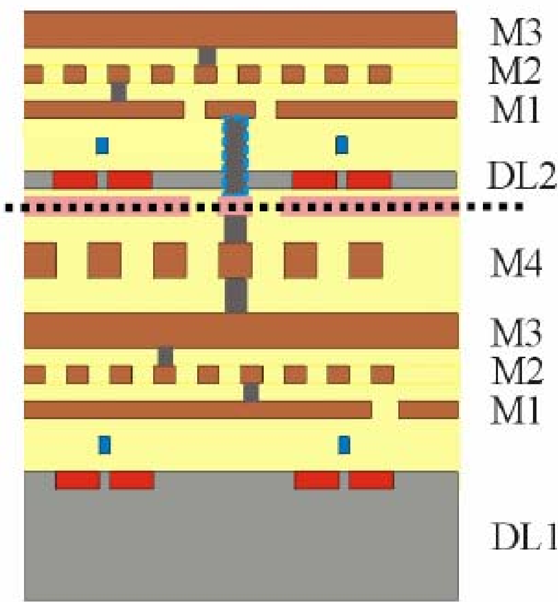
Package level Stacked chip/pkg





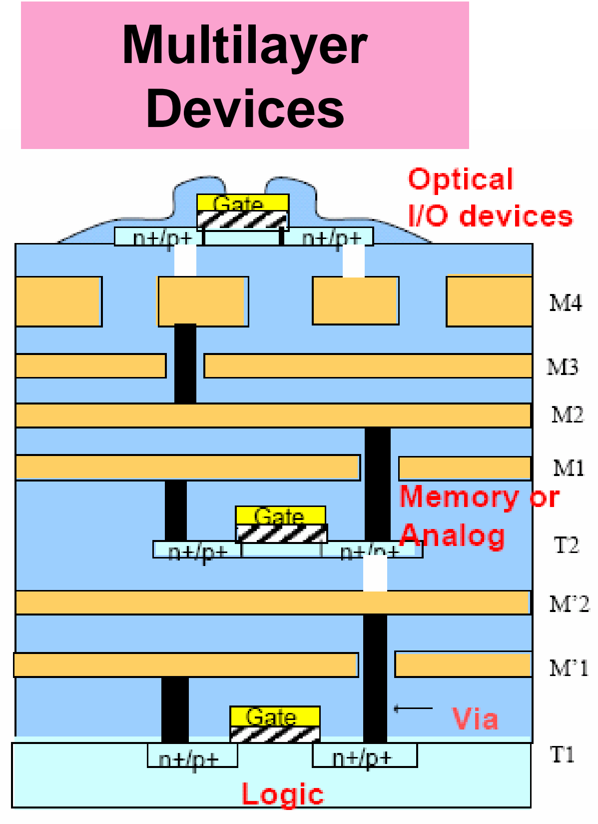
- Memory package
- Form factor, Cost, Time to Mkt
- Wirebond/ bump/ WLCSP

Interconnected Wafer/Die bonding



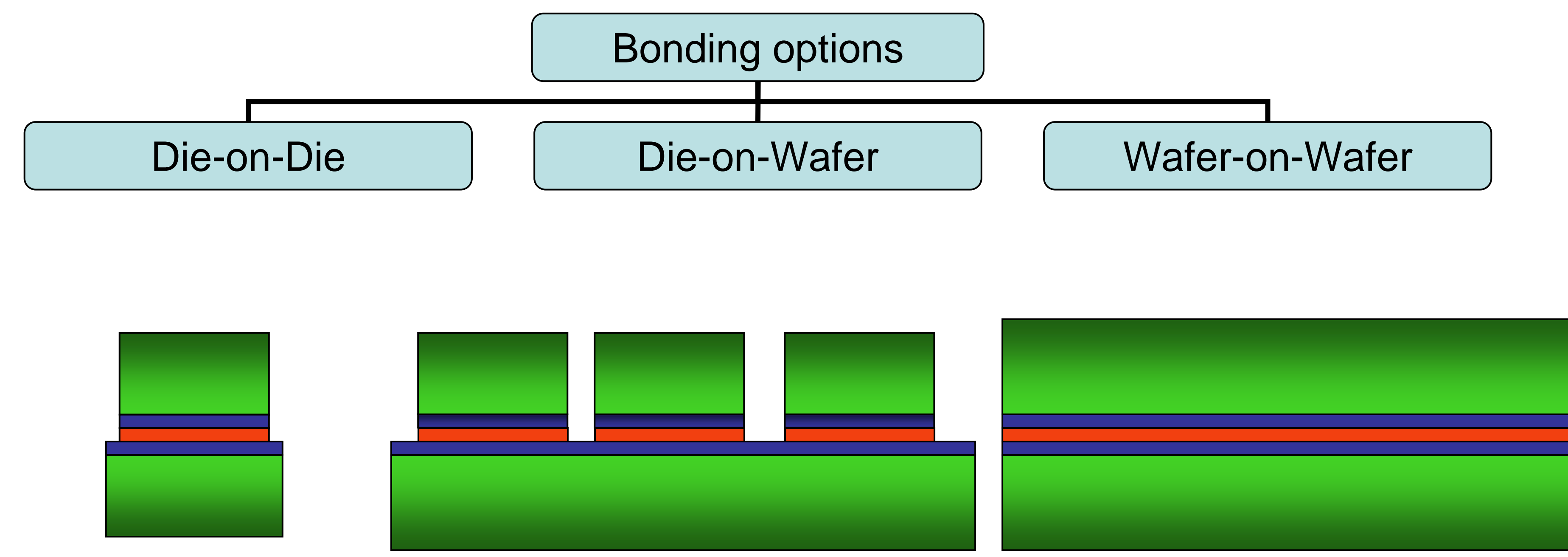
- Bonding of layers
  - Polymers, Oxides, Metal
- Through layer Vias
- Wafer Thinning
- Wafer processes

Multilayer Devices



- Sequential Si layer deposition

Various bonding options

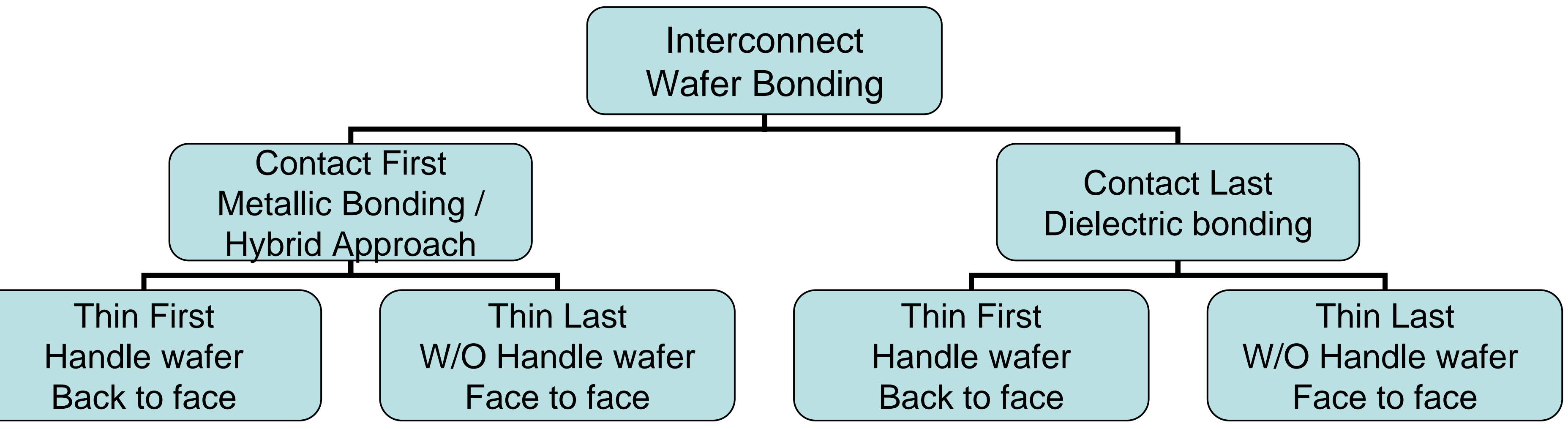


Die-on-Die
- Serial processing
- Use known good dies (KGD) and diff. size of dies

Die-on-Wafer
- Can be parallel processing
- Use KGD and diff. size of dies

Wafer-on-Wafer
- Parallel processing
- Same die footprint reqd.
- Does not use KGD

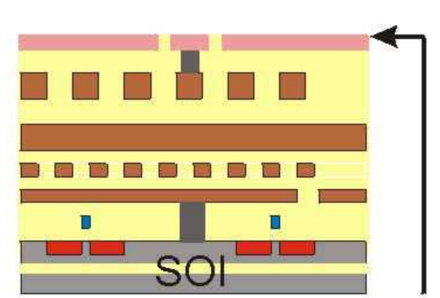
Categorizing 3D interconnect based integration schemes



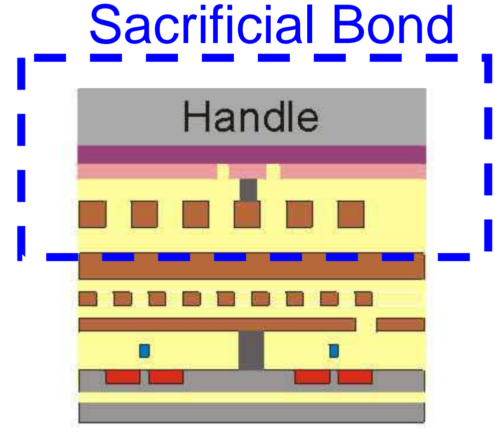
In all these approaches Super or through wafer Vias can be done

- either POST FE and can be grown as chain with all interconnect layers and can be find while grinding
- or POST BE and can be etched afterwards

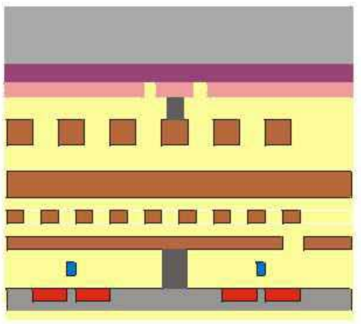
MIT's 3-D Process Flow – Thin First and Bond



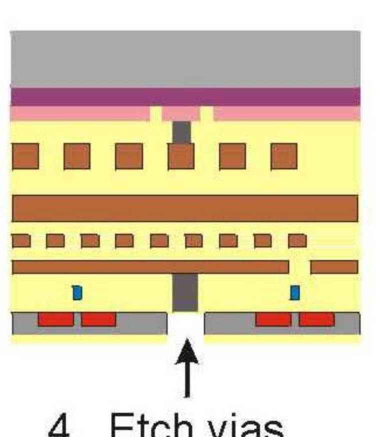
1. Cu patterning on SOI device wafer



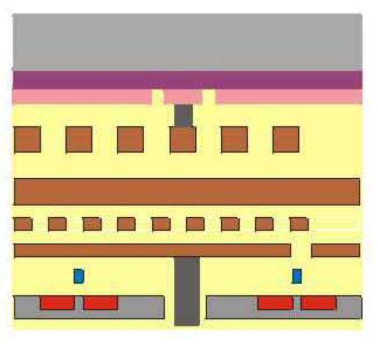
2. Bond to handle wafer



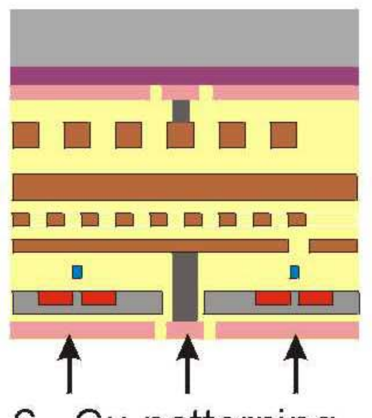
3. Thin back SOI wafer; stop on buried oxide



4. Etch vias

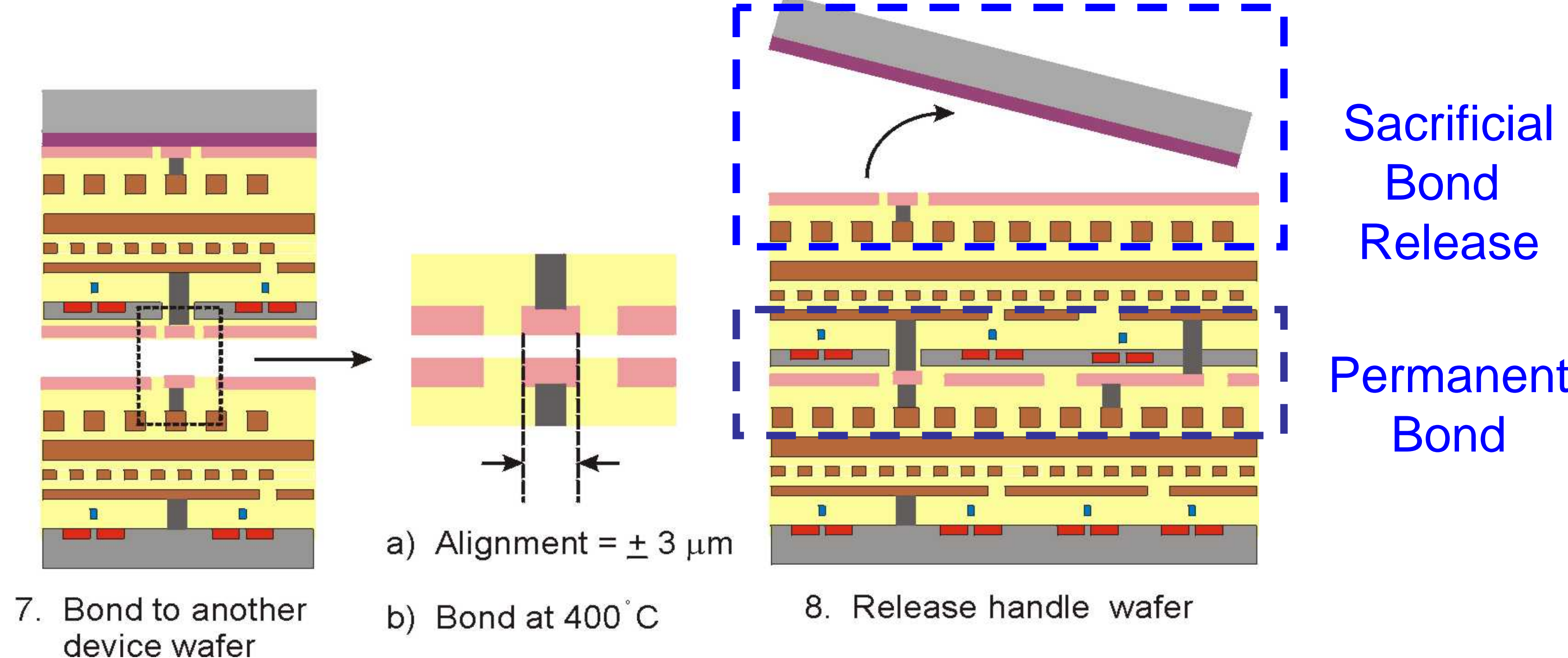


5. Via filling



6. Cu patterning

MIT's 3-D Process Flow – Thin First and Bond



Case Study 2D v. 3D

- Standard 2D IC energy inventory is shown earlier and full environmental footprint will be generated
- Functional unit is quite a challenge in case of comparing technologies such as 2D and 3D
  - Integrating cross functionality in case of 3D
  - No meaning of Si real estate
  - No real product available (so far)
  - Need to define functional unit depending on what are currently integrated for SoC (System on Chip)
  - 1 Logic + 1 Cache (high-speed SRAM) + 1 DRAM memory
  - Packaging has to be considered in this option
- New/additional 3-D processes were identified
  - Grinding has been estimated using oxide CMP, not exactly new to CMOS but not very common
  - Bonding was another new process has been estimated like annealing (with pressure term as another additional energy consumption)
  - Handle wafer bonding and releasing is new to IC technology, there is no standard process developed yet for this technology so still in design phase and can be designed as environmentally benign

New/Additional Processes in MIT's 3D Process Flow w/ Al as release layer

Unit operations	Description and no. of times
PECVD oxide	200 nm on handle wafer (Once)
Sputtering Al	20 micron-release layer on handle wafer (Once)
Sputtering Ta/Cu	50/300 nm on Handle wafer+ bond pads
CMP Cu	Twice before bonding
Grinding/ CMP Si	First layer of device wafer
Wet etch	Thrice (After grinding Si etch TMAH, BOX etch, Al release layer by HCl:H2O)
Photo	Once to make bond pads at back side
Dry etch	Si & ILD to make contacts/ etch oxide (twice)
Bonding	Twice (Handle to device & device to device)
Ashing	Once (Strip PR)
Electrodeposition Cu	Once in contacts formed at back side

Comparison b/w 2D and 3D in Terms of Processes

Unit operation	2D process flow (for one wafer)	Additional 3D processes in flow
Photo/stepper/ashing	25	1
Dry Etch	13	2
Wet etch/Clean	31/14	3/4
CVD	11	1
CMP	14	2
Sputtering Al	1 (0.5 μm for metal 1)	2 (20 μm)
Sputtering Ta/Cu	6	1
Electrodeposition Cu	6	1
Bonding	0	2
Grinding	0	1

First-Order Energy Comparison in 2D v. MIT's 3D Process Flow

- Sputtering twice 20 micron Al for release layer seems outrageously huge number and largely energy consuming
- Bonding and Grinding are new processes which needs to be estimated
- Besides these all processes are small in percentage as compared to full process flow, so can be easily ignored
- Grinding can be estimated using CMP, just that it takes a bit longer to thin wafer but energy usage must be similar
- Bonding can be estimated using vacuum process with temperature budget of 300 degrees centigrade for half an hour

Handle Wafer : Function and Issues

- It seems that handle wafer will play an important role for 3D IC technology
- Handle wafer bonding and releasing is one process for which there no standard process exist
- This present an unique opportunity of DFE (Designing for Environment) with accounting other parameters performance and cost.
- This process unlike any other process does not influence process any process upstream and downstream in defined system boundaries for this particular study
- Function
  - For thin first approach, acts like mechanical support
  - It also provides repeatability or stacking
- Issues
  - Withstand grinding for 600 microns
  - Withstand wet etch-back of Si (TMAH)
  - Should etch selectively to other bonding layer (in our case Cu-Cu)
  - Bonding and release thermal budget is limited by back-end
  - Release with ease

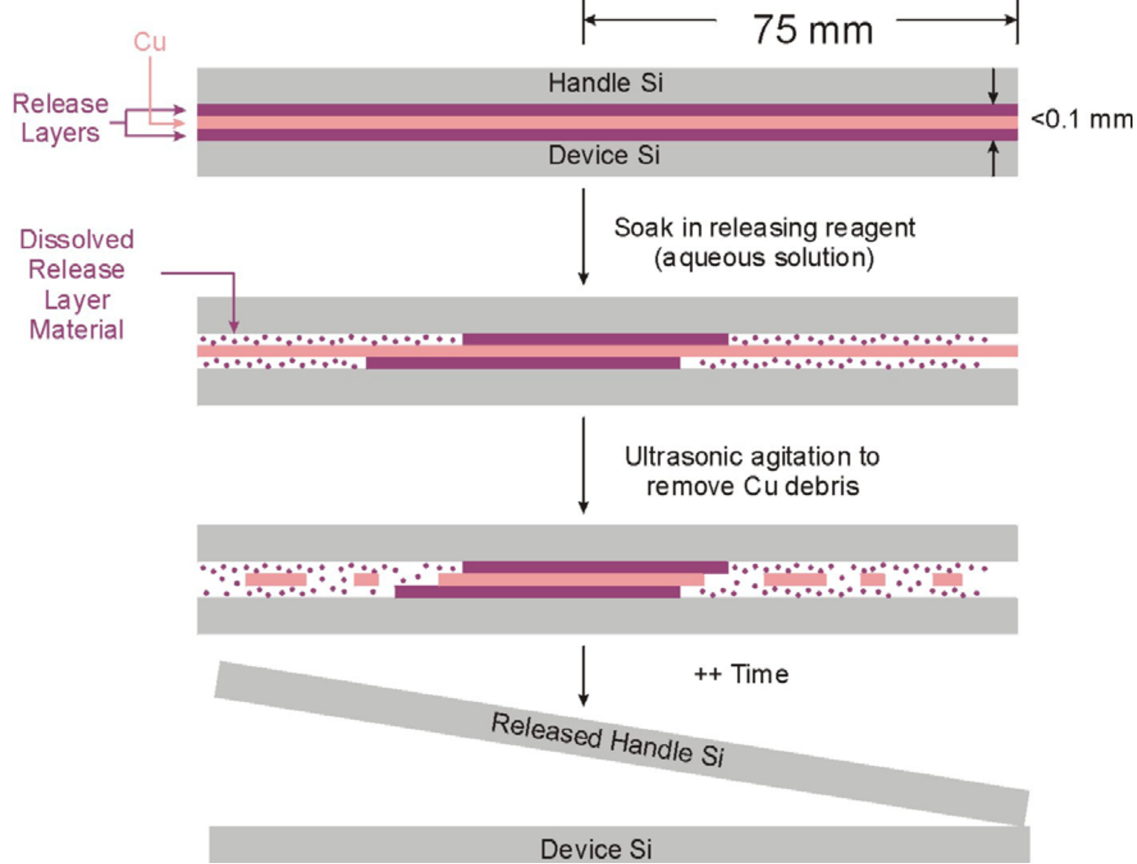
Handle Wafer Options - explored

- For MIT two release mechanism explored
  - Al release layer (inconsistent - mass transfer issues)
  - Smart Cut process (expensive)
- Other handle wafer options explored
  - Polymer released with laser annealing through glass wafer by IBM (seems interesting but no idea about repeatability)
  - Porous Si wafer bonded with polyimide and BCB, etched through pores by IZM (kind of expensive – assuming porous Si wafer is expensive)
  - E-Chuck idea proposed by IZM (just idea no study conducted)
  - Other places no information provided (IP sensitive)

Approach for DFE – Handle wafer

- First find options which will perform
  - In this case performance will be defined by functionality and process capability
- So performance will act as screening option
- Secondly all options will be put on cost and environmental axis along with performance
  - For acquiring environmental footprint, need to estimate all six environmental concerns specific to each choice and with as much chemical specific data
  - First order cost estimation will be done and economies of scale will be applied

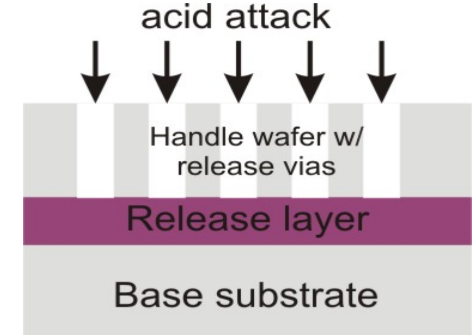
Handle Wafer Release Protocol – in discussed MIT 3D's approach



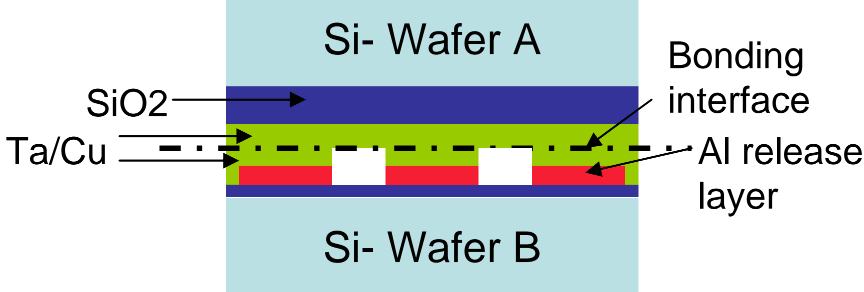
Mass transfer problem in case of Al as it reacts with HCl and gives H_2 which impedes further reaction

Ideas for Handle Wafer

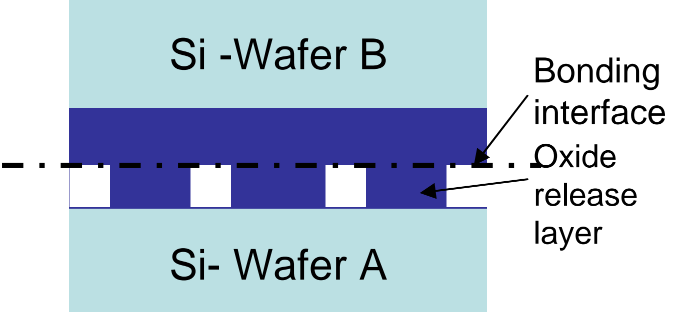
- Solving the mass transfer problem for etch release - by making channels in handle wafer which can be used by acid to have more accessibility
  - Making through wafer vias in handle wafer which can used for acid attack. (manufacturability ?) Figure a
  - Making channels in Al release layer so its thickness can be optimized. Figure b
  - Making channels in oxide release layer in case of oxide-oxide bonding (used by MEMS). Figure c
- Issue for last two options how it can withstand grinding etch-back and after that is patterning possible on thin membranes?



a) Al release layer w/ release vias



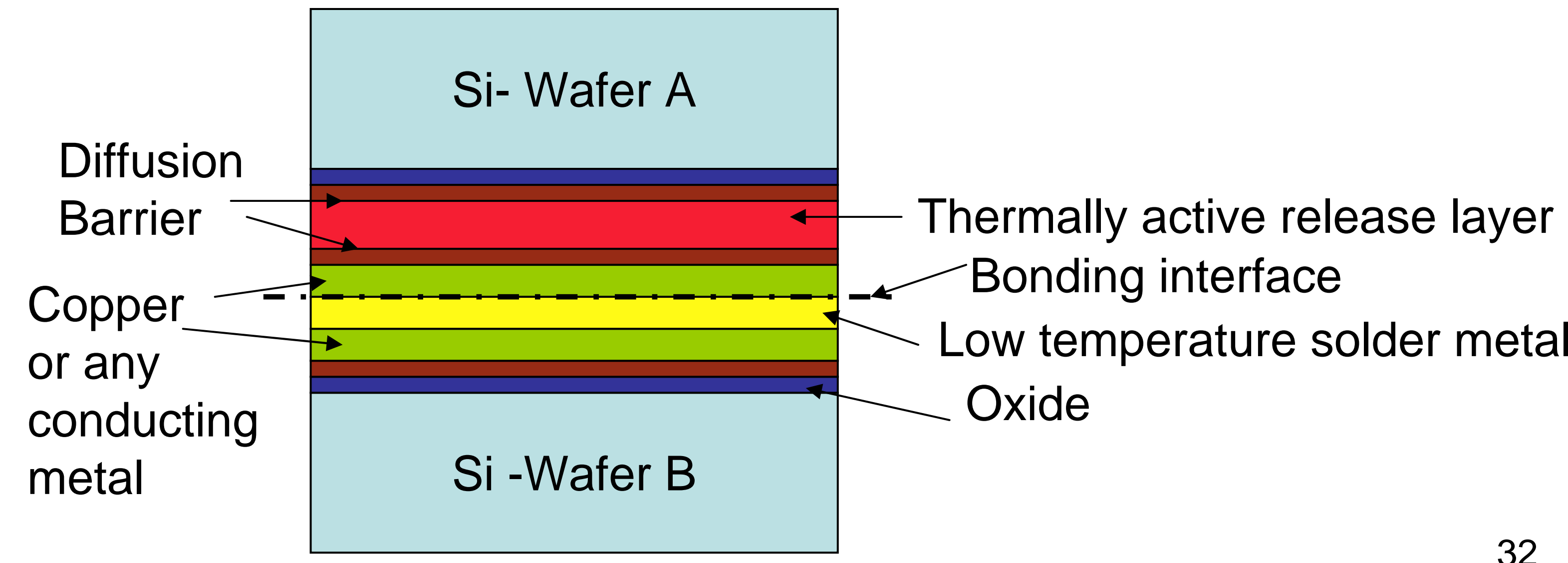
b) Al release layer w/ channels



c) Oxide release layer w/ channels

Ideas for handle wafer

- Reducing bond temperature so the handle wafer can be released at higher temperature
- Higher temperature can not be higher than 350-400 C as it is highest one can go in back-end
- Releasing w/ high temperature may reduce problems of mass transfer
- For reducing bond temperature – solder bonding used



Conclusion and Future Work

- Methodology for environmental evaluation has been established
  - Establish environmental footprint or impact for standard flow
  - Compare it with new/additional significant processes
- MIT 3D technology serving as case study from energy standpoint
  - Will consider similar technology comparisons for other environmental axes such as air emissions like VOC's, HAP's and GWP gases
- Identified Handle wafer as critical process in 3D IC
- Comparing different options for handle wafer on three axes: performance, cost and EH&S

Acknowledgments

- NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing
- Chuan-Seng Tan, Andy Fan and Rajappa Tadepalli, graduate students at MIT
- Prof. Philip Gschwend and Sarah Jane, Civil and Environmental Engineering, MIT
- Robert E. Jones, Scott Pozder and Ritwik Chatterjee, Advanced Interconnect Group, Freescale, Austin
- Nikhil Krishnan, Applied Materials
- Sri Satyanarayana, Sematech
- Microsystems Technology Laboratories Staff, MIT