Surface Passivation and Characterization of Germanium Channel Field Effect Transistor Together with Source/Drain Engineering

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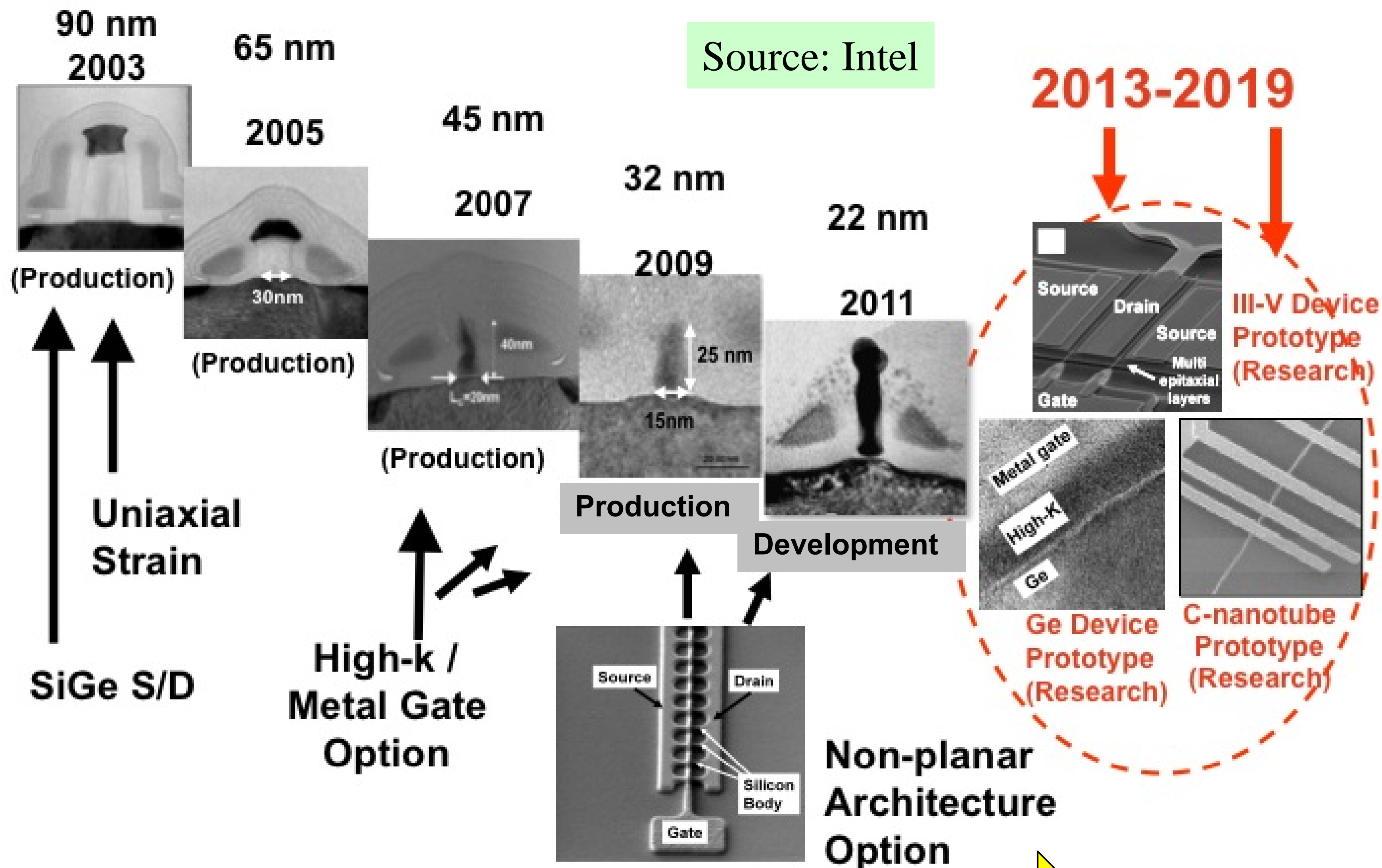
Outline

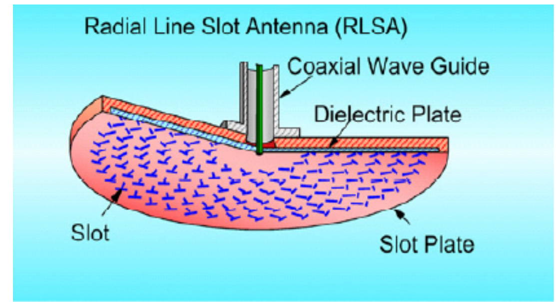
1. Introduction
2. Surface passivation for Ge
3. Source / Drain junctions for Ge
4. Contributions and future work

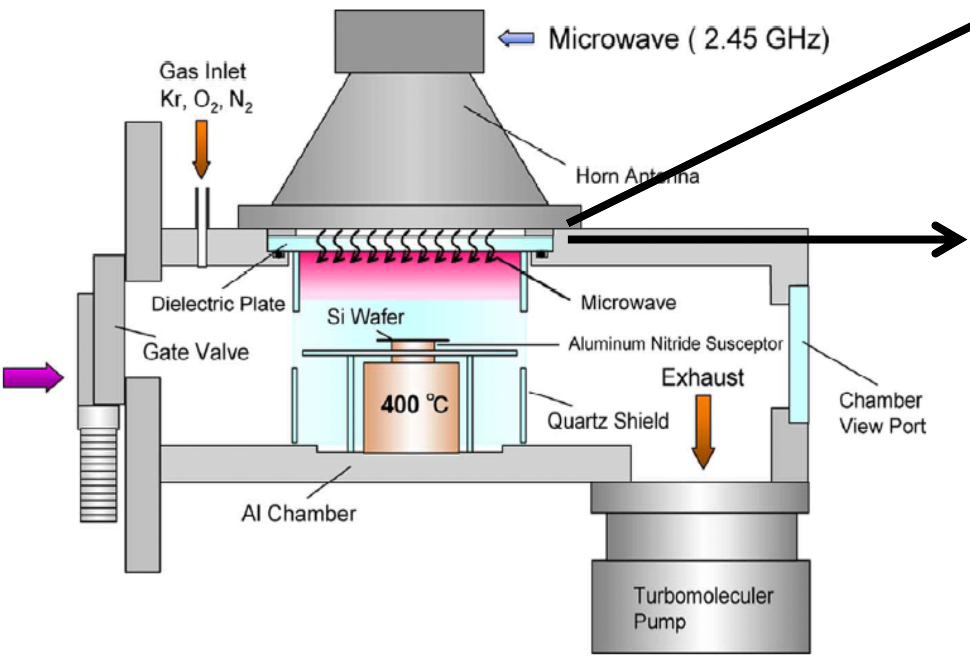
Transistor Scaling

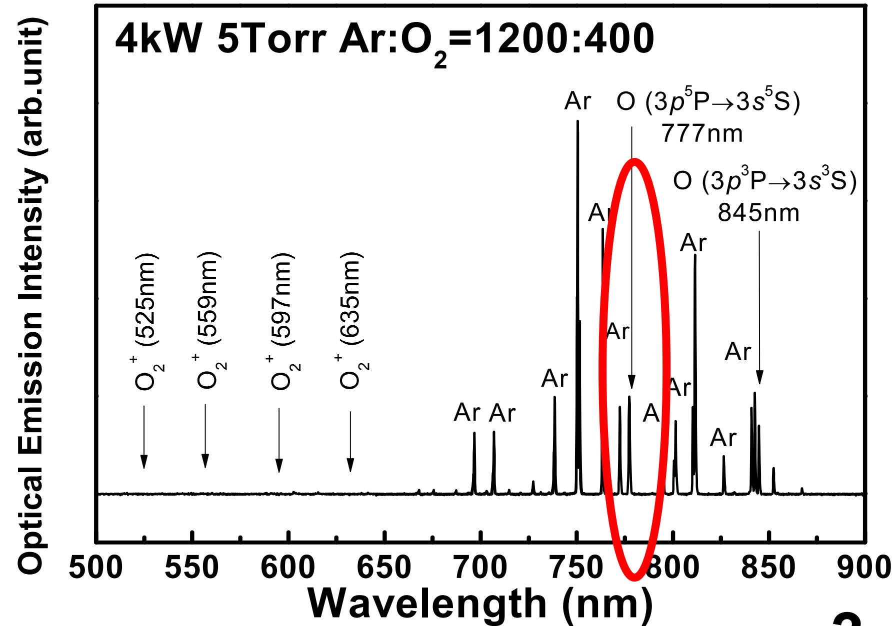


SPA Radical Oxidation

- Radical oxidation[1]
  - Physically breaking bonds and amorphization by atomic O*
  - Enables very low temperature oxidation
- Slot Plane Antenna (SPA)[2]
  - Uniform supply of high density radicals



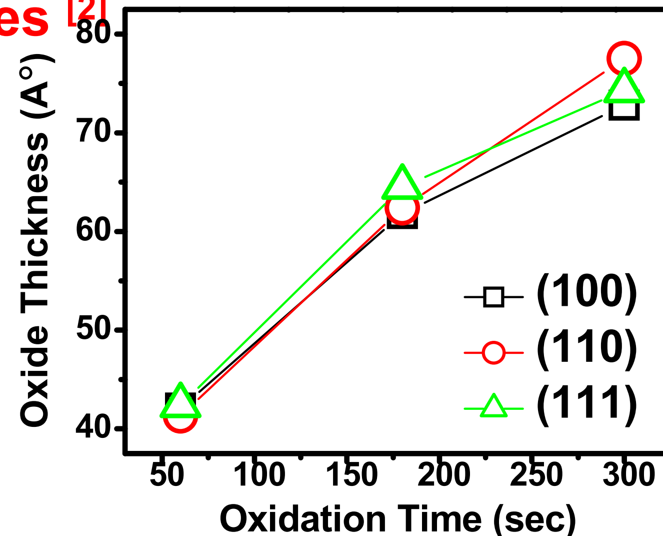


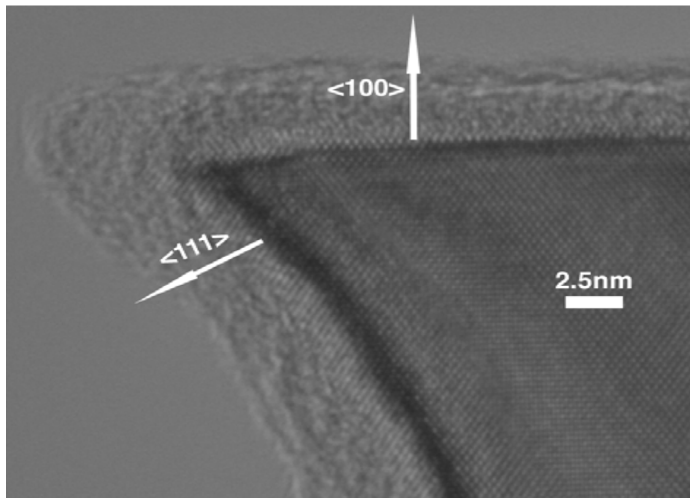


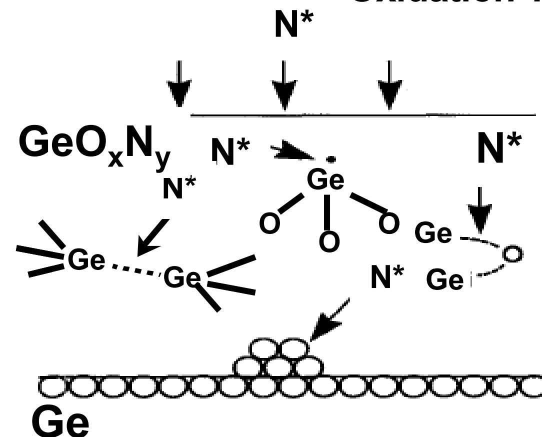
[1] M.Nagamine et al, IEDM 1998, [2] T. Ohmi et al., Proc of IEEE 2001

Unique Features of SPA

- Substrate orientation independent growth [1]
  - Conformal oxidation enabling 3D devices [2]
- Low temperature processing[1]
  - Low D_{it} GeO_2 [3]
- Nitridation [1]
  - GeO_xN_y Interfacial Layers (IL) [3]





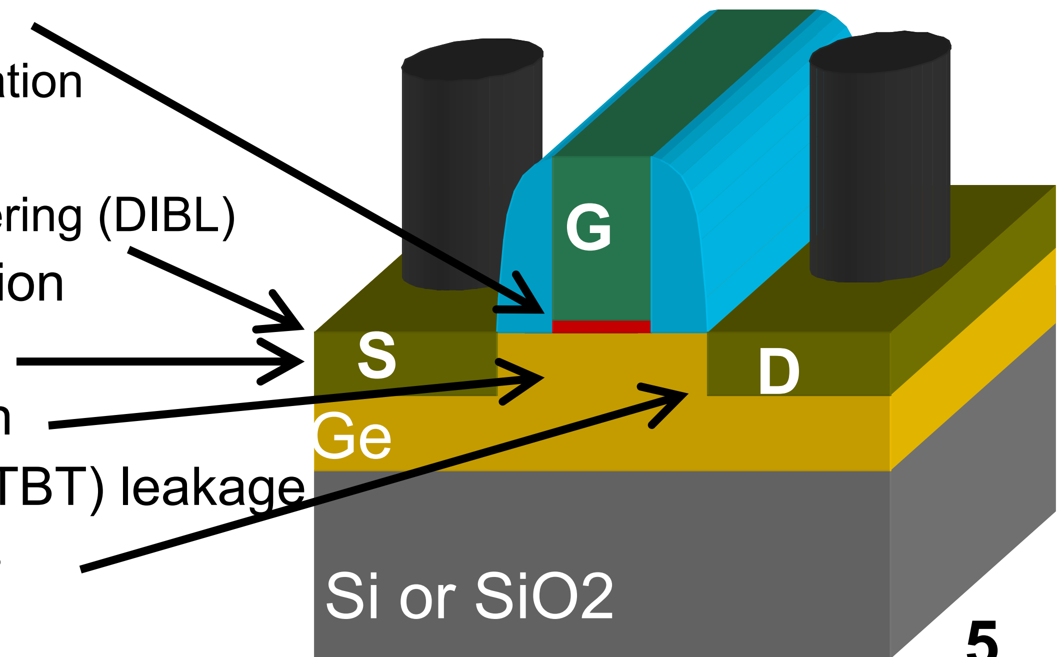


[1] T. Ohmi et al., Proc of IEEE 2001 [2] G.Thareja et al, Trans. Elec Dev (in prep.), [3] G.Thareja et al., Dev. Res. Conf., 2008

High Mobility Channel Ge

- Advantages
  - High electron/hole mobility
  - Compatibility to Si LSI
  - Lower temperature process
  - Possible V_{dd} scaling
- Process and device Issues
  1. Surface Passivation issues
     - Loss of Q_{ch} and μ degradation
  2. Deep S/D junctions
     - Drain induced barrier lowering (DIBL)
  3. Poor N-type dopant activation
     - High parasitic resistance
  4. Small electron mobility gain
  5. Band-to-band tunneling (BTBT) leakage
     - High I_{off} for scaled devices

	Si	Ge
Bulk μ_e(cm²/Vs)	1600	**3900**
Bulk μ_H(cm²/Vs)	430	**1900**
Band gap (eV, 300K)	1.12	**0.66**
Dielectric constant	11.9	**16**



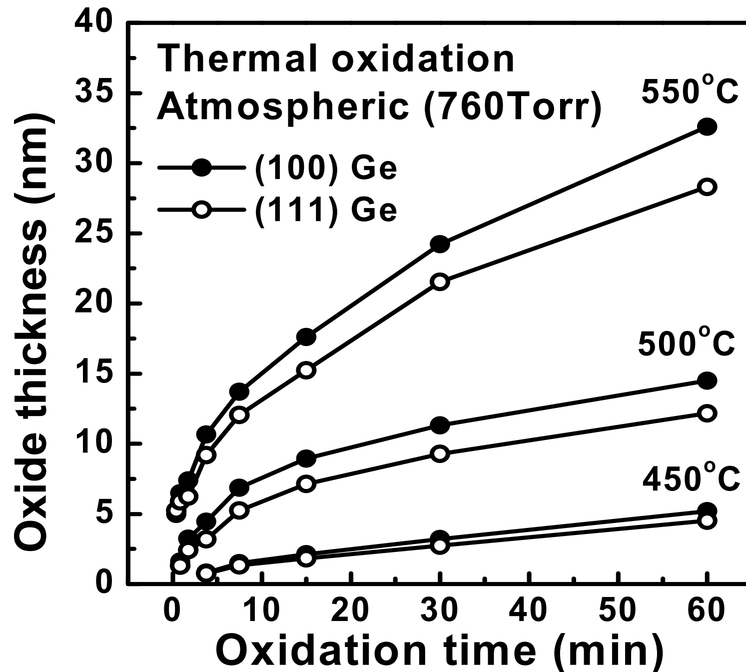
Ge MOS and Solutions

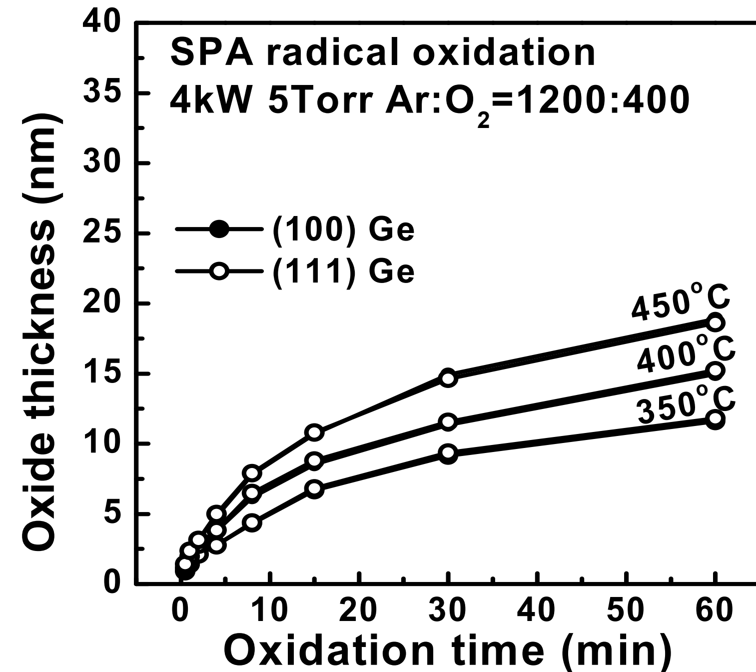
- Surface Passivation Issues
  - Thermal[1] GeO_2, Ge_3N_4 Interfacial Layers (IL) with High-k
  - Ultra-thin[2] GeO_2 IL using SPA radical oxidation
- Ultra Shallow Junctions[2]
  - Plasma Immersion Ion Implantation (P-III)
- High Dopant Activation
  - Laser Thermal Processing (LTP)[3]
  - Rapid Thermal Annealing (RTA) [4]
- Mobility Booster- Uniaxial Stress Engineering[5]
- BTBT Reduction - Si-Ge-Si Hetero-structure design[6]

[1] T. Nishimura et al. , VLSI Symp. 2010 [2] **G.Thareja** et al, Dev. Res. Conf., 2010
[3] **G.Thareja** et al., IEDM 2010 [4] **G. Thareja** et al., Elec. Dev. Lett. (under prep), 2010.
[5] M. Kobayashi et al, VLSI Symp. 2009, [6] T. Krishnamohan et al, VLSI Symp. 2006

GeO_2 Growth Rate

- Radical vs thermal oxidation
  - No orientation dependence was observed in radical oxidation between (100) and (111) Ge[1]
  - This was confirmed on silicon previously

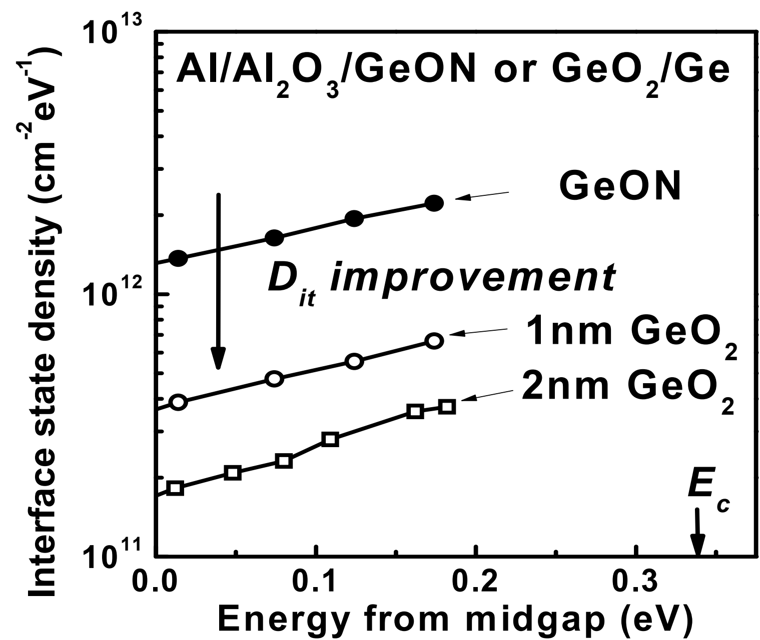


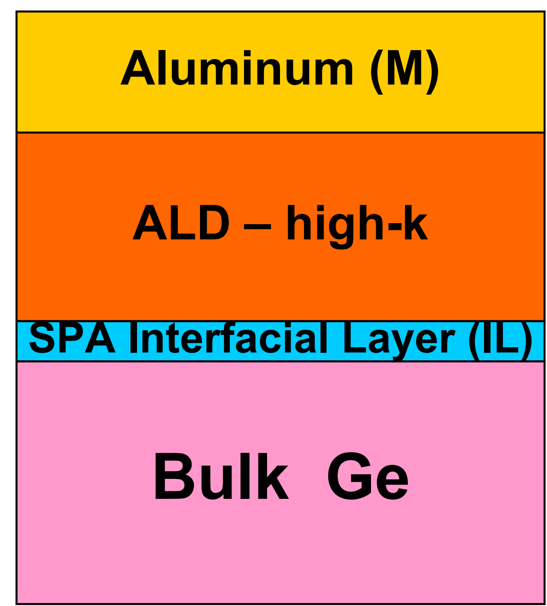


[1] M.Kobayashi, **G.Thareja et al,** J. Appl. Phys., 2009

D_{it} of GeO_2/Ge

- Comparison between GeO_xN_y and GeO_2
  - D_{it} was measured by conductance method
  - Significant improvement from GeON
  - Achieved ***D_{it} ~ $2x10^{11}cm^{-2}eV^{-1}$*** at midgap

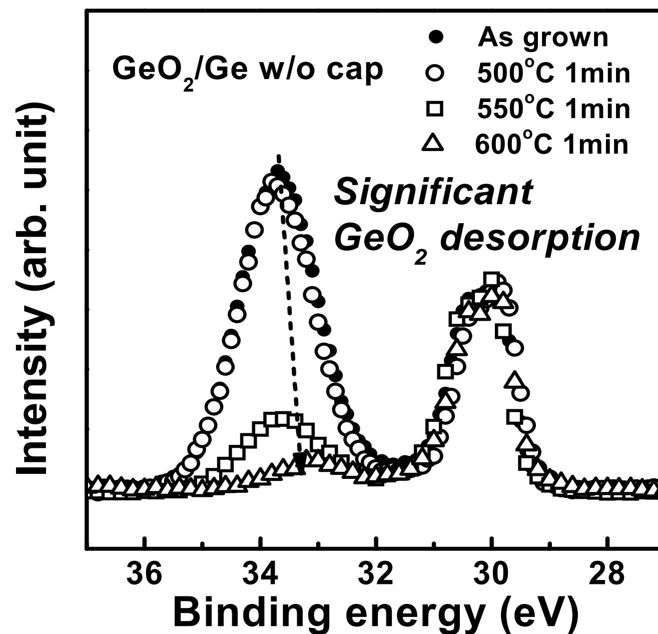


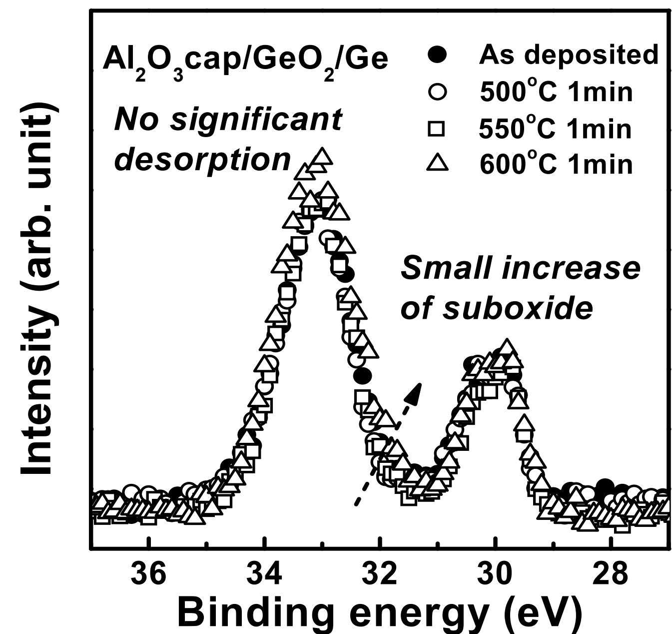


[1] G.Thareja et al., Dev. Res. Conf., 2008

Thermal Stability of Gate Stack

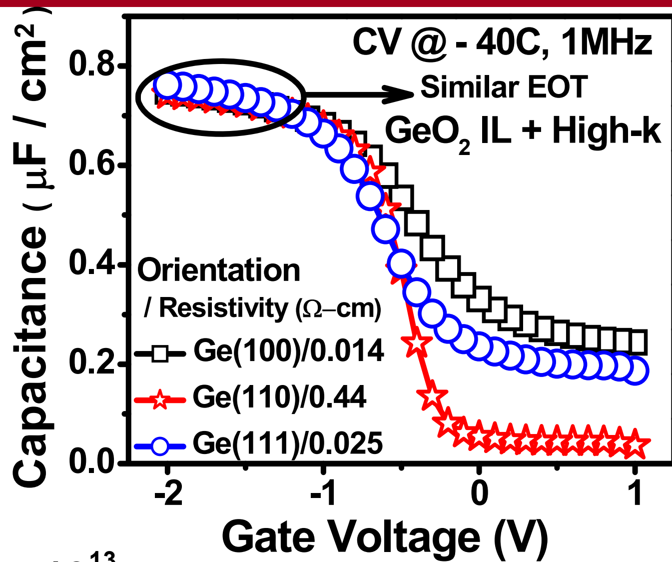
- GeO_2/Ge
  - Significant GeO_2 decomposition and GeO out-diffusion
- Al_2O_3/GeO_2/Ge
  - Al_2O_3 works as an out-diffusion barrier and maintains GeO_2
  - Suboxide formation

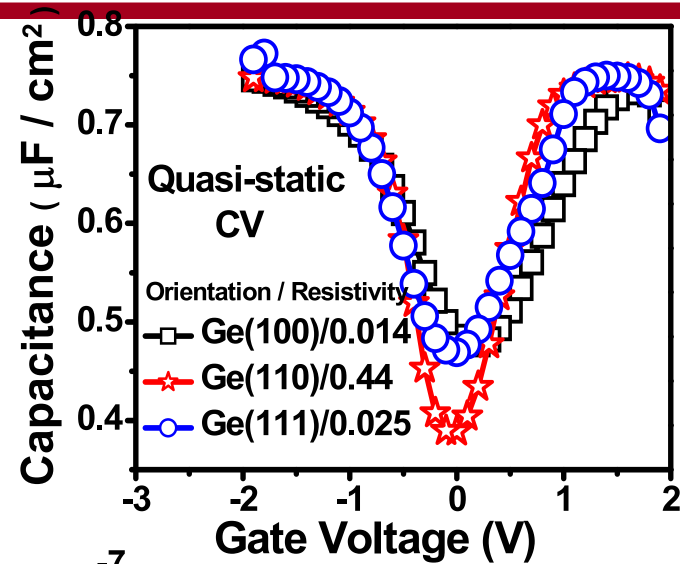


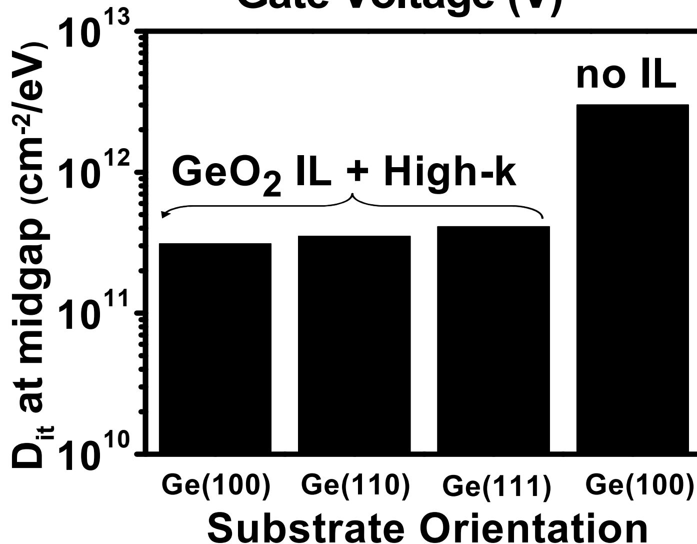


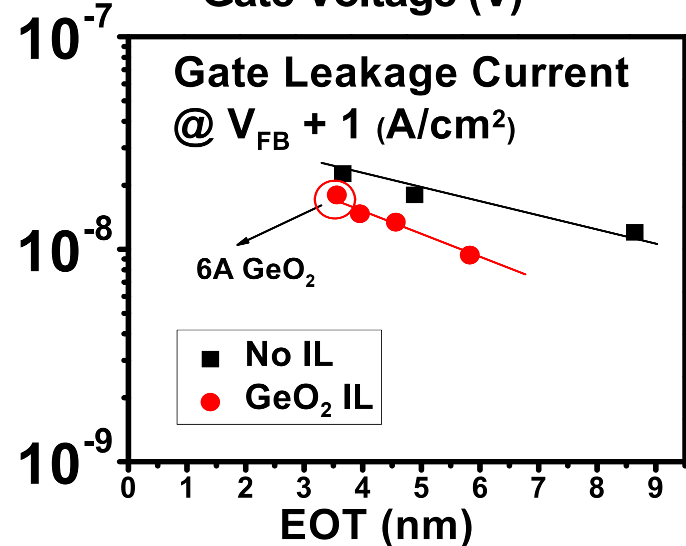
[1] M.Kobayashi, **G.Thareja et al,** J. Appl. Phys., 2009

GeO_2 : Growth Rate, D_{it}, Scalability



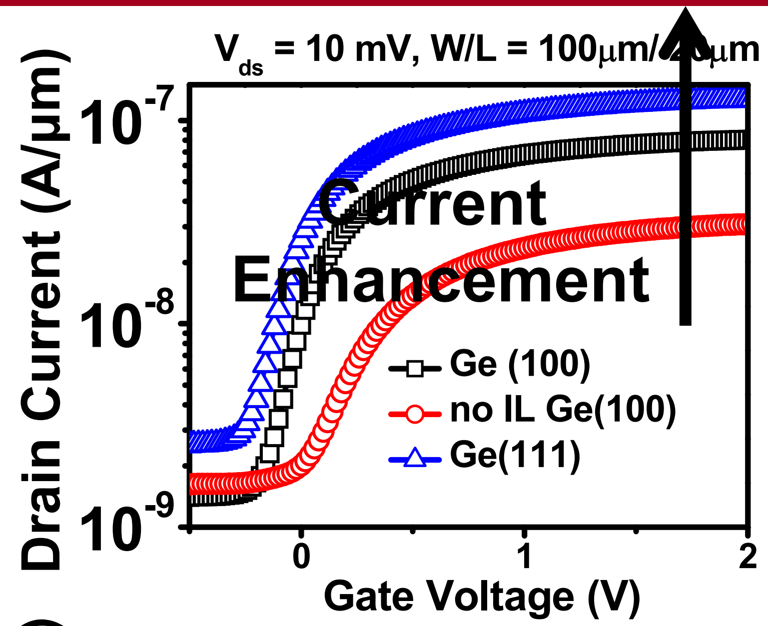


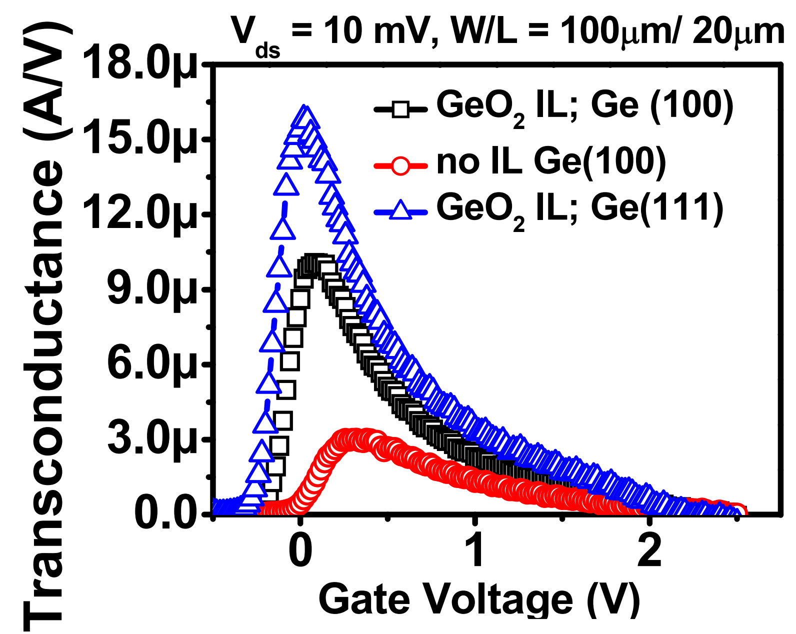


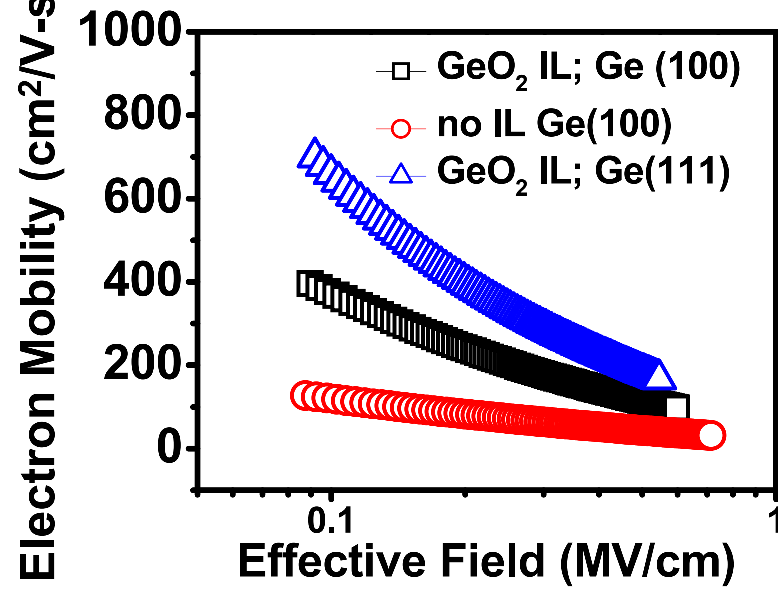


Substrate orientation independent growth rate and D_{it}, Ultra thin IL have be realized

Drive Current, Mobility Enhancement



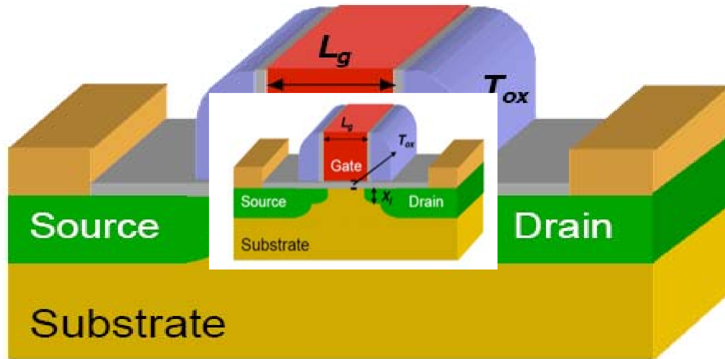


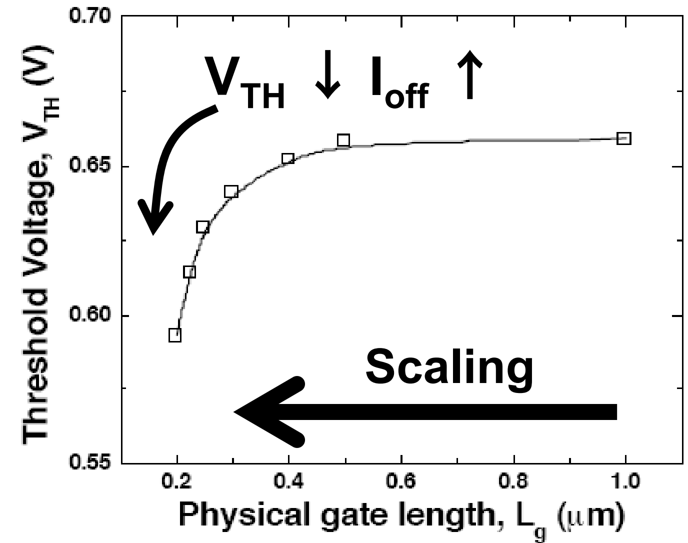


Ge(111) has higher mobility – lower m*
Samples without GeO_2 – poor mobility - interface/coulomb scattering

[1] **G.Thareja et al.,** Elec. Dev. Let. (submitted), 2010

S/D Junction Depth (X_j) Scaling

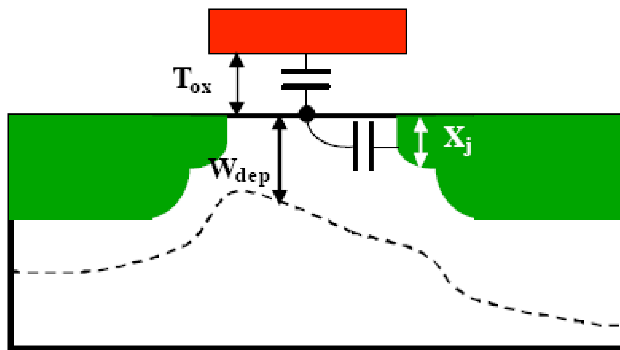


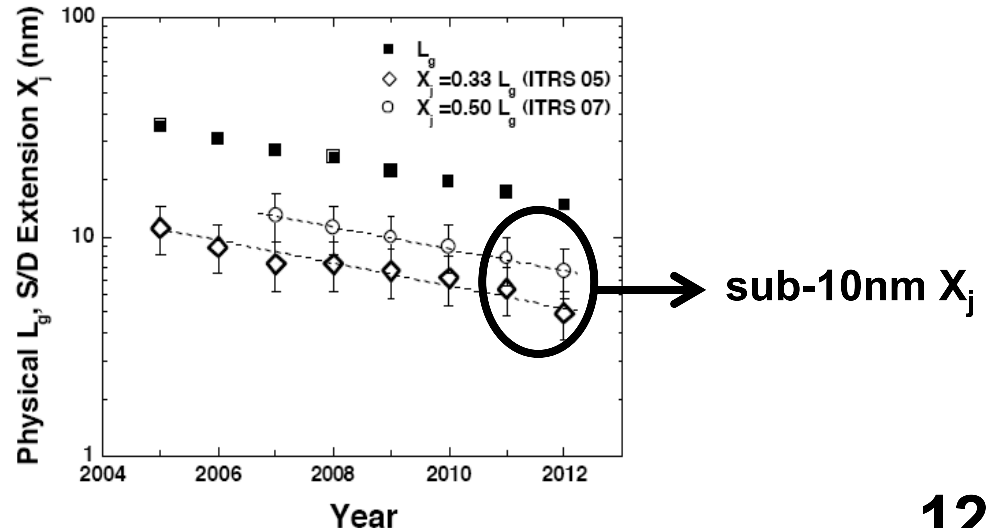


Short Channel Effect (SCE)

L_g ↓ , Source & Drain interact – V_{TH} ↓ , I_{off} ↑

Drain Induced Barrier Lowering (DIBL) exacerbates SCE

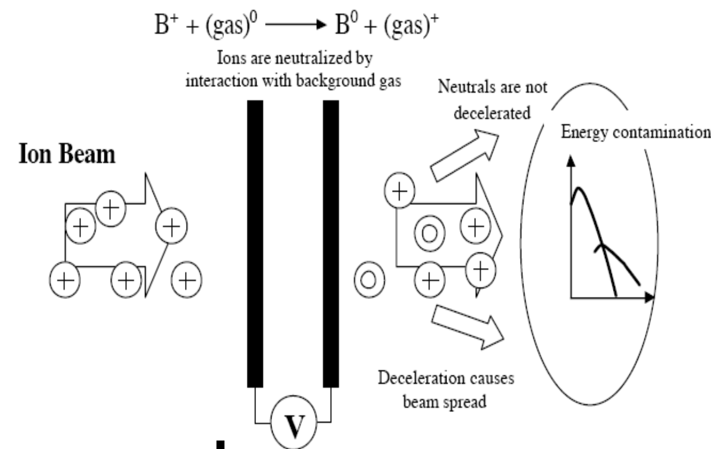


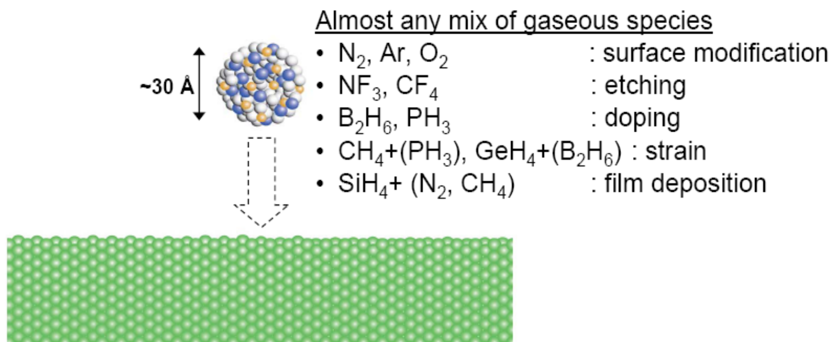


T_{ox} ↓ , W_{dep} ↓ , X_j ↓ → SCE ↓

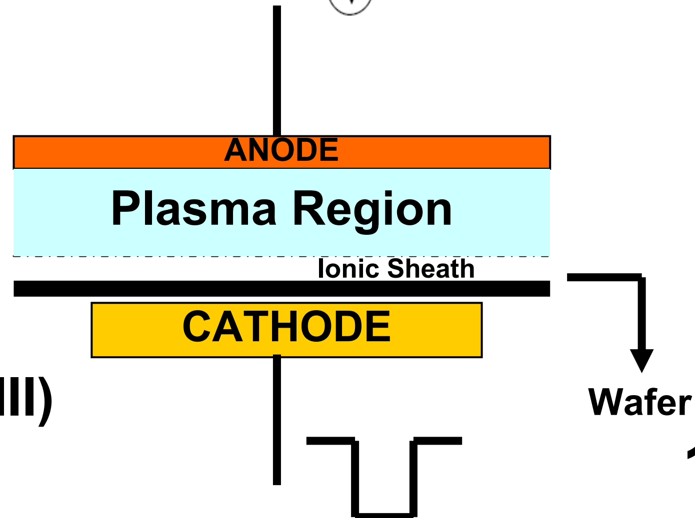
USJ Route

- Ion Implantation (I/I) – Ultra Low Energy - Deceleration mode
  - Issues
    - Low beam current – longer implant time – low throughput
    - Energy contamination due to neutrals
    - Beam Spreading
    - Wafer non-uniformity issues
- Some respite by molecular implants
- Gas Cluster Ion Beam (GCIB)

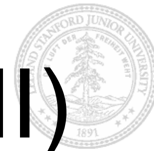




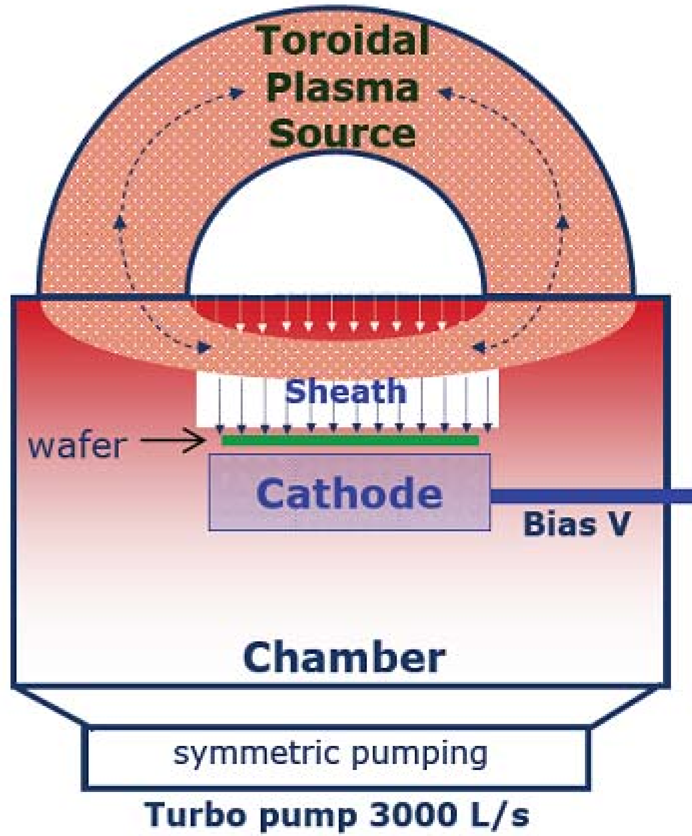
- Plasma Immersion Ion Implantation (P-III)



Plasma Immersion Ion Implantation (P-III)



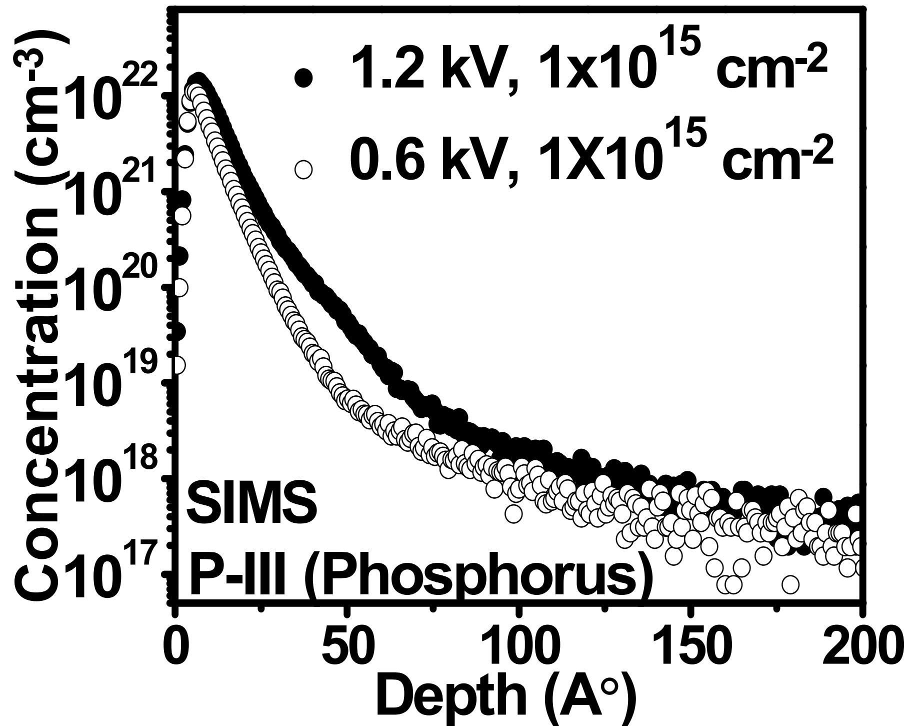
- Doping capability: BF3, B2H6, AsH3 and PH3
- In-situ chamber clean & season capability
- High throughput and high process repeatability

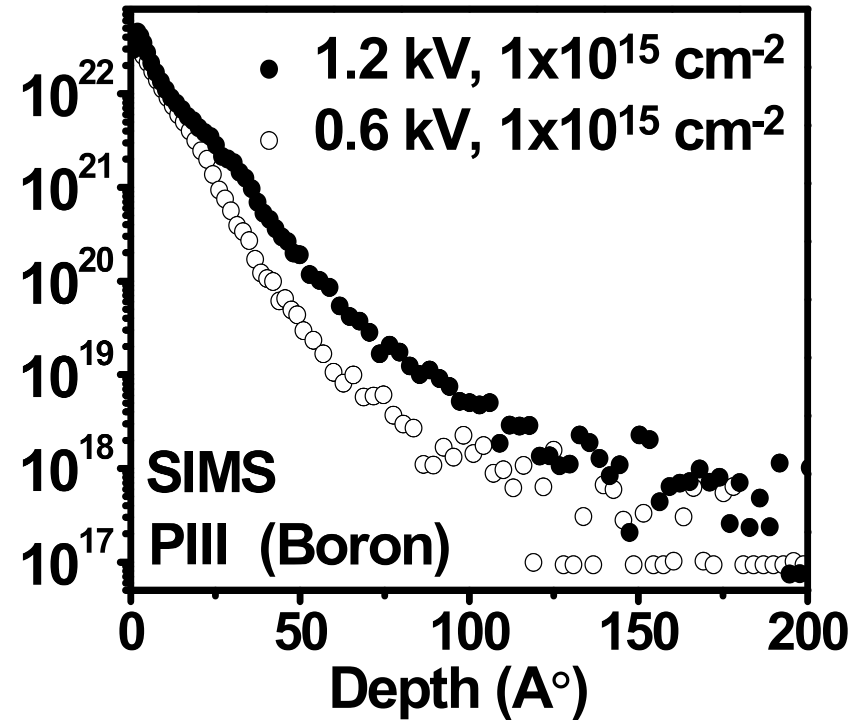


- Plasma sustained by induc ed RF
- RF wafer bias match controls implant ion energy
- Temperature of the chamber and cathode independently controlled

- Plasma created above the wafer
- Pulsed voltage applied on the wafer
- Ion acceleration and implantation

P-III in Ge

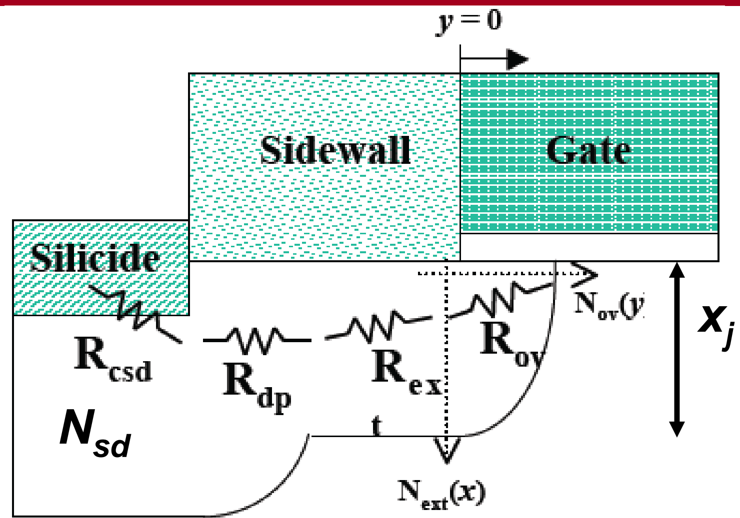


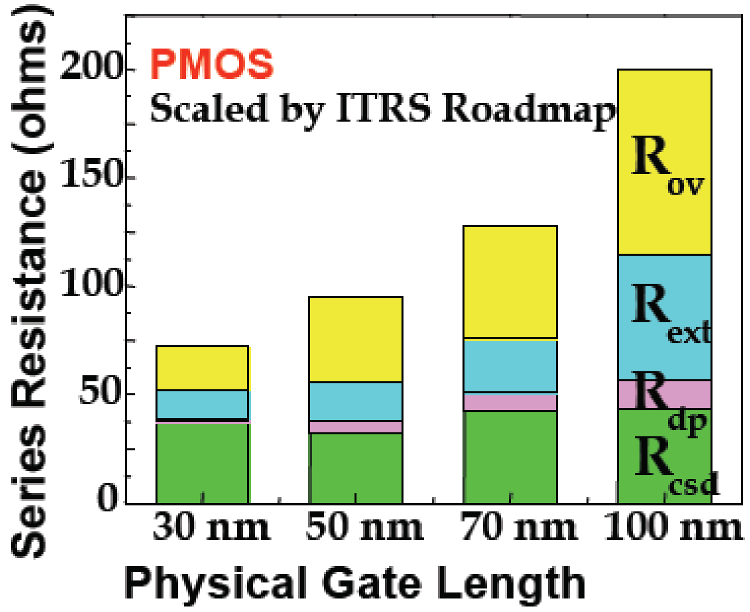


- X_j < 10nm @ 5 x 10^{18} cm^{-3}
- Shallower junctions possible
  - Scaling the voltage
  - Using arsenic species

G.Thareja et al. "Ultra Shallow Junctions in Germanium for sub-22nm ITRS Technology Node ", *IEEE Electron Device Letters*, 2010 (under preparation)

Poor Dopant Activation: Parasitic Resistance





J. Woo et al., TED 2002

- Impact of series resistance
  - Decrease gate overdrive
  - g_m reduction
- Resistance scaling
  - Channel resistance scalable
  - Contact resistance not scalable

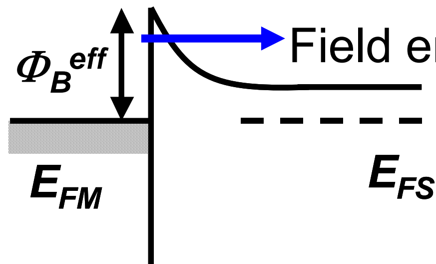
$$R_{sh} \propto \frac{1}{N_{sd} x_j}$$

$$R_c \propto \exp\left(\frac{\Phi_B^{eff}}{N_{sd}^{1/2}}\right), area^{-1}$$

Contact Resistance

Thermionic emission (TE)

Field emission (FE)



$$R_c \propto \exp\left(\frac{\Phi_B^{eff}}{N_{sd}^{1/2}}\right), area^{-1}$$

Doping ↑, R_c ↓

Metal/Ge contact

Φ_B = 0.6eV

0.5eV

0.4eV

0.3eV

0.2eV

0.1eV

0eV

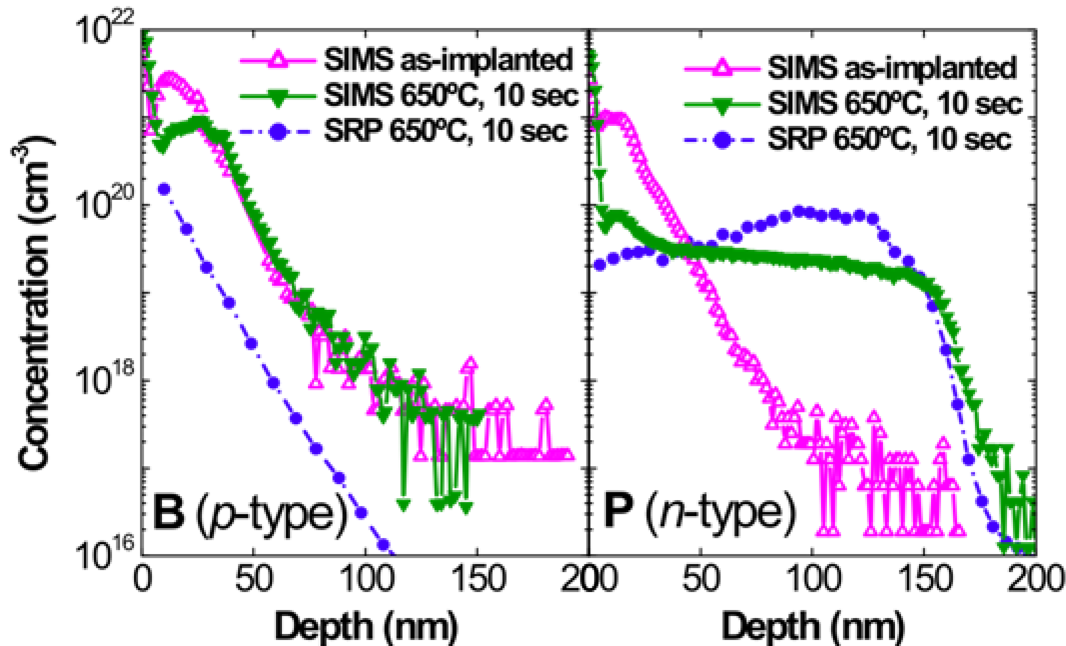
Contact resistance (Ω-cm^2)

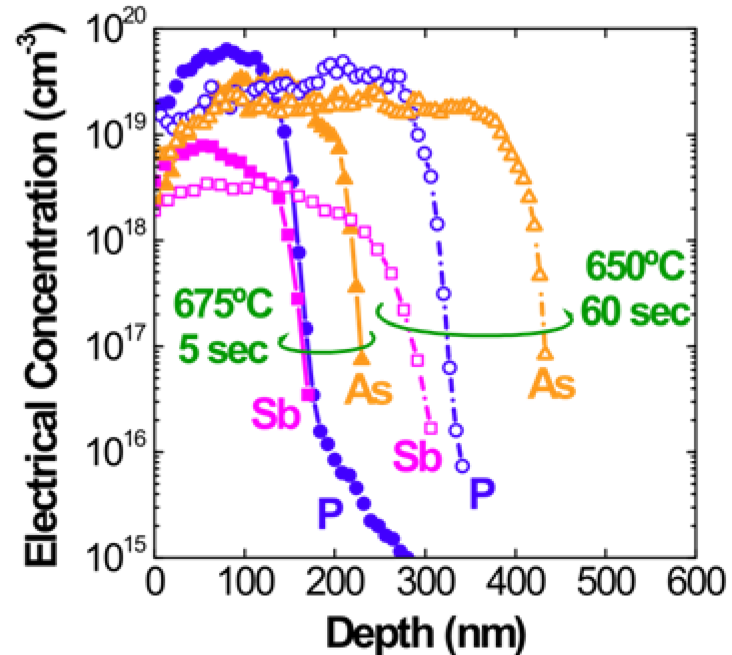
10^4, 10^2, 10^0, 10^{-2}, 10^{-4}, 10^{-6}, 10^{-8}, 10^{-10}, 10^{-12}

Doping concentration (cm^{-3})

10^{18}, 10^{19}, 10^{20}, 10^{21}

Doping in Ge



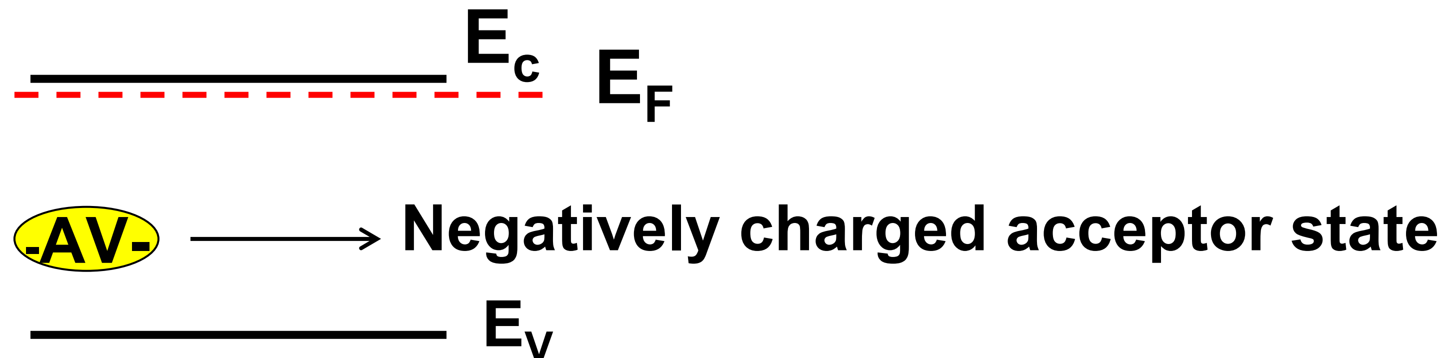


- **P-type dopant (B) has high solid solubility and low diffusivity**
- **Problems with N-type dopants:**
  - Lower solid solubility - High S/D resistance
  - High diffusivity - Shallow junctions??
  - Problems for NMOS

Chui, Kulig, Moran, Tsai and Saraswat, Appl. Phys. Lett., 87, 091909, (2005).

N-type Dopant Activation in Ge

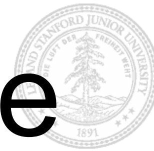
- Ion implantation generates damage in Ge.
- Damage centers form acceptor level defects[1,2]
  - Compensates the donor electrical activation

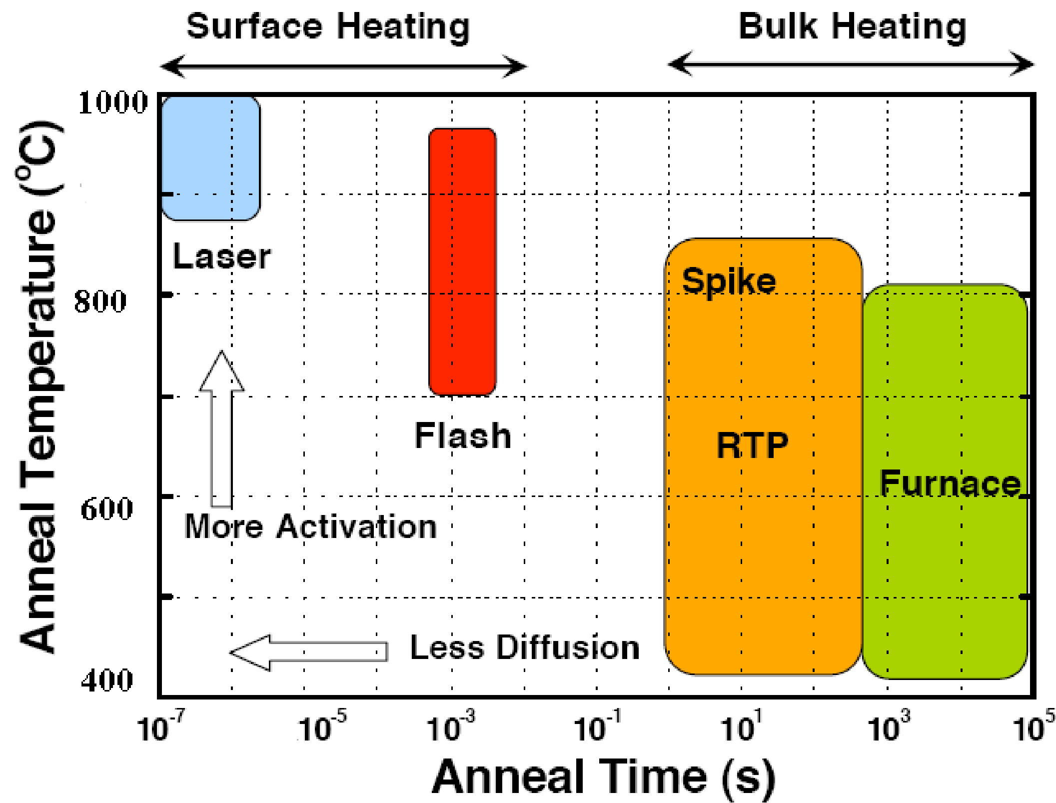


[1] **A. Chroneos et al.,** J. Appl. Phys., 113724, 2008

[2] **V.P. Markevich et al.,** Phys. Rev. B, 235213, 2004

Dopant Activation for USJ in Ge

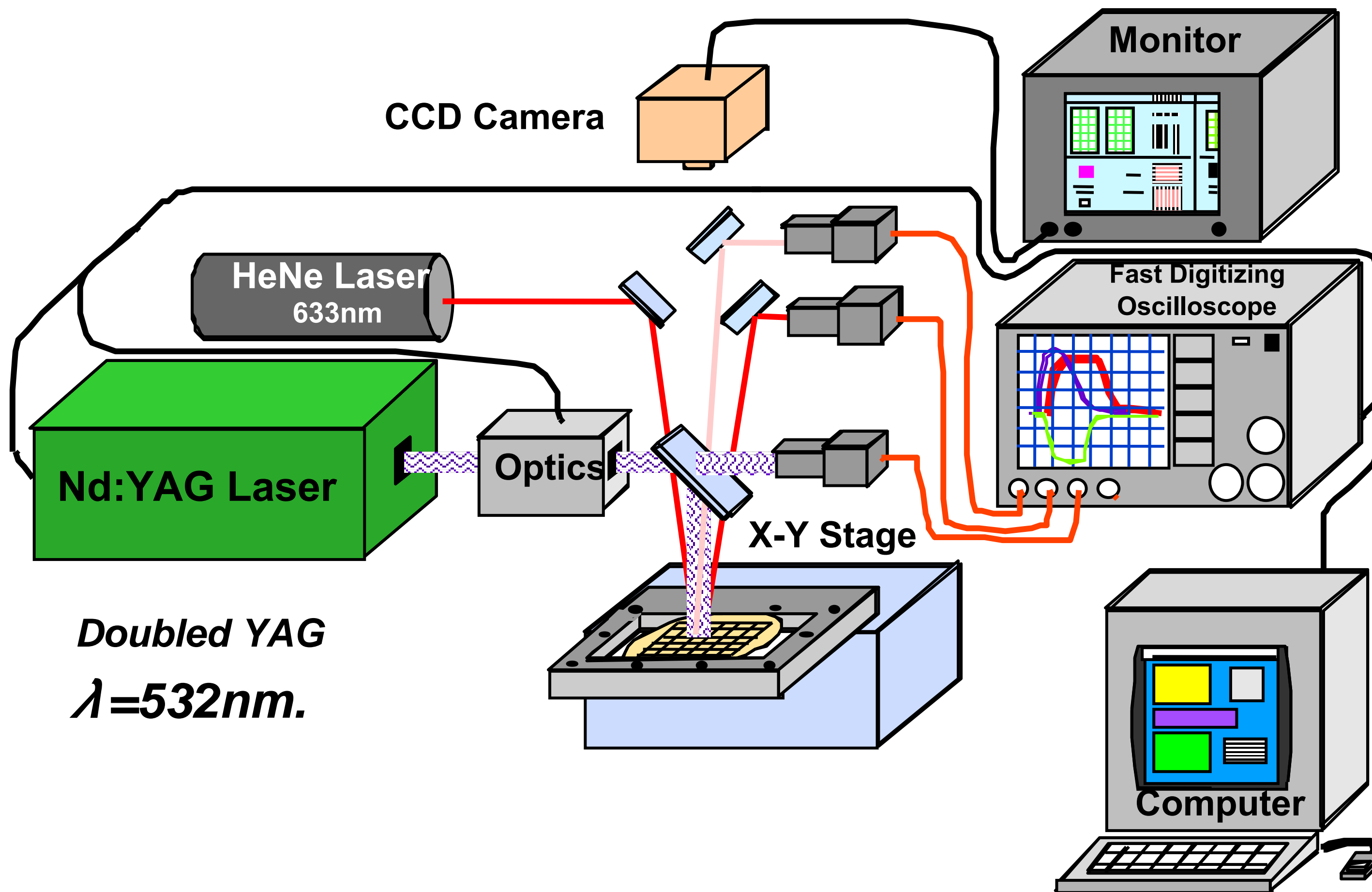




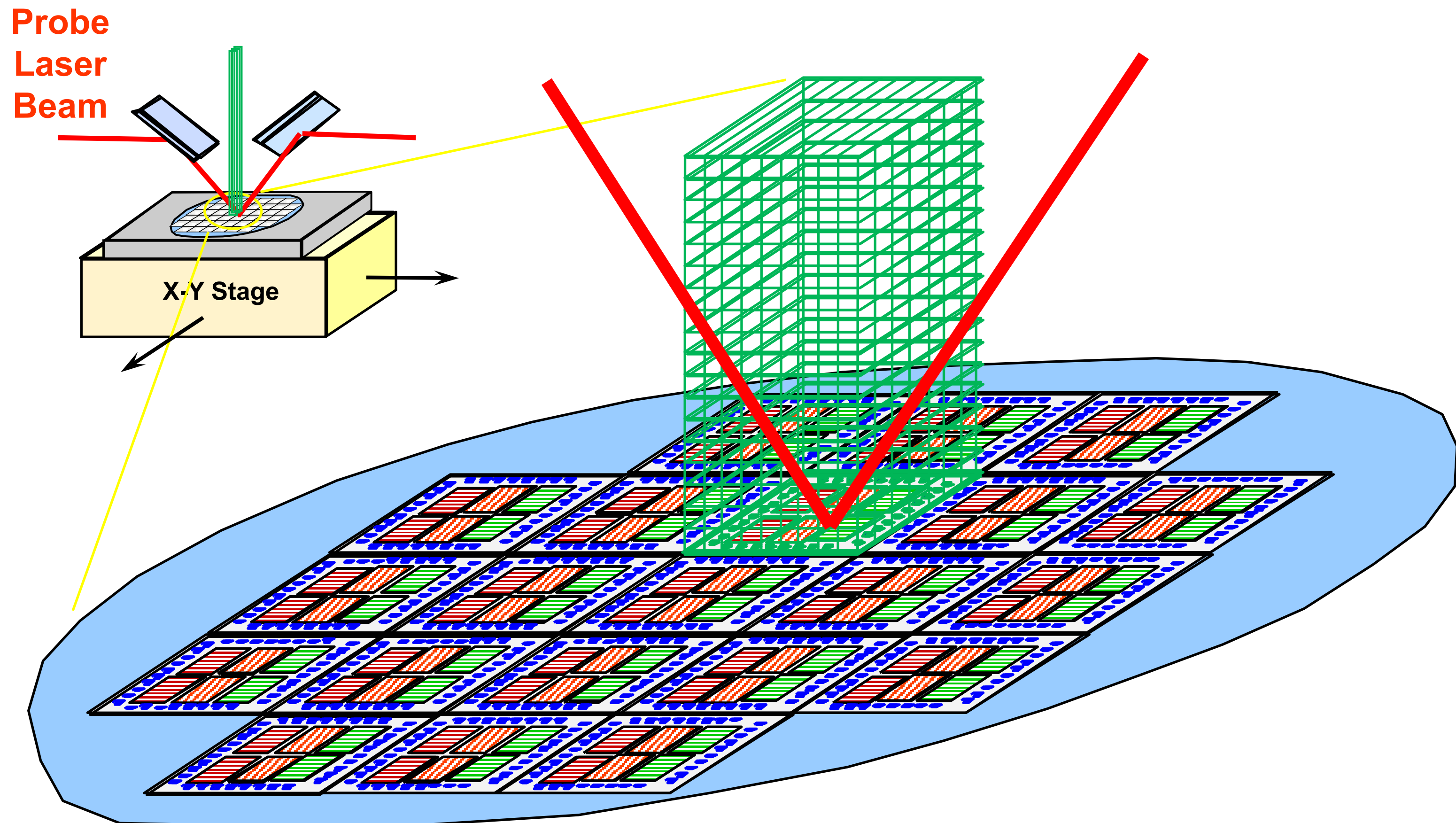
- Laser Thermal Processing (LTP)
  - High dopant activation
  - Reduced diffusion
  - Implantation damage annihilation (Melt – Regrowth)

LTP Setup - I

Main hardware components



LTP Setup - II

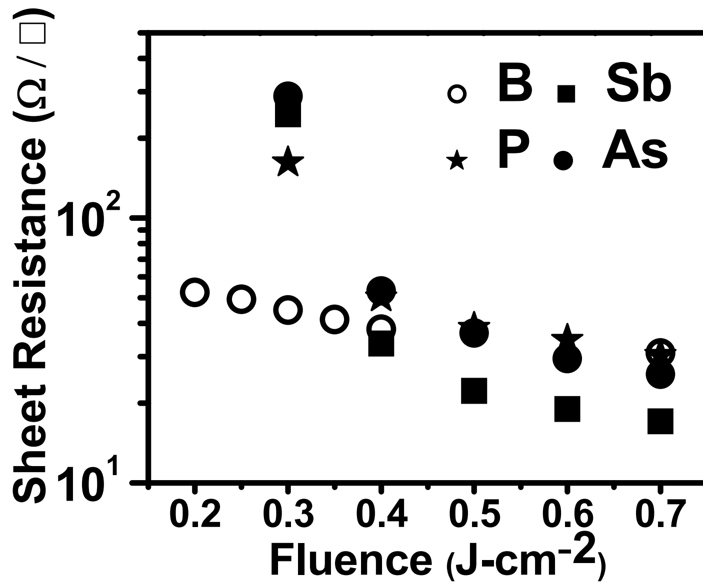


Die by Die Laser Annealing

LTP Parameters

Parameter	**Effect**
Wavelength (λ) [532 nm]	Absorbance and Reflectivity
Pulse Width (t) [10s of nsec]	Annealing fluence threshold
Laser Fluence (J/cm^2) [variable]	Melt Depth

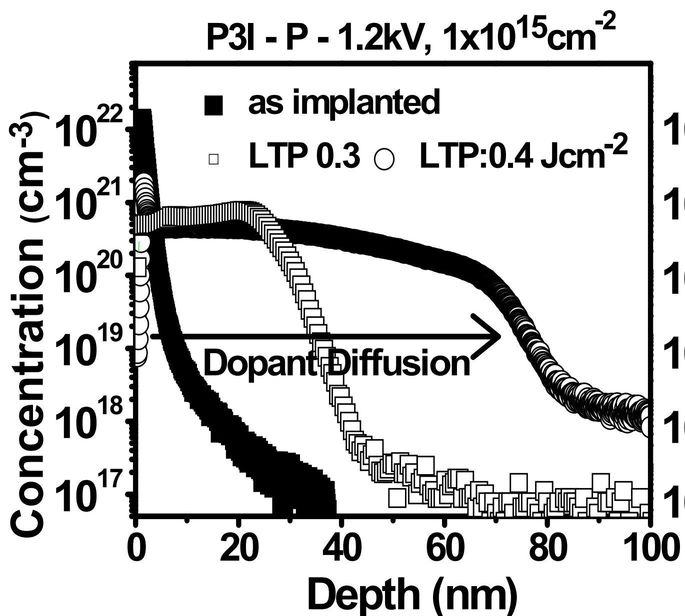
Sheet Resistance & SIMS

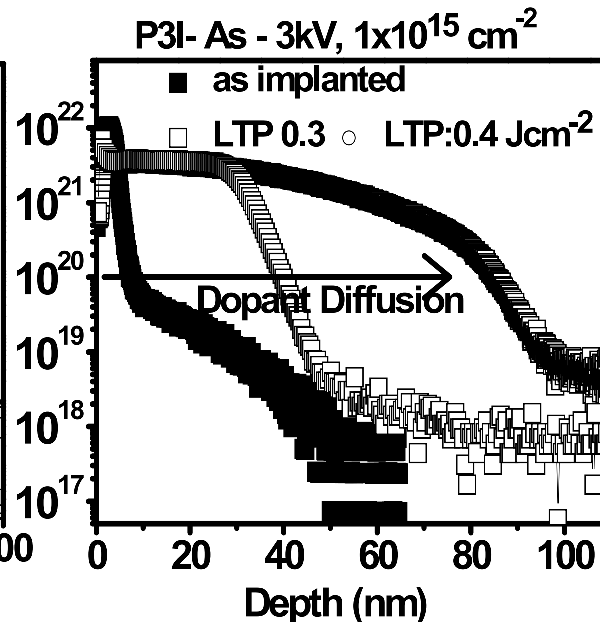


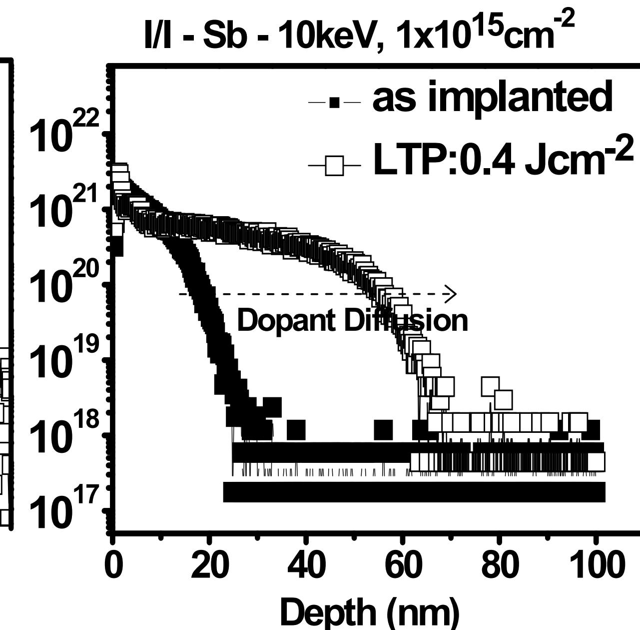
Laser Fluence ↑

Dopant diffusion ↑

Sheet Resistance ↓







Sheet Resistance and TEM

Sheet Resistance (Ω/□)

500
400
300
200
100
0

as implanted

10 nm

Melt initiates
(confirmed
using reflectivity
of HeNe laser)

Polycrystalline films

Low Fluence
Poly Films

5 nm

Melt Penetrates incompletely

Melt Penetrates completely
(Crystalline films)

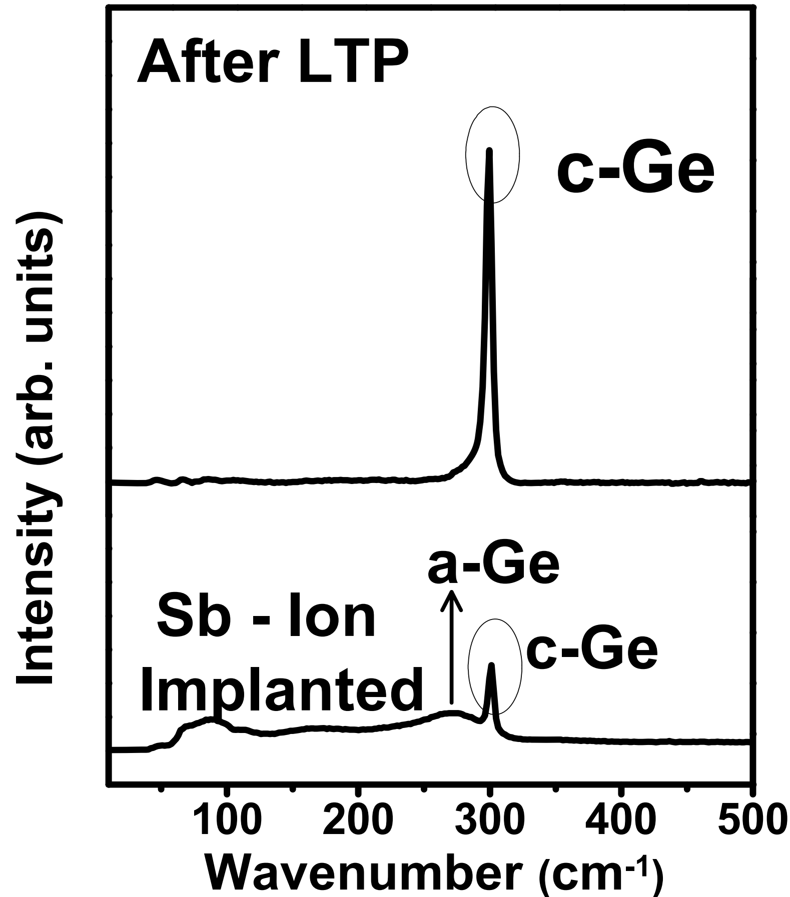
Optimized Fluence

5 nm

0.00 0.15 0.30 0.45 0.60 0.75

Laser Fluence ($J\text{-}cm^{-2}$)

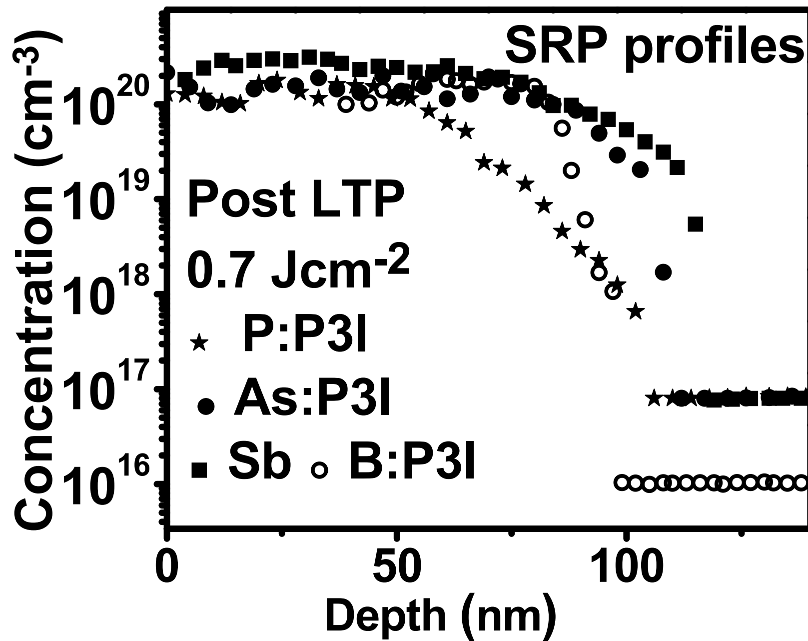
Crystallinity of LTP Junctions



Crystallinity restoration confirmed using Raman

[1] **G.Thareja** et al, IEDM, 2010

Dopant Activation using LTP

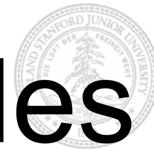


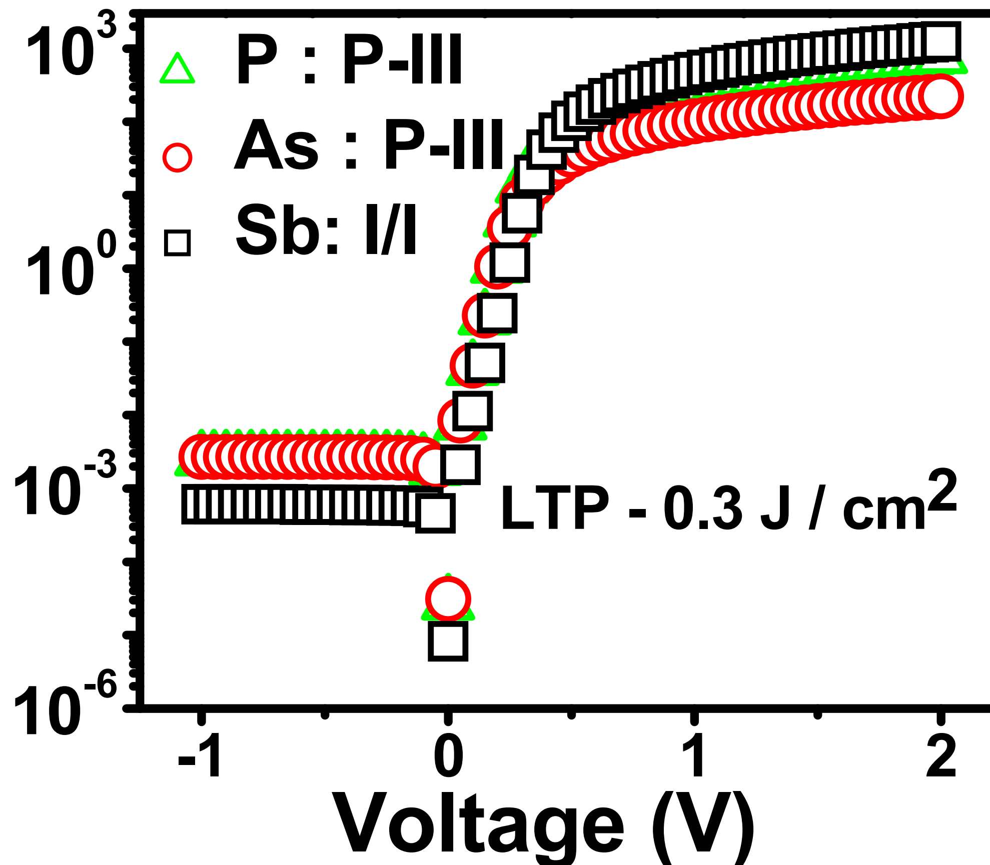
Annealing Technique	Dopant	Electrical Activation (cm^{-3})
Furnace Anneal[1]	P	8×10^{18}
Rapid Thermal Anneal (RTA)[2]	P / As / Sb / B	2×10^{19} / 8×10^{18} 8×10^{18}/ 1×10^{20}
Flash Anneal[3]	P	6×10^{19}
In-situ doping[4]	P	1×10^{19}
This Work (LTP)	P/ As / Sb / B	> 1×10^{20}

Dopant Activation > 1×10^{20} cm^{-3}

[1] D.Kuzum, et al., IEDM, 2009, 453, [2] C.O.Chui, et al. APL, 83, 3275, 2003,
[3] C. Wundisch, et al. 95, 252107, 2009, [4]H.-Y. Yu, et al. 685, IEDM 2009

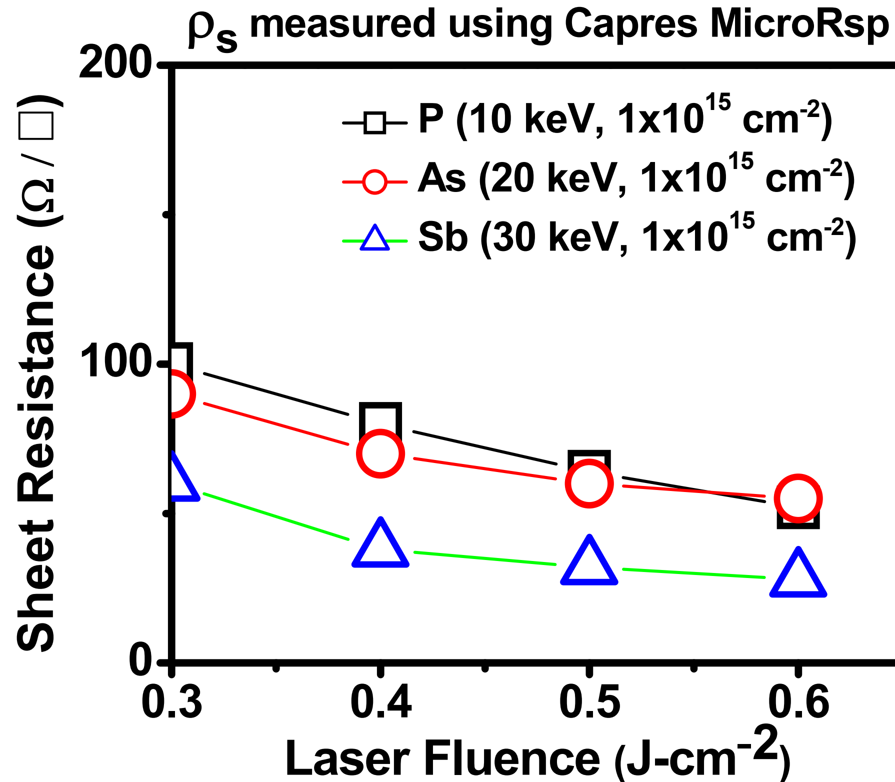
High Performance N^+/P Ge Diodes





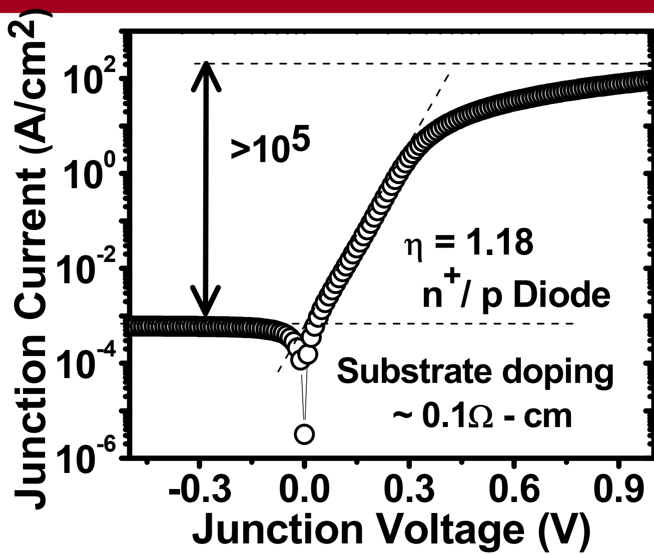
$I_{on} / I_{off} > 1 \times 10^5$, $\eta < 1.2$

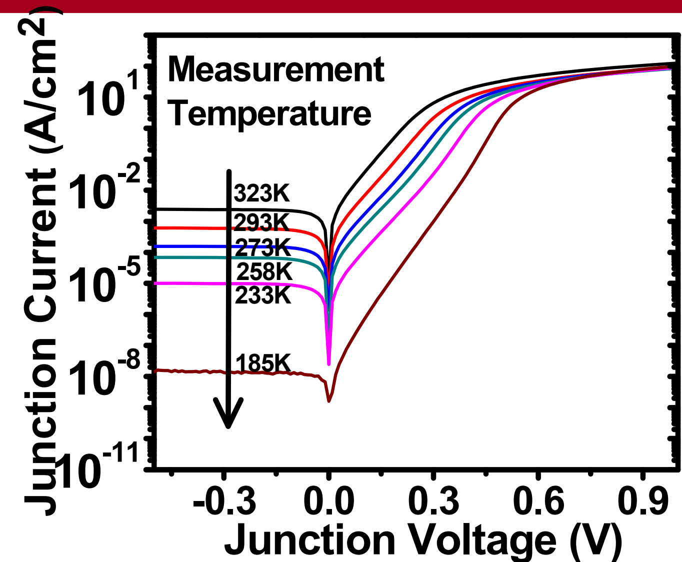
Sheet Resistance, SRP



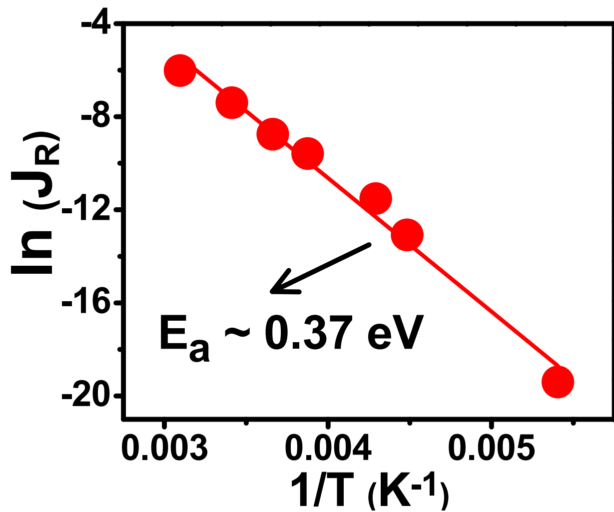
Sb provides the lowest R_s

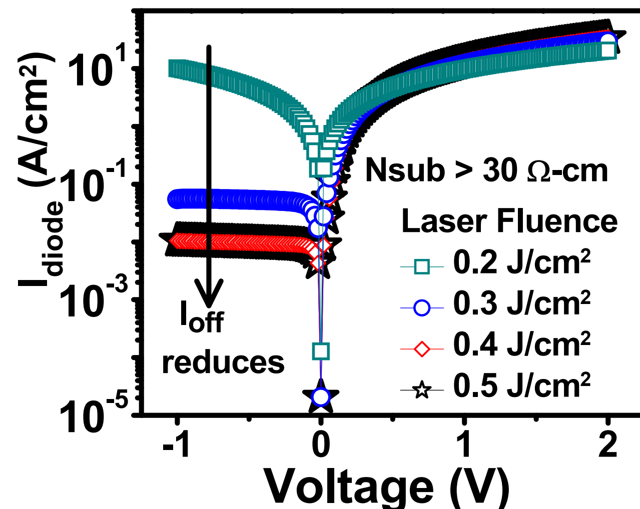
High Performance N^+/P Diode





High I_{on}/ I_{off}, $\eta < 1.2$

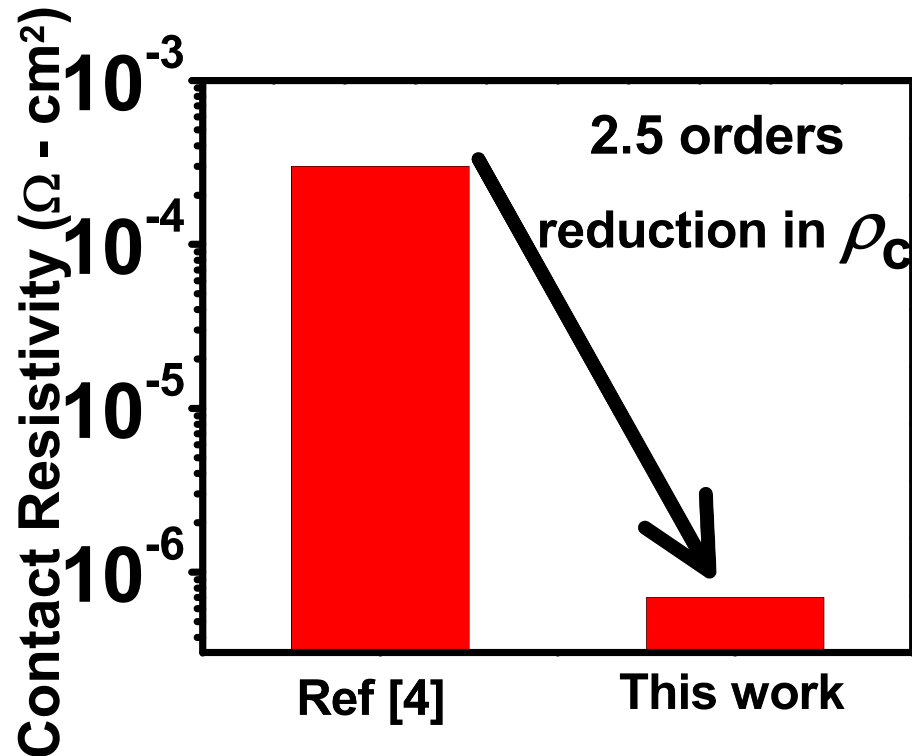


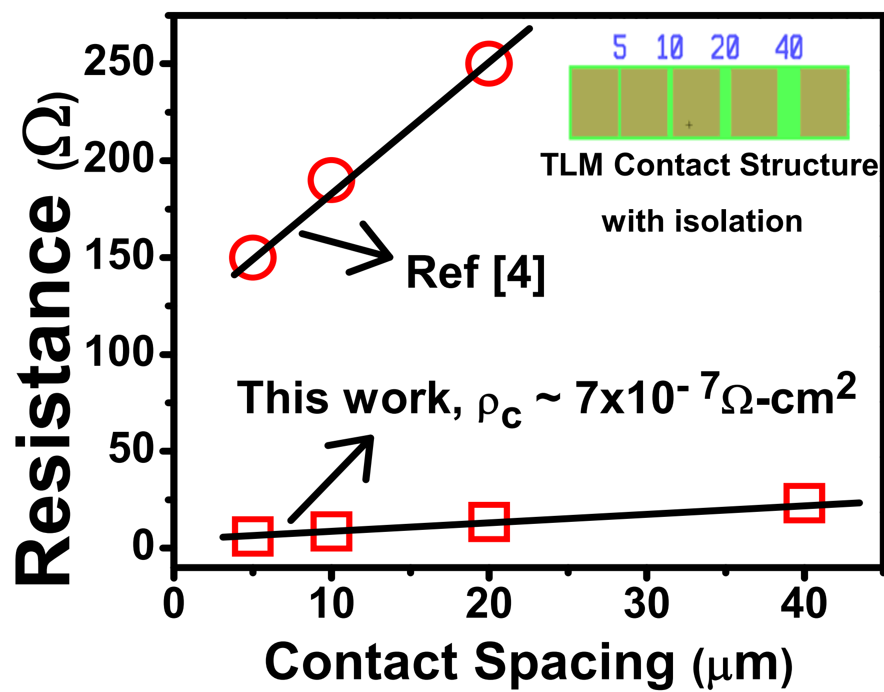


$E_a \sim E_g / 2$, No defect assisted current

Junction formed at 0.5 J/cm²

Contact Resistivity (ρ_c) & Benchmark



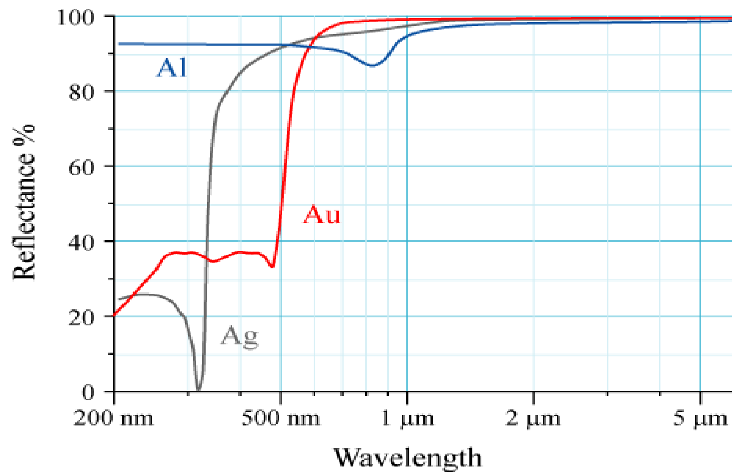


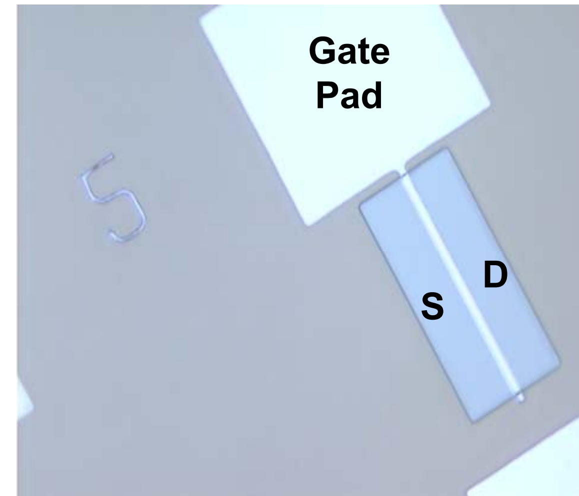
Significant reduction in Metal / N$^+$ Ge ρ_c of 7 x 10^{-7} Ω-cm^2

[4] **J. Oh et al.,** VLSI 2009, p. 238

[1] **G.Thareja** et al, IEDM, 2010

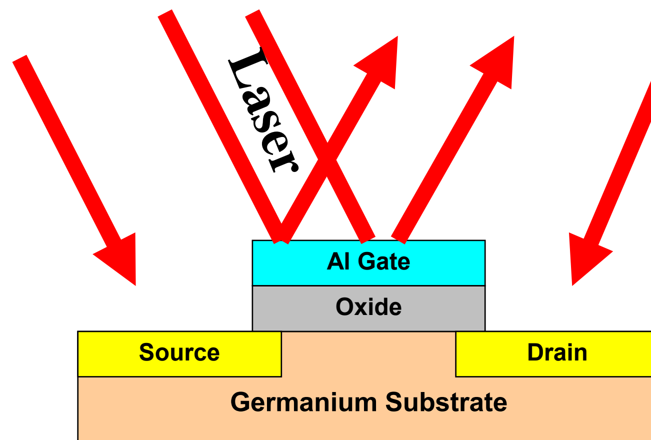
Gate First MOSFET Process





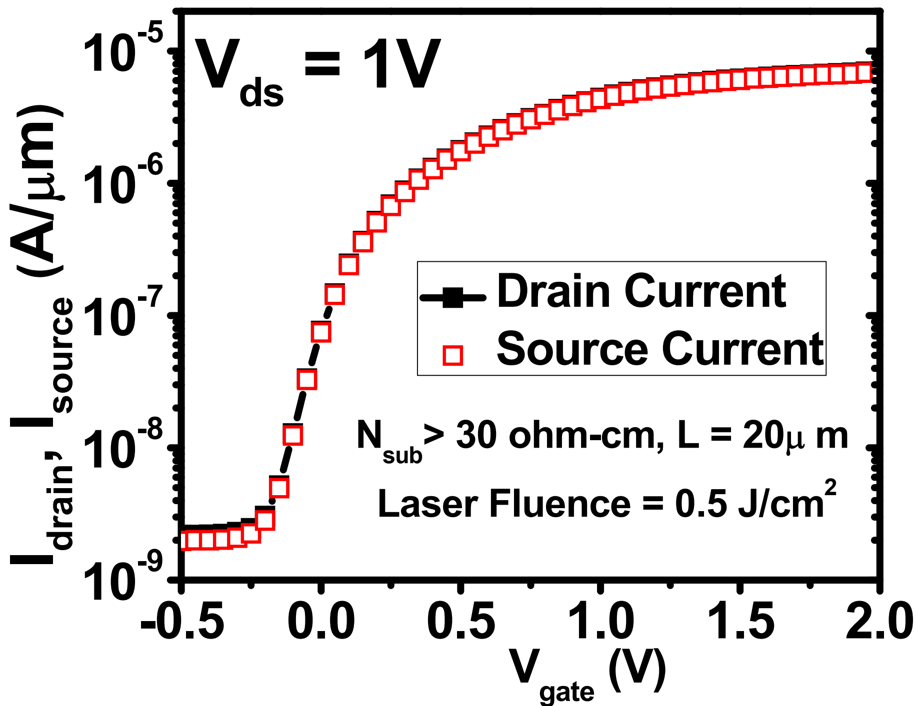
Aluminum (low ψ_m) reflective across a wide wavelength range

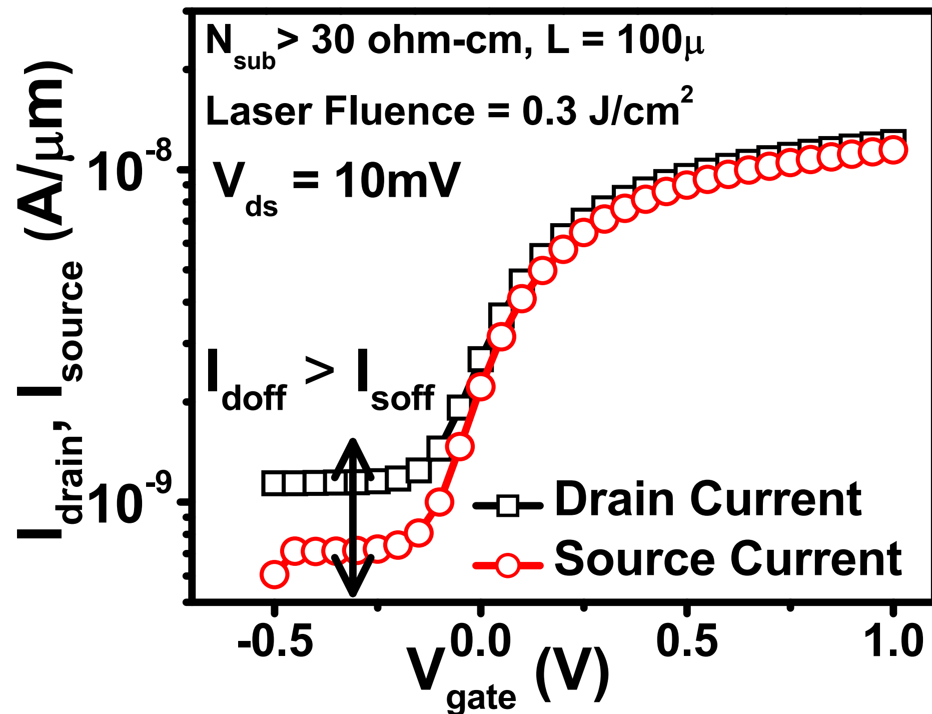
Bright Field Image: Single pulse laser shot
No visible damage effect on transistor structure



[1] **G.Thareja** et al, IEDM, 2010

MOSFET results





Unoptimized laser fluence causes discrepancy between I_{drain} and I_{source} due to high diode leakage

Contributions

- First demonstration of
  - High dopant activation (> $1x10^{20}$ cm^{-3}) using Sb dopants (n-type) in Ge
    - Well behaved n^+/p diodes (I_{on}/I_{off} > $1x10^5$, η < 1.2) and MOSFETs.
    - Lowest contact resistivity for metal(Ti/Al)-n^+ Ge contacts ($7x10^{-7}$ Ω-cm^2)
  - Ultra Shallow Junctions (X_j < 10nm) for Ge
  - Scalable GeO_2 Interfacial Layers (IL) (sub -1nm) for Ge MOS with performance enhancement for Ge NMOSFET
  - Substrate orientation independent growth rate and D_{it} for GeO_2 engineered using SPA oxide

Future Work

- Short channel MOSFETs combining P-III and laser annealing.
- Thermal stability of high dopant activation in Ge
- Alternate methods to obtain high dopant activation
- Reliability analysis of dielectrics for Ge with reduced EOT

Thank you for your time & patience !