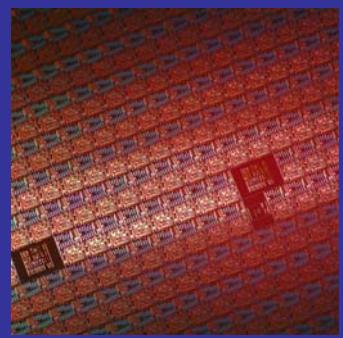
SEMATECH

Accelerating the next technology revolution

Wet Processing Techniques for Achieving Ultra-shallow Junctions in Future CMOS Devices



Joel Barnett, Richard Hill,
Chris Hobbs and
Prashant Majhi

07-October-2010

Outline

- CMOS Scaling Trends and Associated Junctions Challenges
- Challenges, Opportunities and Results for Ultra Shallow Junctions using Monolayer Doping (MLD)
  - Si
  - III-V
- Summary

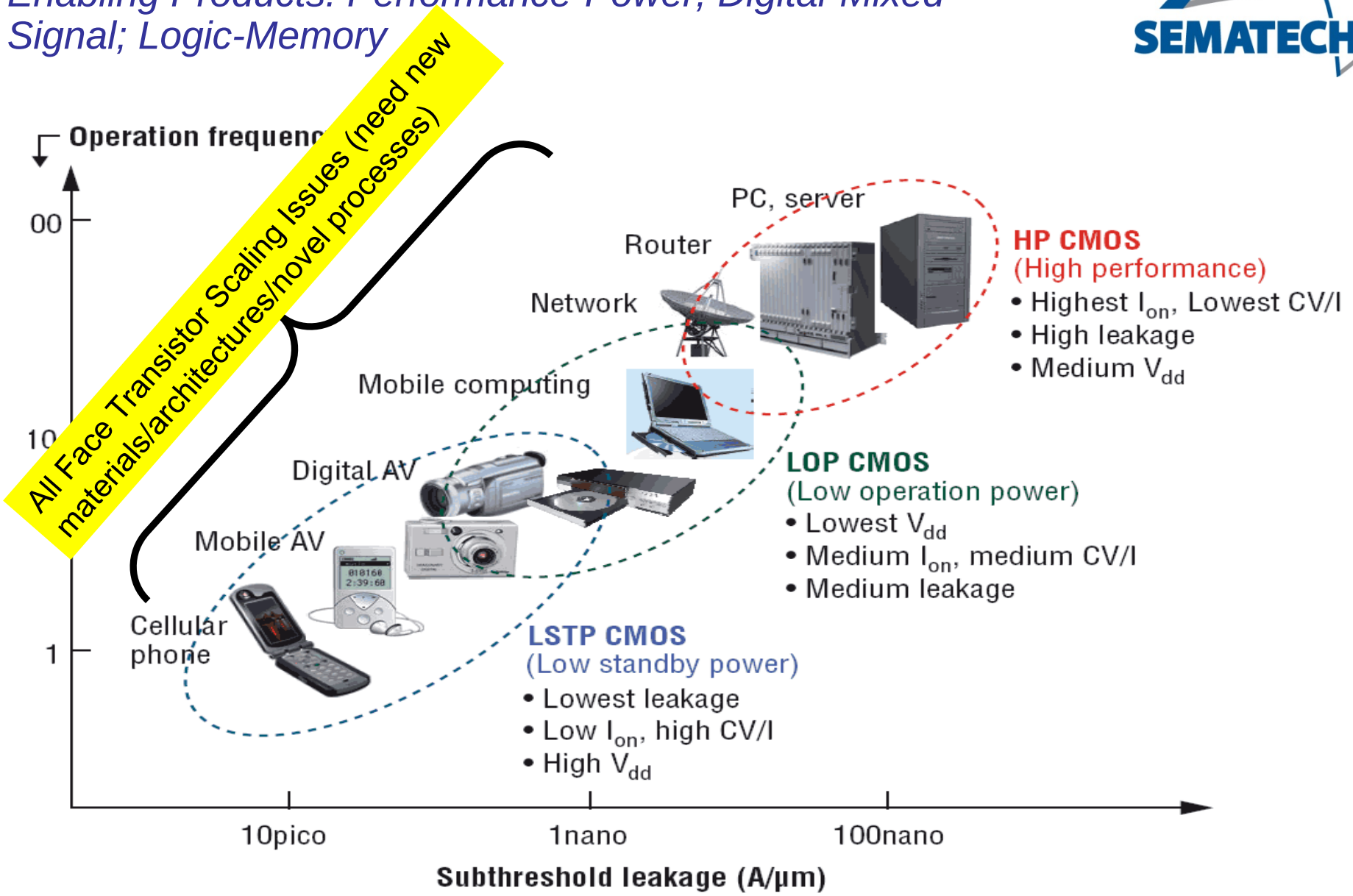
How Is the Industry Changing?

Consumers Demand Low Power with High Performance , Mobile Devices

Source: 1995 Gartner Dataquest; 2009 Semico Research

SEMATECH Front-End Research:

Enabling Products: Performance-Power; Digital-Mixed Signal; Logic-Memory



MOSFET Scaling Trends & Junctions Challenges

Novel Materials and Architectures

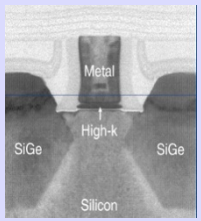
New Mat'l/Structure

2015-2019

planar

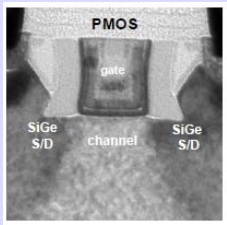
High-K
MG

45nm
2007



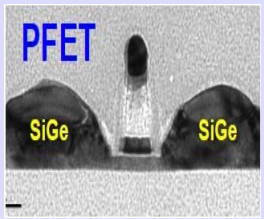
(Production)
Intel IEDM 2007

32nm
2009



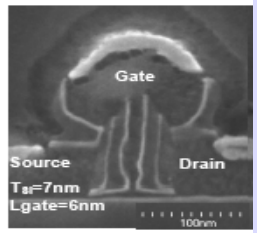
(Production)
Intel IEDM 2009

22nm
2011



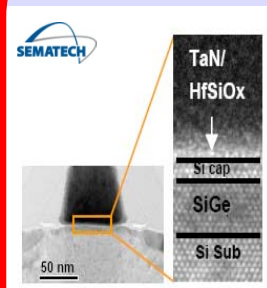
(Development)
IBM, IEDM 2009

16nm (?)
2013

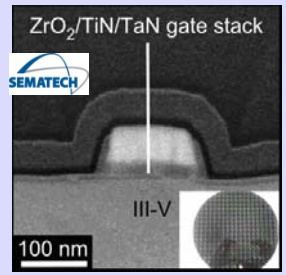


6nm Length
(Research)
B. Doris IEDM 2002

Si-Ge Device



III-V Device



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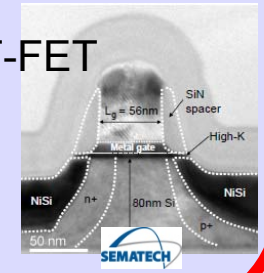
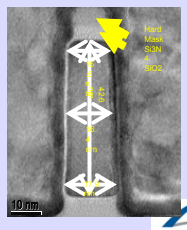
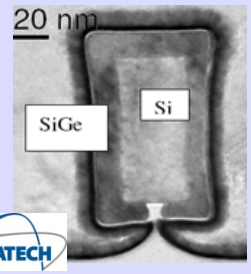
T-FET



Non-planar

FinFET/trigate/Nanowire





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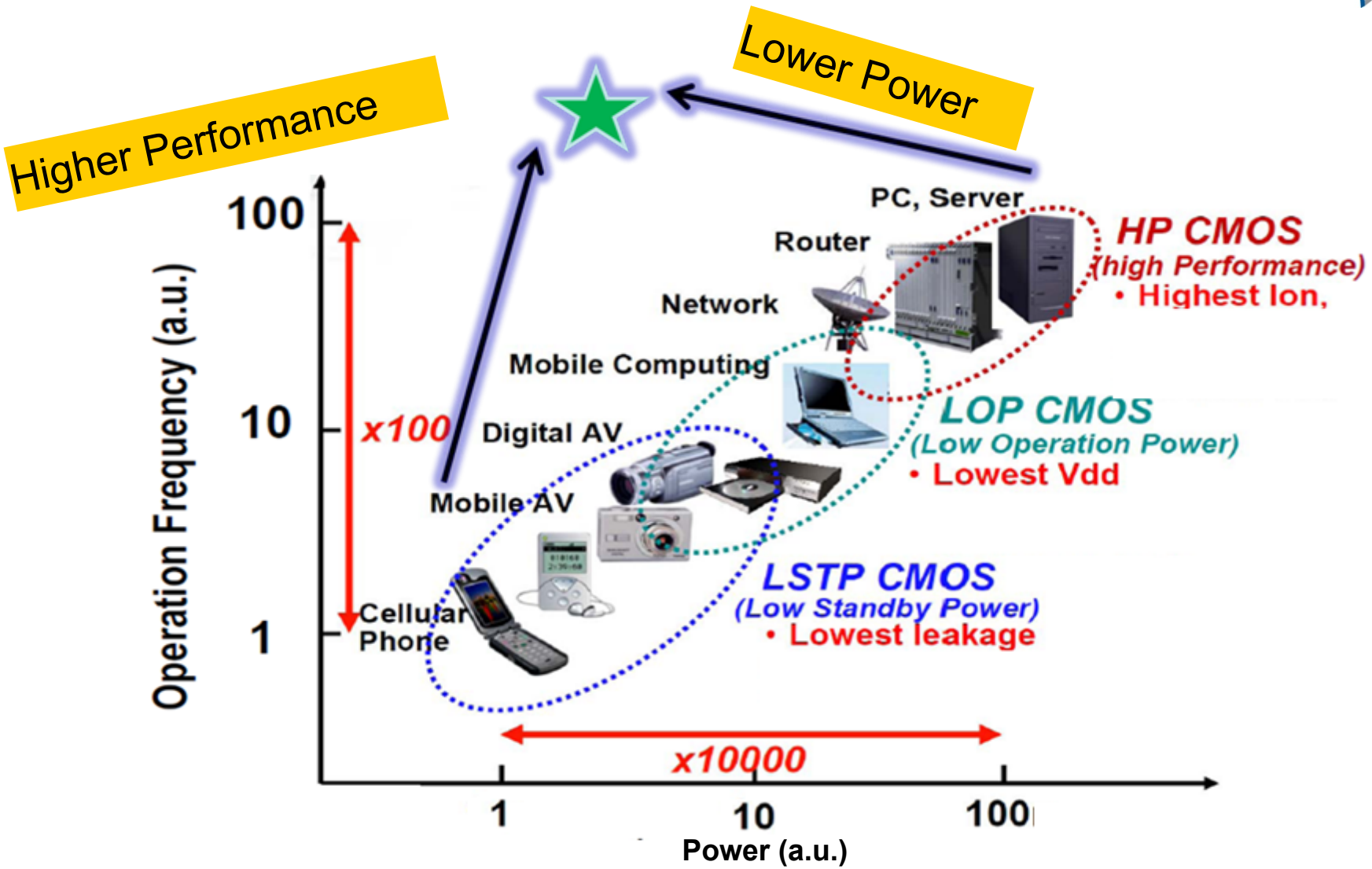
Nano-wire

Need Ultra Shallow and Low Rs Junctions, Control of Short Channel effects

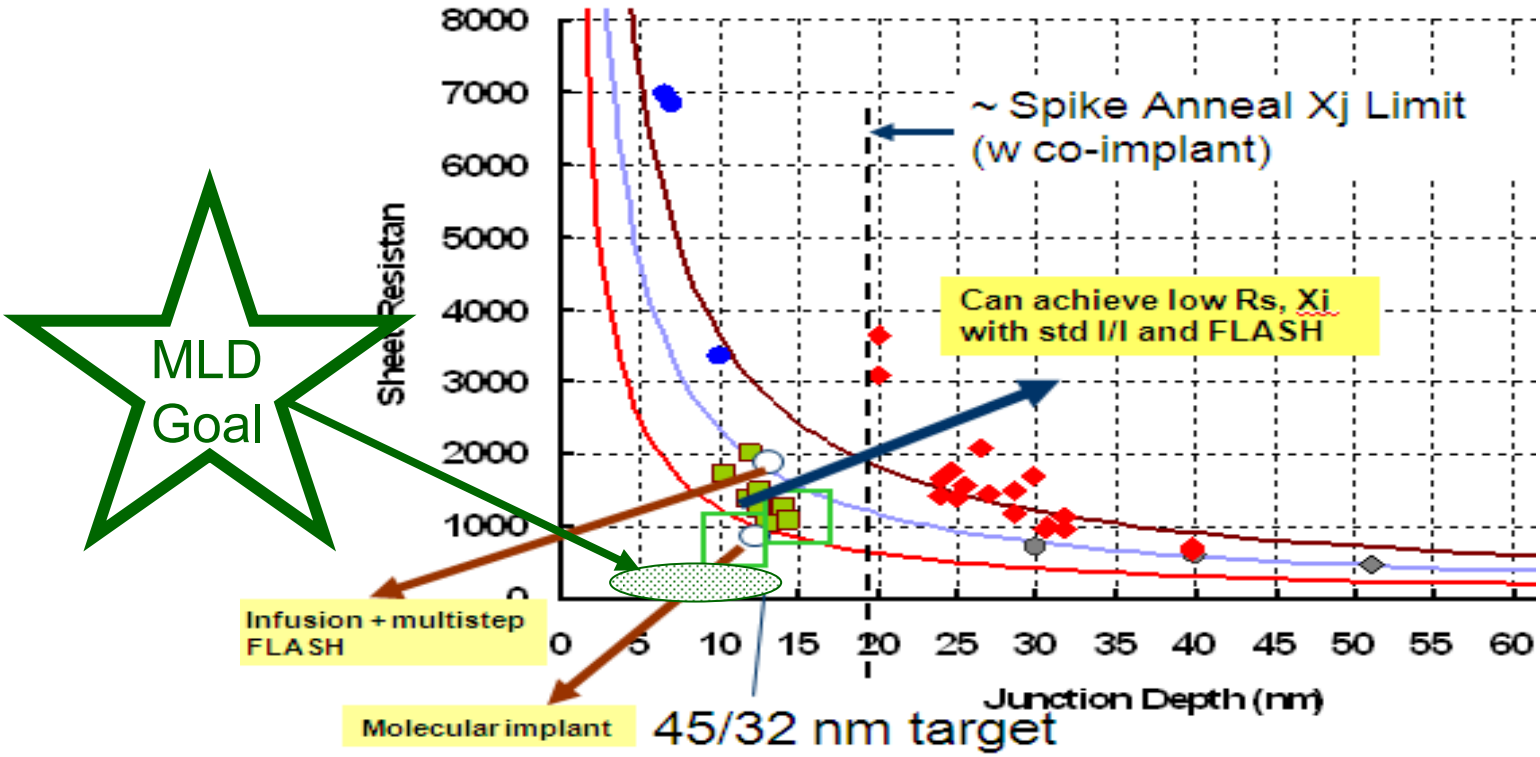
Need Conformal Doping and Low R_{sh}

Need Defect-Free Ultra Shallow and Low Rs Junctions

III-V: Enabling High Performance AND Low Power



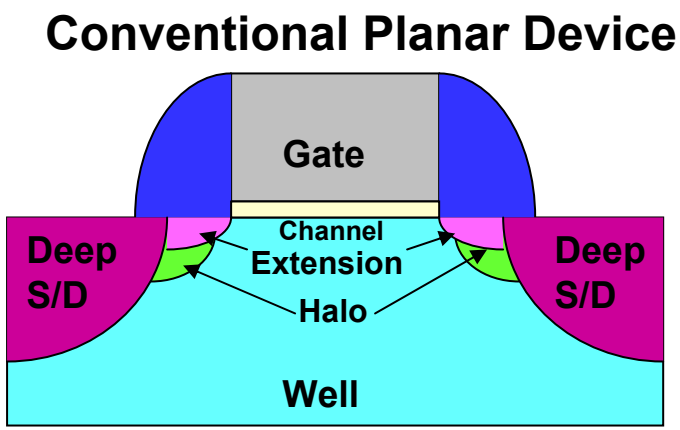
Rs-Xj Benchmark

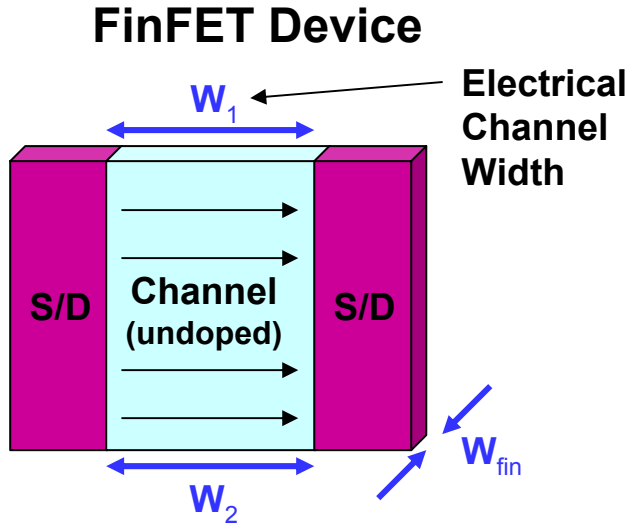


- **MPU/ASIC target is 10 nm (2010) and 9 nm (2012).**
  - **Extension junction depth target is challenging with implant/anneal techniques.**
  - **Must minimize damage to extension**
    - **Impact to junction leakage and junction depth**

MLD and Silicon

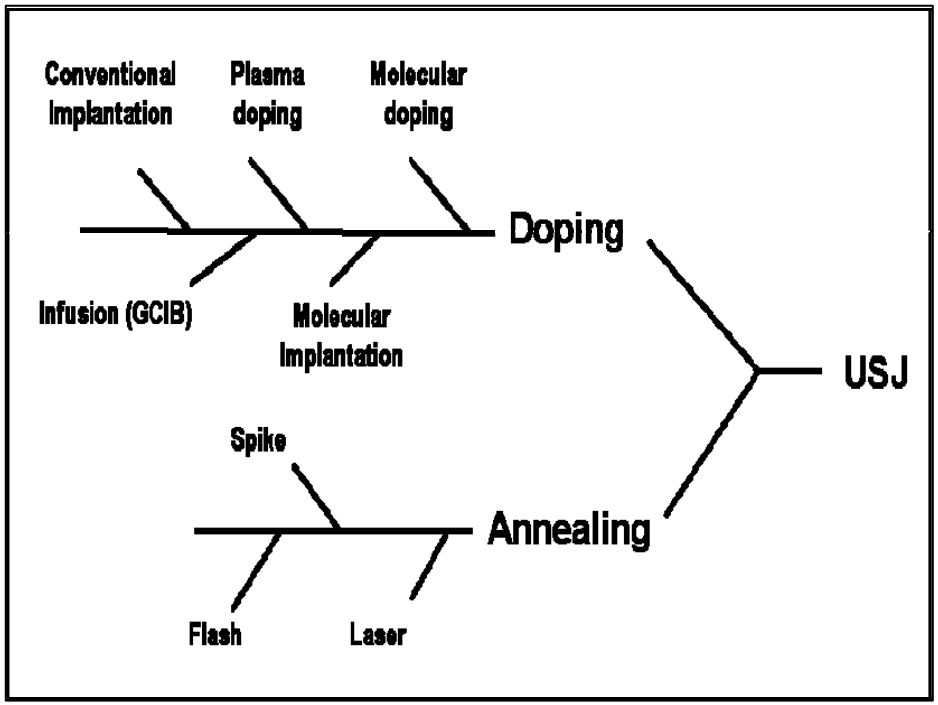
FinFET S/D Junction Formation Needs

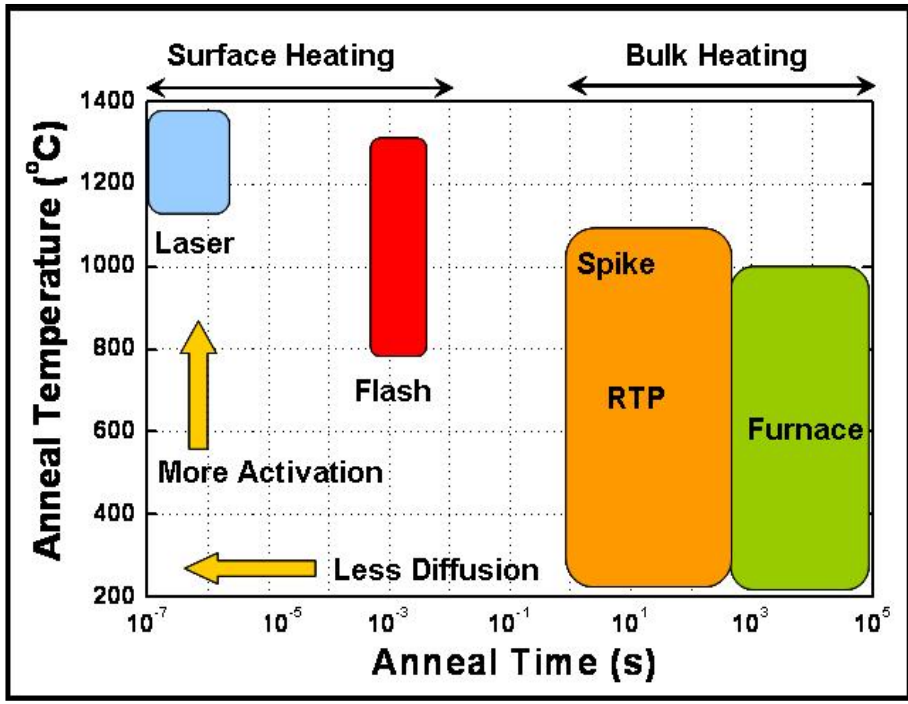




- Planar CMOS:
  - S/D Junction implants results in non-uniform junction profiles.
  - Short channel effects controlled with Halo & Extensions
- FinFET
  - Short channel effects controlled with Double Gate & Small W_{fin}.
  - For device with uniform current flow at top and bottom of fin, $W_1 = W_2$ is needed.
    → Uniform S/D doping in fin needed
  - Achieving uniform junctions with conventional implants on tall fins with short Lg is difficult.
    → Advanced fin doping techniques are needed

Conventional Approaches to Form Low Rs USJ's

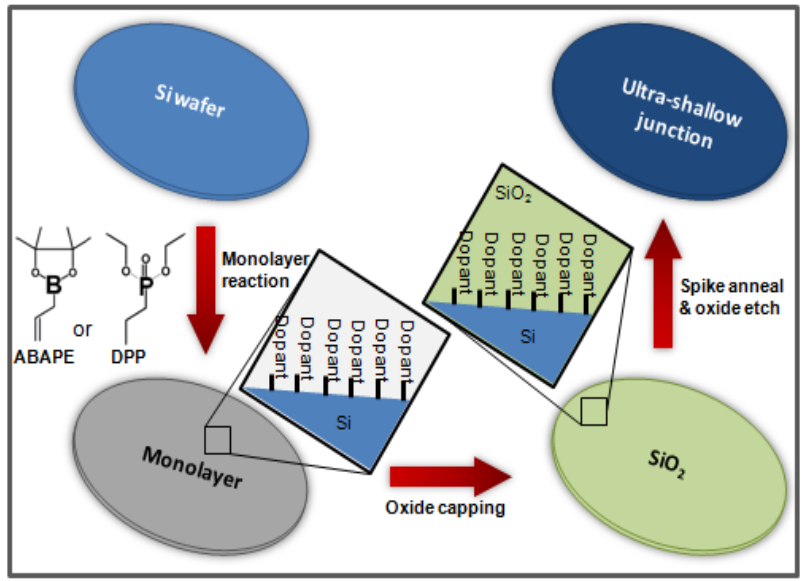


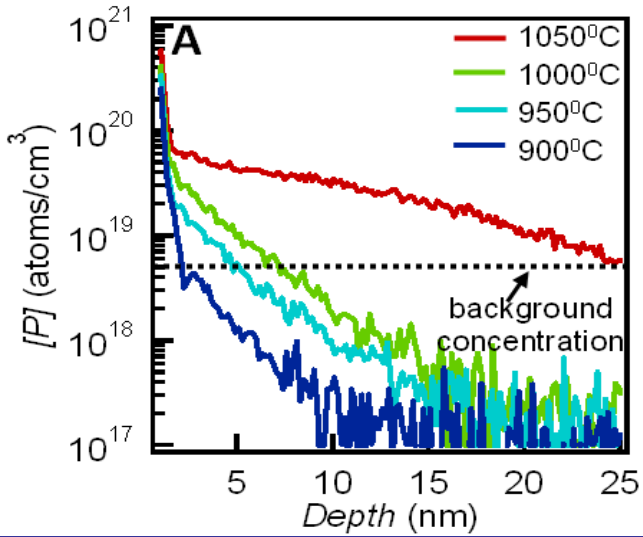


- Advanced doping and anneals are needed for USJ's with low Rs

Ultra Shallow Junctions in Silicon By Monolayer Doping (MLD)

- Extremely Simple Process
  1. HF Deglaze to remove native oxide
  2. Chemical Doping
     - Boron or Phosphorous
  3. Oxide Cap
  4. Anneal
  5. Cap Removal





Benefits of Monolayer Doping

- Sub 10-nm junctions achievable
- No implant damage to substrate
  - **Very significant to LSTP and III-V as it is defect-free**
  - **Hence USJ with very low junction leakage**
- Best known method for doping non-planar structures
- Minimal material loss associated with post implant clean-up
- Lower equipment and processing costs

- Applicable to various substrates (Si, SiGe, Ge, III-V)
- Long roadmap envisioned for MLD

UC Berkeley MLD Process for Si Substrates

http://nano.eecs.berkeley.edu/publications/MLD_NatureMat_2008.pdf

- Si wafers are treated with dilute hydrofluoric acid to remove the native SiO_2.
- The Si surface is then reacted with dopants and mesitylene as a solvent for 2.5 h at 120°C to assemble a dopant-containing monolayer.
- SiO_2 is electron-beam evaporated as a cap
- The substrate is spike annealed between 900-1050°C in Ar ambient to drive in the atoms and achieve USJs.

MLD of Si: Manufacturing Issues to Address

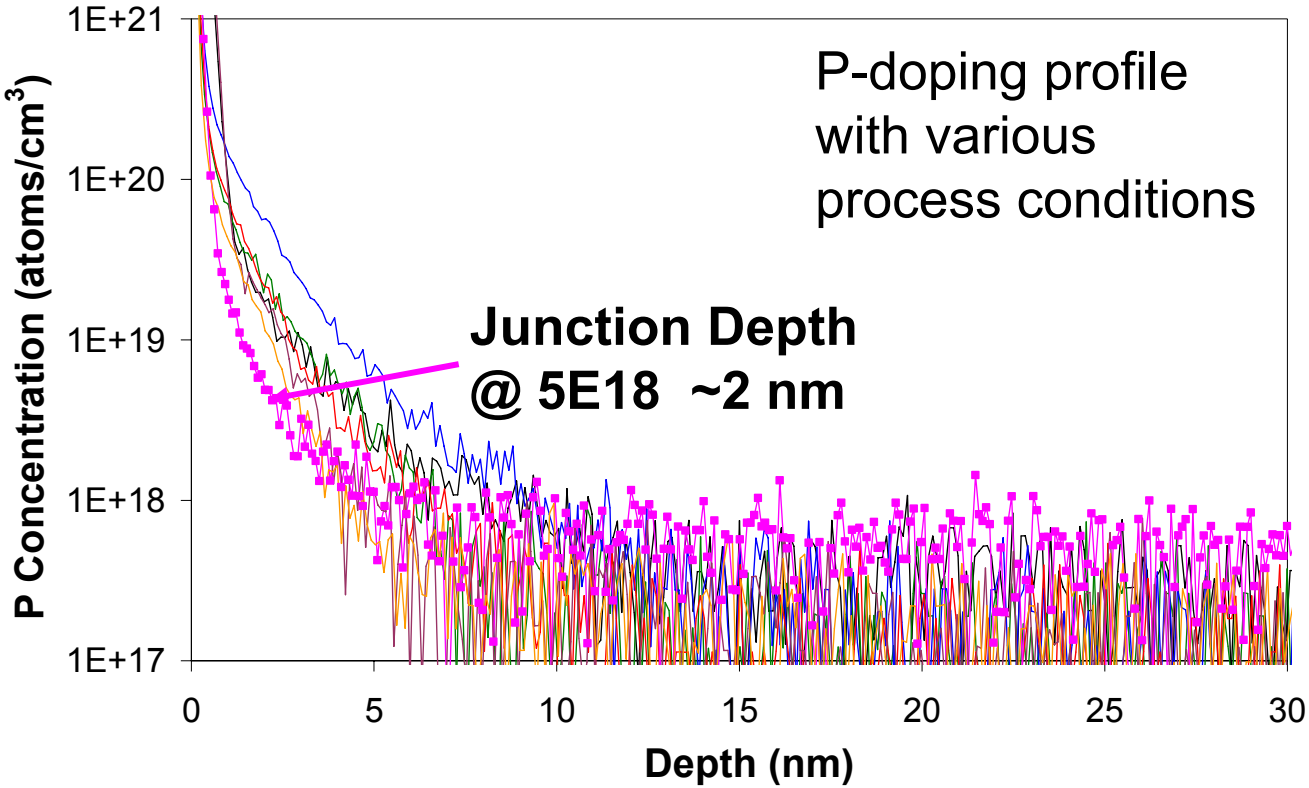
http://nano.eecs.berkeley.edu/publications/MLD_NatureMat_2008.pdf

- Mesitylene solvent Process: 2.5 hours @ 120°C
- Mesitylene Boiling Point (BP) is 140°C / Flash Point (FP) is 44°C
  - University work carried out in a glove box with a dry N_2 environment, and all reactions performed under argon bubbling to ensure an oxygen-free environment
- Semiconductor industry disinclined to run potentially explosive process
  - Major equipment manufacturers have declined running demonstrations with Mesitylene
- Will require integration to properly implement masks to differentiate n and p junctions
  - Typical photoresist mask will not hold up to solvents
  - Can incorporate oxide mask as part of oxide cap process

SEMATECH Plans/Progress for USJ of Si

- Reengineer process to be safer
  - Raise solvent FP
  - Lower Process Temperature
- Requirements for alternative solvent
  - Aromatic
  - Small molecular structure
  - No ligand exchange during reaction
- Requirement for reaction process
  - Process Temp ⇩ Process Time ⇧

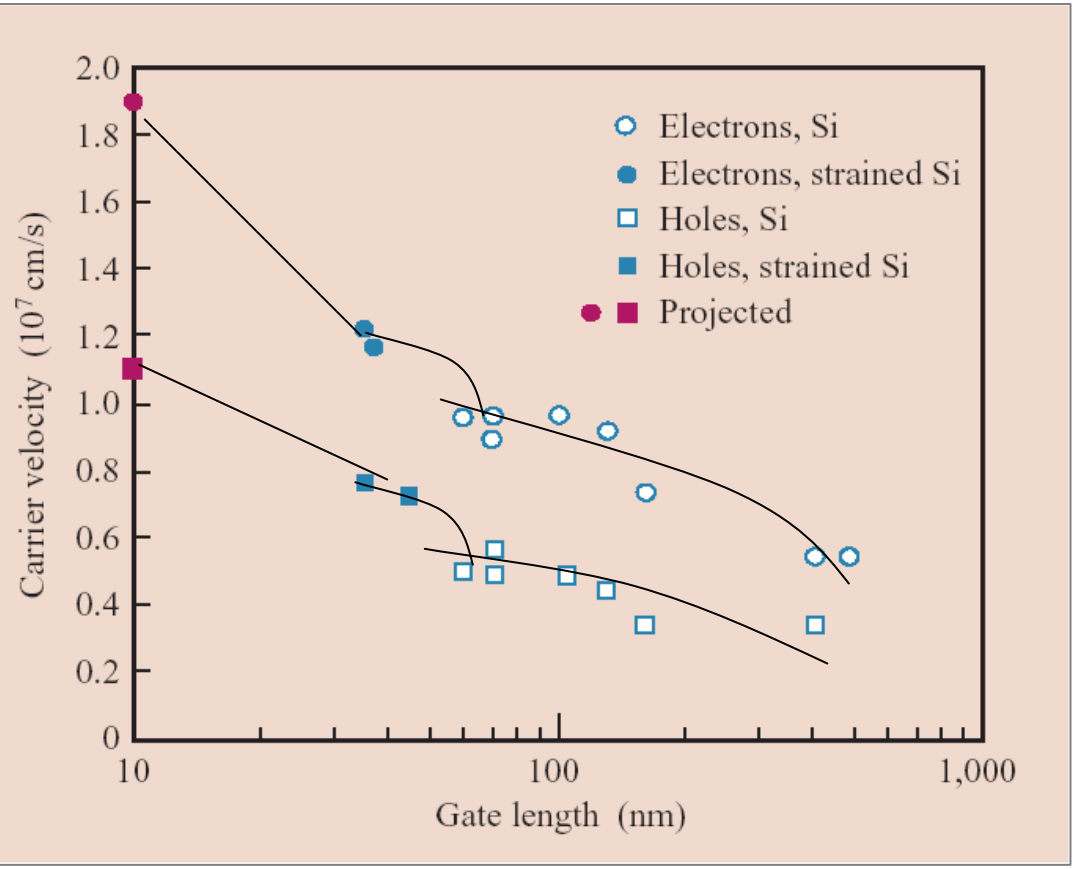
P-Doping Demonstration Results



- MLD Process run in purged glove box @ supplier site with alternative solvent
- Capped with SiO_2 at SEMATECH
- Spike annealed in N_2

MLD and III-V

High Mobility for High Performance at Low Power



- For L_G<20nm, carrier velocity may be ballistic
- Note: $v \sim 1/\sqrt{m^*}$
- And: $\mu \sim 1/m^*$
- Therefore: $\mu \sim v_\theta^{\,2}$
  - Assume τ constant
- Which implies:
  - Channel mobility μ~16x r-Si (~3500 cm^2/Vs)
  - Not demonstrated for s-Si
  - New channel material with adequate *surface* channel μ
  - For example: GaAs requires 2-3x$\rightarrow$ μ ~10^4

After: D. Antoniadis, IBM J. Res. Dev (2006)

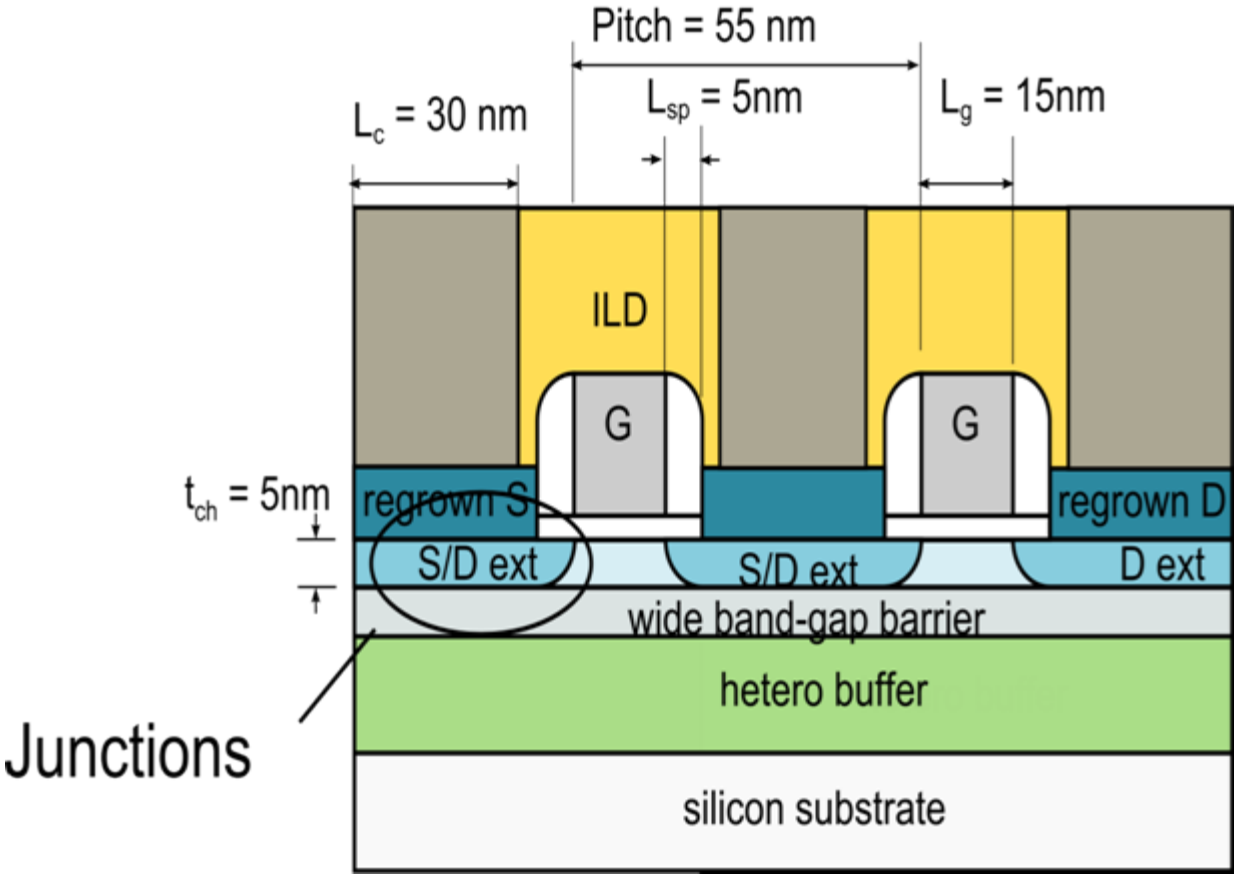
High mobility channels (Ge, III-V based) provide for high performance (Ion) AND low power (Vcc scaling)

Properties of Promising High Mobility Materials [Electrons and Holes]

Property/ Material	Si	Ge	GaAs	$In_{0.53}Ga_{0.47}As$	InAs	Graphene
Eg (eV)	1.1	0.66	1.4	0.75	0.35	0*
μ_n (cm^2/v-sec)	1,350	3,900	4,600	>8,000	40,000	>100,000
μ_p (cm^2/v-sec)	480	1,900	500	350	<500	>100,000
m^*/m_o	0.165	0.12	0.067	0.041	0.024	<0.01
Lattice mismatch to Si	0	4%	4%	8%	12%	n.A

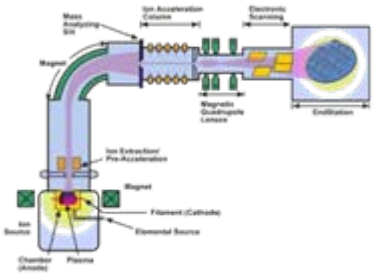
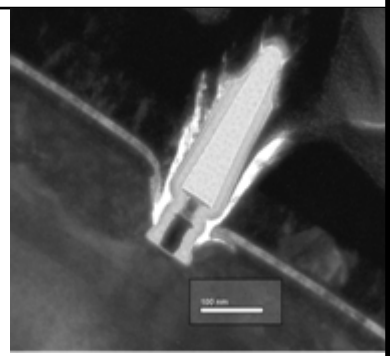
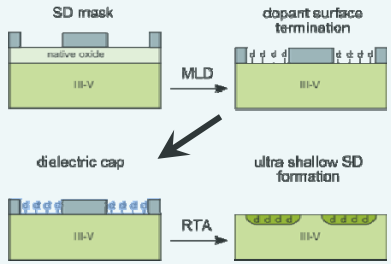
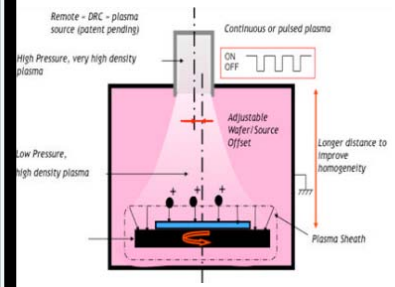
pMOSFET nMOSFET

Parasitic Resistance and Junctions Requirements with III-V



Targets
R_{sh} = 100-200 Ω/sq
X_j = 5 -15 nm
μ = 2500 cm^2/Vs
$n_s = 2.5x10^{13}\ cm^{-2}$
$N_d = 5x10^{19}\ cm^{-3}$
J_j < 0.1A/cm^2
Low defect density $I_{S/D\ leak}$ < 100 nA/μm

III-V Junction options

	Beam line	Epi S/D	MLD	Plasma
				
Pro	• Industry standard process	• High Nd • Abrupt junctions • Zero damage	• Elegant • Zero damage • USJ • Conformal	• Lower damage than beam line. • Low energy for USJ • Conformal
Con	• Damage • Profile • Activation	• Process complexity • Low R_{sh} S/D extension	• Optimization Required • Activation	• Optimization Required

Challenges with III-V USJ Implant/Anneal Options

- Damage in the crystal lattice
  - Leakage of low power transistors
- Accurate placement of dopant profile
  - Currently devices use spike anneals to activate dopant, but unlikely to meet the targets for future generations.
- Accurate placement of dopant due to angle
  - Shrinking wells and device isolation
- Cost
  - Expensive tools, process complexity

SEMATECH MLD Process on III-V Substrates

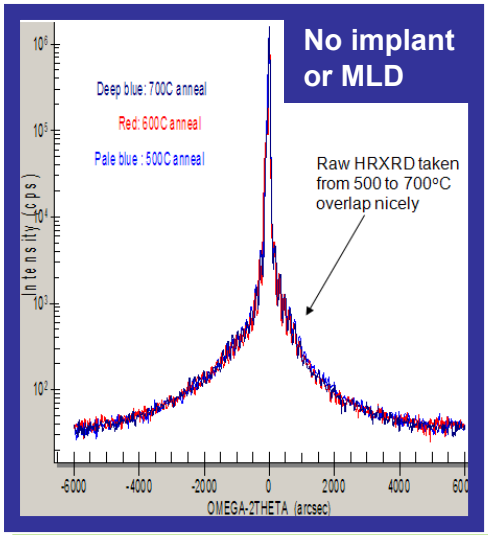
- InGaAs pieces
  - Cleaned with acetone and isopropanol
  - Deglazed in HF
- Placed in an **Ammonium Sulfide solution $(NH4)_2S_x$**
  - Solution is maintained in a water bath at elevated temperature

How does S Passivation Work?

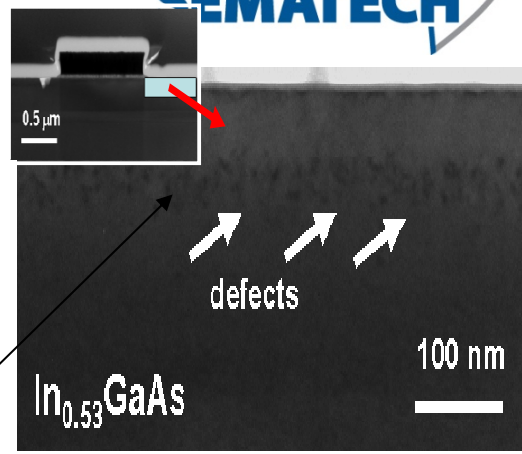
- Two competitive chemical reaction processes occuring
  - $GaAs + S^{2-} \rightarrow GaS + As_2S_3$ sulfides
  - Ga + As sulfides + $H_2O \rightarrow Ga_xO_y + As_xO_y$
- Second reaction is stronger
  - Sulfide layer formed is mostly converted into oxides
  - Oxides are soluble in water.
- One monolayer of S atoms remains on the surface
- The atomic surface density is 5.6Ex14 /cm^2, which represents the maximum areal sulfur dose
  - Assuming a perfect monolayer

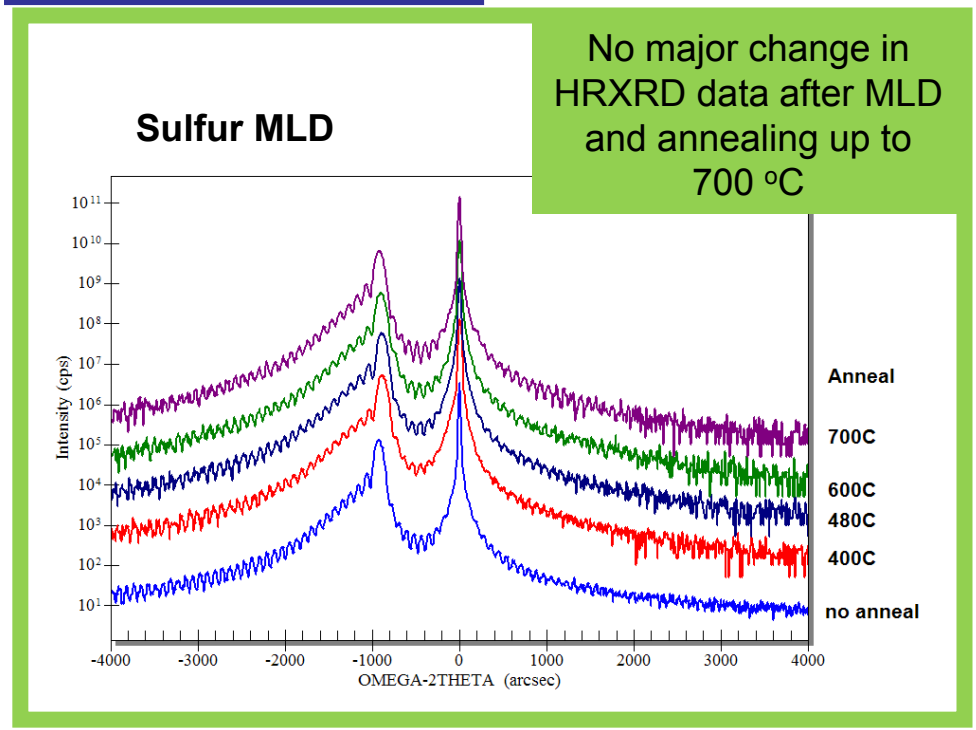
Li J. Appl Phys, 78 (4) 2764 (1995)

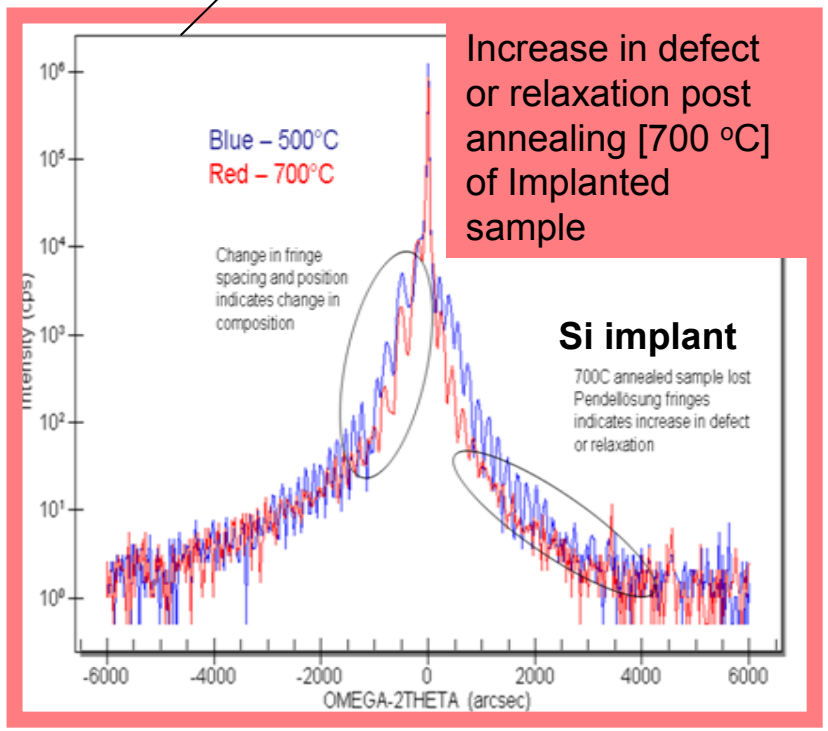
MLD Advantage over Implantation



High resolution X-Ray Diffraction on $In_{0.53}GaAs$/ InP indicates lattice quality deteriorates with high anneal temperature for implanted sample but not for non-implanted or MLD sample

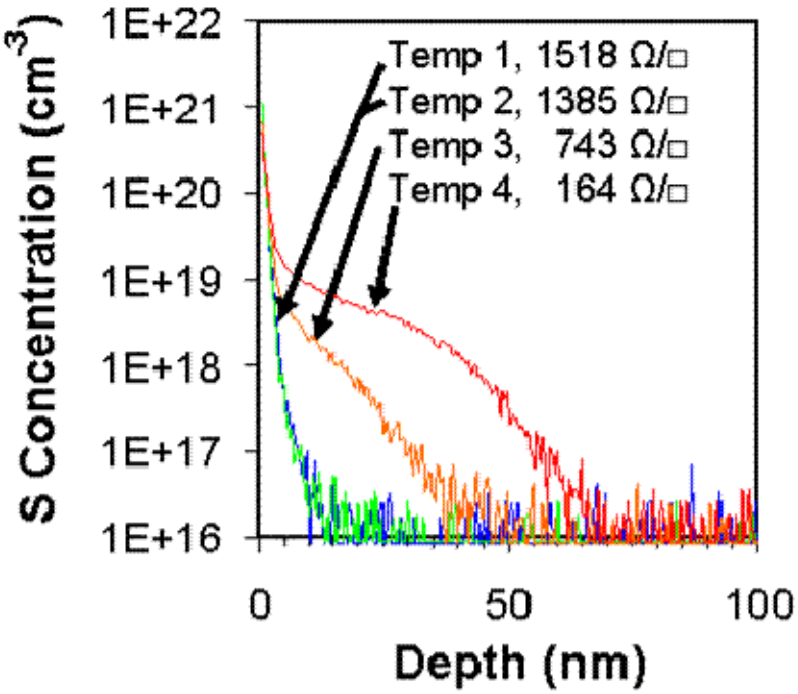






Effect of RTA Temperature

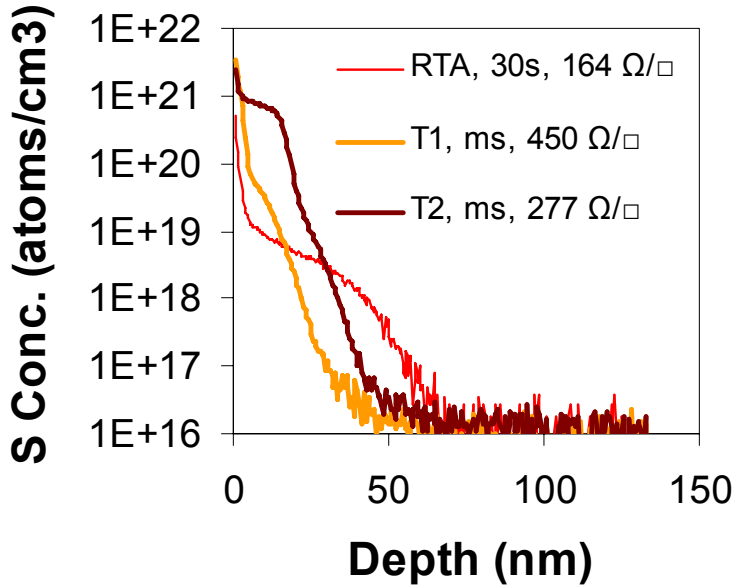
- < 500 ˚C, 30 s
  - X_j < 3nm*, R_{sh} > 1300 Ω/sq
  - Doping profile ~ 1 nm/dec
- > 500 ˚C, 30 s
  - X_j = 9 nm*, R_{sh} = 164 Ω/sq
  - Long diffusion tail



N_d and X_j increase with temperature

Effect of ms-Flash Anneal

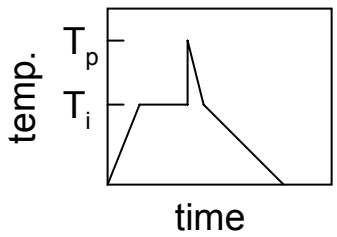
Sample	R_{sh}*	μ*	n*
	Ω/sq	cm^2/Vs	$x10^{12}$ cm^{-2}
$Temp_1$	450	3200	4.3
$Temp_2$	277	1460	15
RTA, 30s	164	2682	14



Ms-flash has higher near surface concentration, but not increased activation, further optimization necessary.

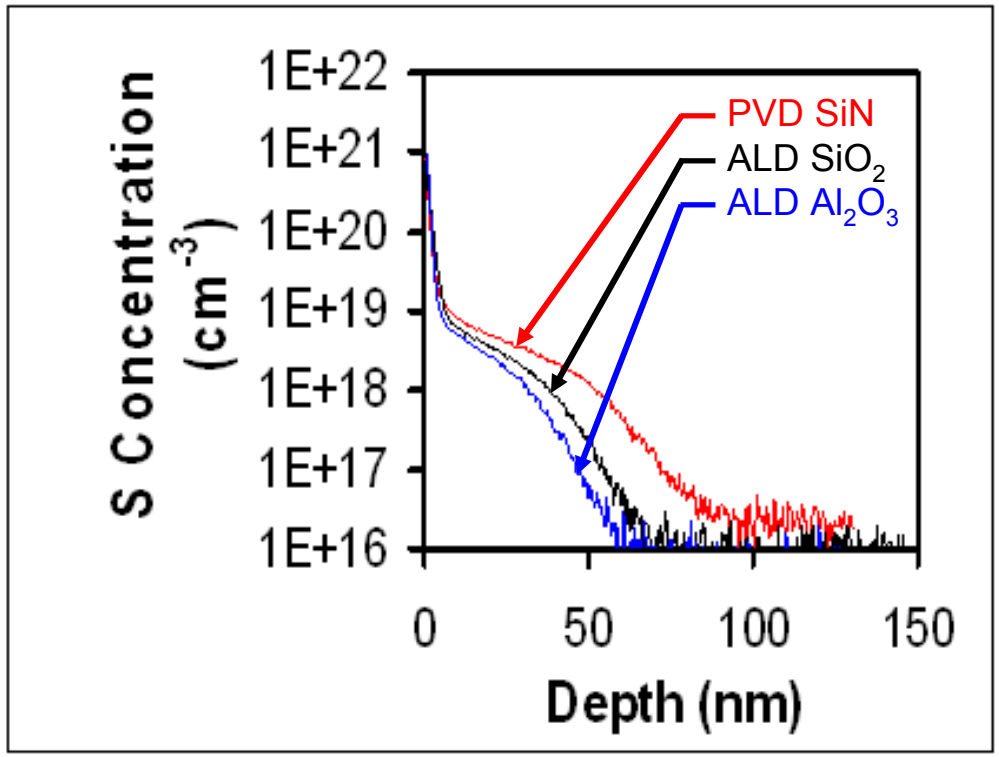
* VdP Hall data. ** Estimated T_p

Ms- flash profile



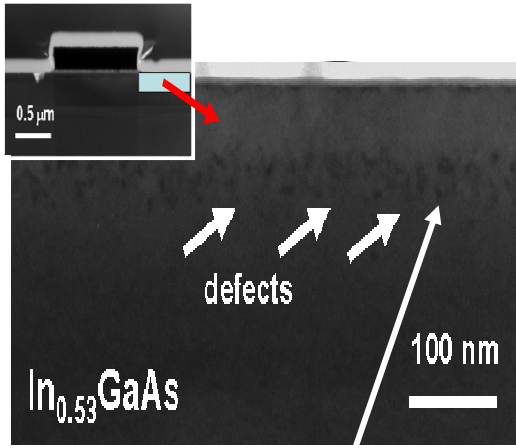
Effect of Capping Layer

- S desorbs at temps ≥ 250 °C
- Cap type influences S incorporation
- Attributable to temperature of deposition

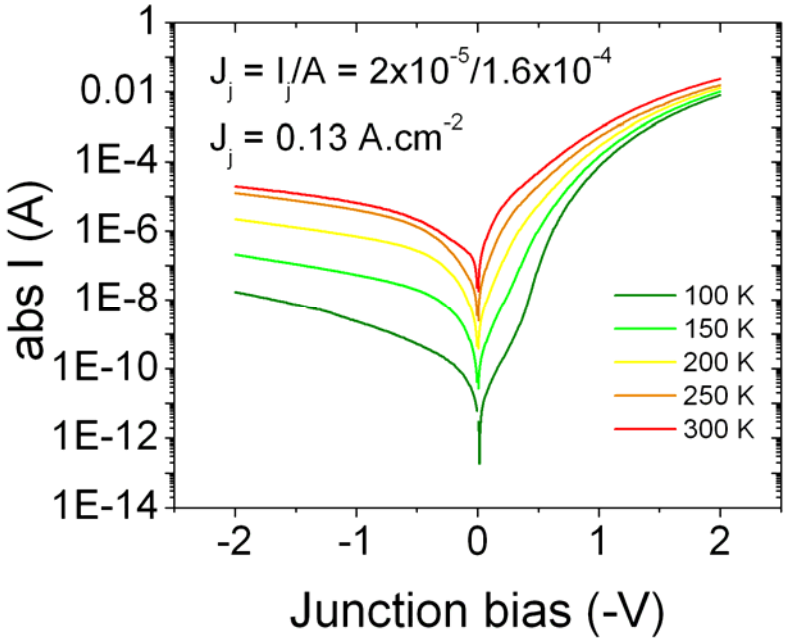


Process	Total Dopant	R_{sh} (ohm/□) Hall	Mob ($cm^2 V^{-1}s^{-1}$)
PVD SiN	3.5E+13	104	2570
ALD SiO_2	4E+13	223.5	1570
ALD Al_2O_3	1.9E+13	296.8	1830
250°C SiO_2	2.5E+13	291	1310

Temp Dependence on Leakage Current



MLD



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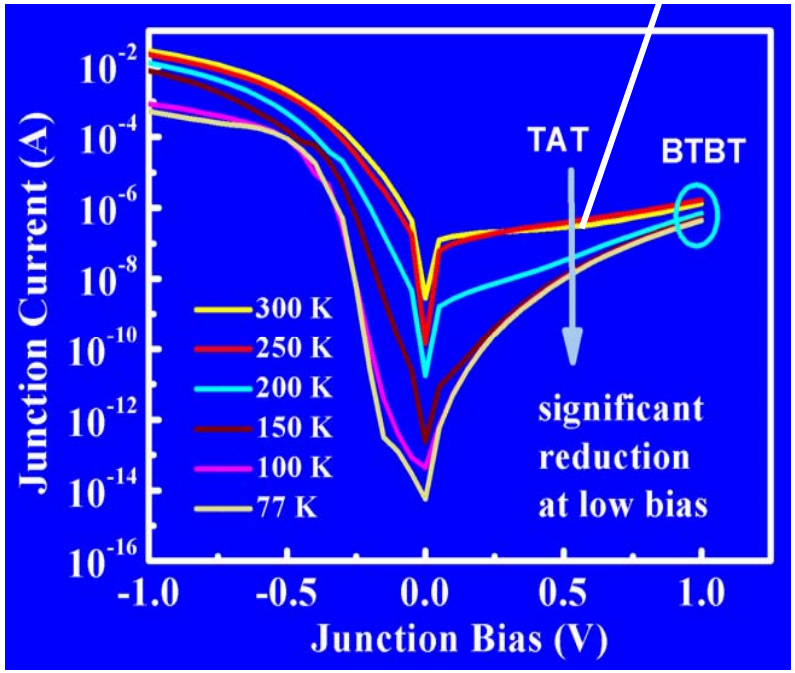
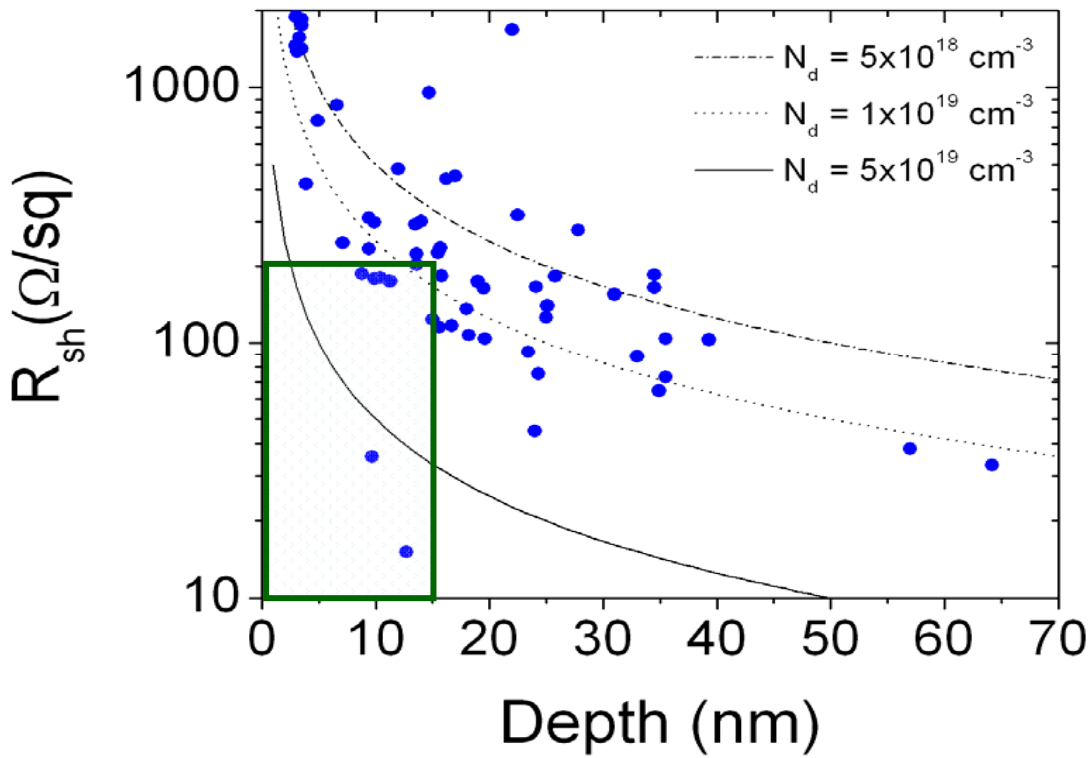


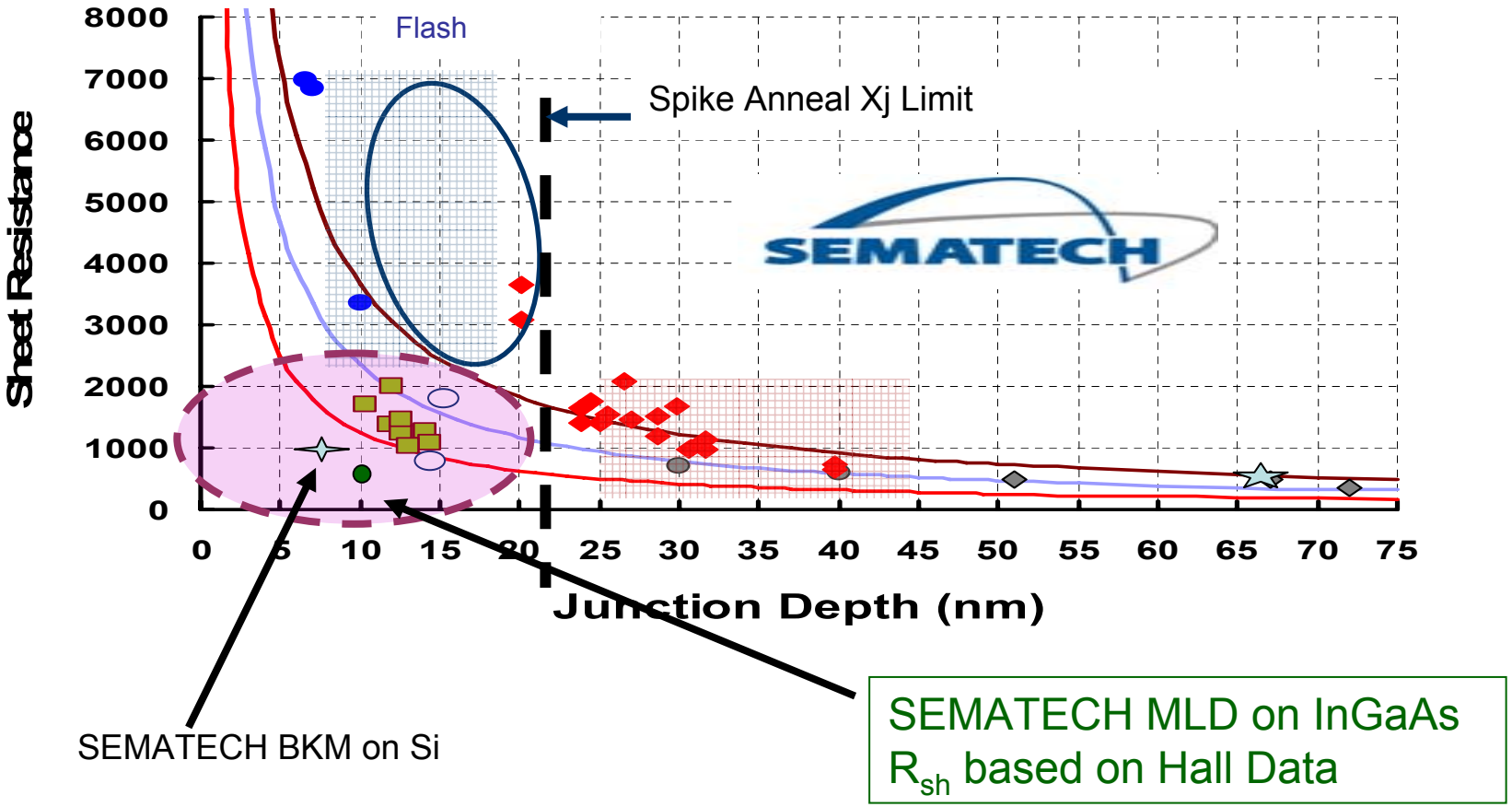
MLD reverse junction leakage shows stronger temp. dependence indicating damage induced tunneling process is not dominant.

Self-aligned III-V USJ with Low R_{sh}



- Self aligned junction formation without regrowth.
- Steep junctions with low R_{sh}
- Achieving X_j and R_{sh} targets

Benchmarking MLD Results



Promising process for self aligned junctions in III-V FETs for low R_{ext}

MLD of III-V: Manufacturing Issues to Address

- n-dopant - Ammonium sulfide solution $(NH4)_2S_x$, not environmentally friendly
  - Very Toxic – stringent storage requirements
  - Processing limited to below 45°C
  - Off-site disposal may be required
  - BUT – solutions exist

- p-dopant identification challenging

Summary

- Power constrained CMOS scaling and control of short channel effects ⇒ challenges for junctions
- New materials and new architectures require new techniques and processes
  - FinFETS - Shallow conformal doping
  - III-V Materials – Shallow non-damaging doping
- SEMATECH has successfully demonstrated a 200mm manufacturable self-aligned III-V MLD USJ with low R_{sh} using wet processing
- SEMATECH's advanced process and device technologies for USJ's are enabling CMOS Scaling

Worldwide collaboration
SEMATECH and ISMI members